DATA SHEET

Part No.	AN12959A
Package Code No.	UBGA021-W-2525AEA

Contents

AN12959A

I²C bus control compatible AGC built-in stereo BTL amplifier IC (For driving a piezoelectric speaker)

■ Overview

AN12959A has a built-in AGC function in a stereo BTL amplifier for driving a piezoelectric speaker to prevent noise at output clip. And I²C bus control method is applied in switching of each mode like some Standby function is turned ON/OFF.

■ Features

- The piezoelectric speaker can be driven by applying the circuit of high withstand voltage power amplifier.
- On level in AGC can be selected by controlling I²C bus.
- Attack and recovery times in AGC can be selected by controlling I²C bus.
- Resistance and capacitor, which were used for conventional analog AGC aren't needed anymore.
- I²C is controlled almost in the same way as those of AN12979A/AN12978A.
- Shut-down function is mounted.
- Amplifier gain switching
- The input circuit constructs a bus boost circuit easily and improves the sound quality of the piezoelectric speaker.

■ Applications

- Audio amplifier for mobile, such as a cellular phone

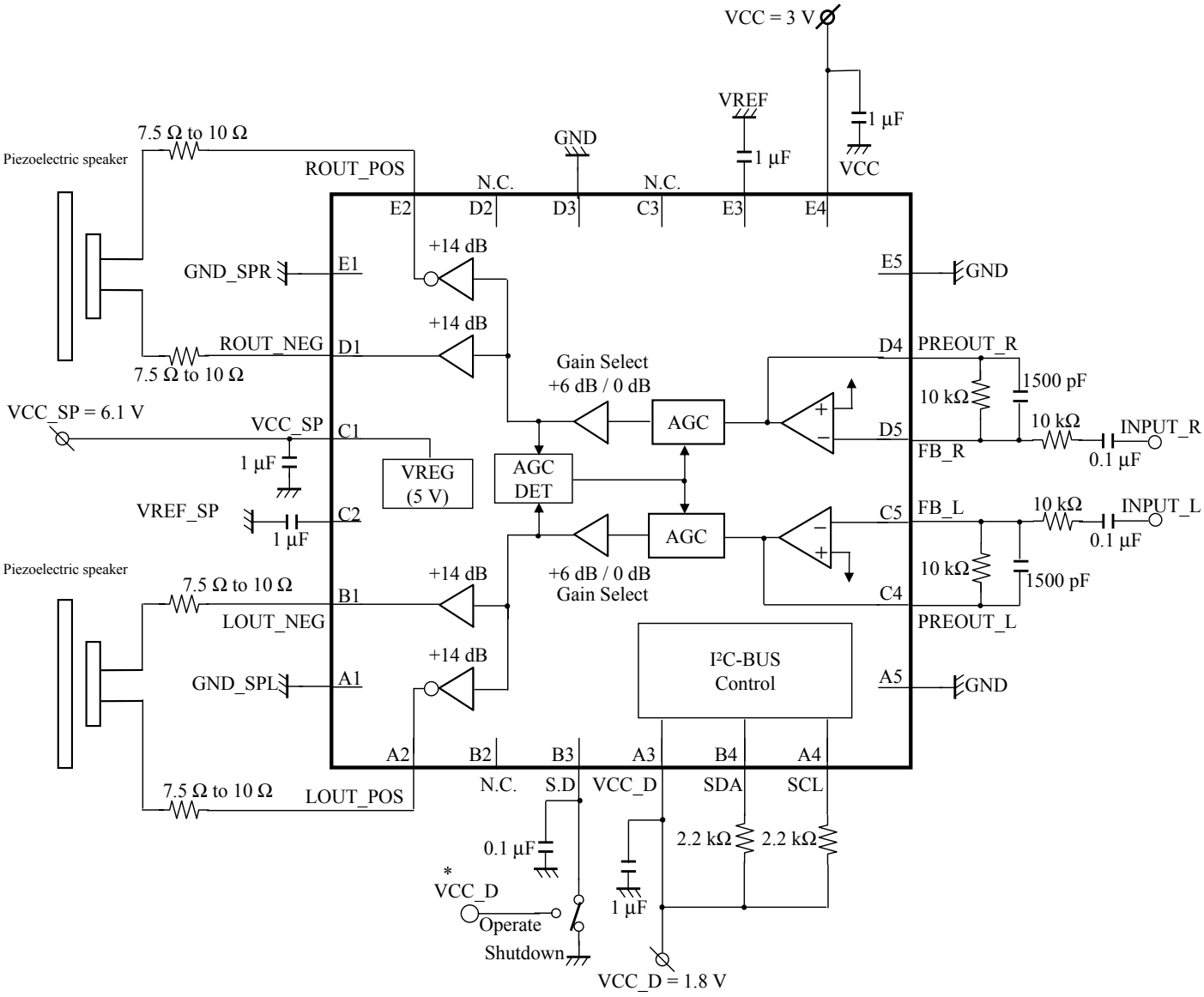
■ Package

- 21 pin plastic quad 5 column BGA package (0.5 mm pitch)

■ Type

- Silicon Monolithic Bi-CMOS IC

■ Application Circuit Example (Block Diagram)



B3 pin Operate voltage

VCC_D = 1.8 V	VCC_D = 2.6 V
Operate > 1.62 V	Operate > 2.34 V
Shut-down < 0.18 V	Shut-down < 0.26 V

Note) 1. This circuit and these circuit constants show an example and do not guarantee the design as a mass-production set.
2. *: The threshold voltage at Pin B3 has the VCC_D dependency.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
A1	GND_SPL	Ground	Grounding (For speaker L-channel)
A2	LOUT_POS	Output	Speaker output L-channel (+)
A3	VCC_D	Power Supply	VCC_D for logic circuit
A4	SCL	Input	SCL
A5	GND	Ground	Grounding
B1	LOUT_NEG	Output	Speaker output L-channel(–)
B2	N.C.	—	N.C.
B3	S.D	—	Shut-down pin
B4	SDA	Input / Output	SDA
C1	VCC_SP	Power Supply	VCC_SP for the circuit of speaker output
C2	VREF_SP	Input	Reference voltage pin for the circuit of speaker output
C3	N.C.	—	N.C.
C4	PREOUT_L	Output	First amplifier output L-channel
C5	FB_L	Input	First amplifier negative feedback input L-channel
D1	ROUT_NEG	Output	Speaker output R-channel(–)
D2	N.C.	—	N.C.
D3	GND	Ground	Grounding
D4	PREOUT_R	Output	First amplifier output R-channel
D5	FB_R	Input	First amplifier negative feedback input R-channel
E1	GND_SPR	Ground	Grounding (For speaker R-channel)
E2	ROUT_POS	Output	Speaker output R-channel(+)
E3	VREF	Input	Reference voltage pin
E4	VCC	Power Supply	Power supply VCC
E5	GND	Ground	Grounding

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage	VCC	5.0	V	*1
		VCC_D	3.6		
		VCC_SP	12		
2	Supply current	I_{CC}	—	A	—
3	Input voltage	VI	—	V	—
4	Power dissipation	P_D	113	mW	*2
5	Operating ambient temperature	T_{opr}	–20 to +70	°C	*3
6	Storage temperature	T_{stg}	–55 to +150	°C	*3

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The power dissipation shown is the value at T_a = 70°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the • P_D – T_a diagram in the ■ Technical Data and use under the condition not exceeding the allowable value.

*3: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	VCC	2.7 to 4.5	V	*1
	VCC_D	1.7 to 2.6		*1, *2
		1.7 to 3.3		*1, *3
	VCC_SP	5.9 to 11.5		*1

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The values under FAST- mode.

*3: The values under STANDARD- mode.

■ Electrical Characteristics at VCC = 3.0 V, VCC_D = 1.8 V, VCC_SP = 6.1 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
Circuit Current								
1	Circuit current 1A at non-signal (VCC)	IVCC1A	Non-signal, STB = OFF, SP = ON, AGC = ON	—	0.5	1.0	mA	—
2	Circuit current 2A at non-signal (VCC_SP)	IVCC2A	Non-signal, STB = OFF, SP = ON, AGC = ON	—	9.0	18	mA	—
3	Circuit current 3A at non-signal (VCC_D)	IVCC3A	Non-signal, STB = OFF, SP = ON, AGC = ON	—	0.1	10	µA	—
4	Circuit current 1B at non-signal (VCC)	IVCC1B	Non-signal, STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	—
5	Circuit current 2B at non-signal (VCC_SP)	IVCC2B	Non-signal, STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	—
6	Circuit current 3B at non-signal (VCC_D)	IVCC3B	Non-signal, STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	—
7	Circuit current 1C at non-signal (VCC)	IVCC1C	Non-signal, STB = OFF, SP = OFF, AGC = ON	—	0.5	1.0	mA	—
8	Circuit current 2C at non-signal (VCC_SP)	IVCC2C	Non-signal, STB = OFF, SP = OFF, AGC = ON	—	4.5	6.5	mA	—
9	Circuit current 3C at non-signal (VCC_D)	IVCC3C	Non-signal, STB = OFF, SP = OFF, AGC = ON	—	0.1	10	µA	—
I/O Characteristics								
10	SP reference output level	VSPOL VSPOR	Vin = –26.0 dBV, f = 1 kHz, RL = 100 Ω	–1.0	0.0	1.0	dBV	—
11	SP reference output distortion	THSPOL THSPOR	Vin = –26.0 dBV, f = 1 kHz, RL = 100 Ω, to THD 5th	—	0.07	0.5	%	—
12	SP reference output noise voltage	VNSPOL VNSPOR	Non-Signal using A curve filter	—	–75	–68	dBV	—
13	Output level at SP Save	VSSPOL VSSPOR	Vin = –26.0 dBV, f = 1 kHz, RL = 100 Ω, using A curve filter	—	–114	–90	dBV	—
14	SP AGC output level	VSPOA1L VSPOA1R	Vin = –6.0 dBV, f = 1 kHz, RL = 100 Ω, VCC_SP = 10 V, AGC – SELECT = [010]	12.9	13.9	14.9	dBV	—

■ Electrical Characteristics at VCC = 3.0 V, VCC_D = 1.8 V, VCC_SP = 6.1 V (continued)

Note) T_a = 25°C±2°C unless otherwise specified.

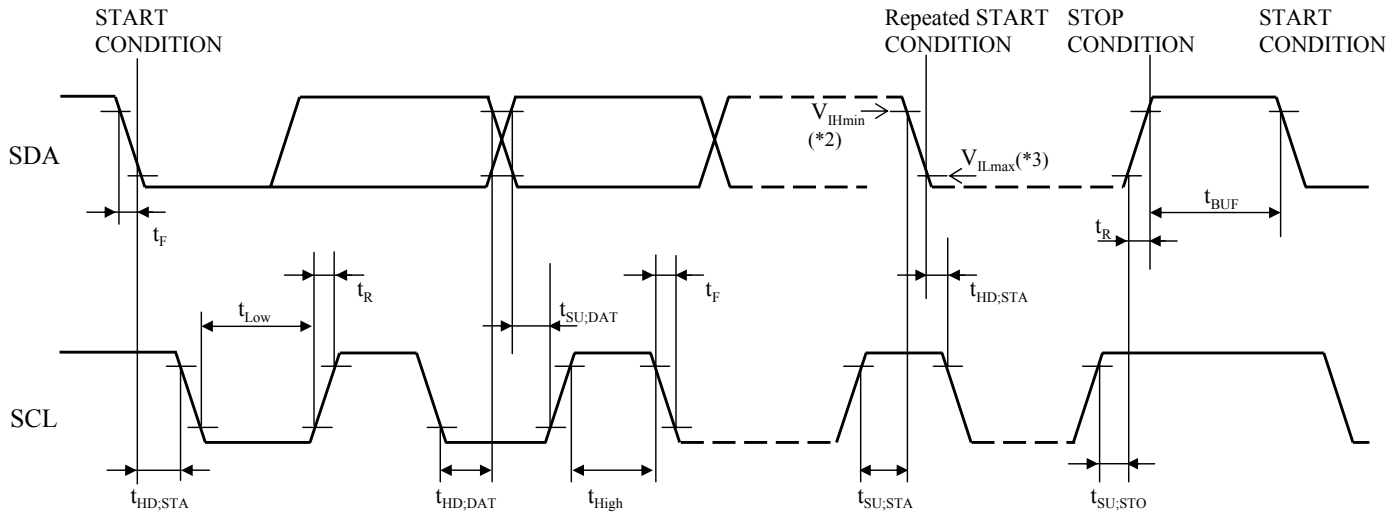
B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I^2C interface								
15	SCL, SDA signal input Low level	V_{IL}	—	–0.5	—	0.3 × VCC_D	V	—
16	SCL, SDA signal input High level	V_{IH}	—	0.7 × VCC_D	—	VCC_D + 0.5	V	—
17	SDA signal output Low Level	V_{OL}	Open corrector, sync current: 3mA	0	—	0.2 × VCC_D	V	—
18	SCL, SDA signal input current	I_i	Input voltage 0.1 V to 1.7 V	–10	—	10	µA	—
19	Max. frequency of SCL signal allowable to input	f_{SCL}	—	0	—	400	kHz	—
The threshold voltage at Pin B3								
20	Shut-down input Low level	Vsdlth	—	—	—	0.1 × VCC_D	V	—
21	Shut-down input High level	Vsdhth	—	0.9 × VCC_D	—	—	V	—

■ Electrical Characteristics (Reference values for design) at $V_{DD} = V_{MSP} = V_{MAC} = V_{MST} = V_{MBX} = V_{MLO} = 5$ V, $V_{REF} = 1.65$ V, STBY = 3.3 V

Note) $T_a = 25°C \pm 2°C$ unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I²C interface								
31	Bus free time between stop and start conditions	t_{BUF}	—	1.3	—	—	µs	*1
32	Setup time of start condition	$t_{SU;STA}$	—	0.6	—	—	µs	*1
33	Hold time of start condition	$t_{HD;STA}$	—	0.6	—	—	µs	*1
34	Low period of SCL clock	t_{Low}	—	1.3	—	—	µs	*1
35	High period of SCL clock	t_{High}	—	0.6	—	—	µs	*1
36	Rising time of SDA, SCL signal	t_R	—	—	—	0.3	µs	*1
37	Falling time of SDA, SCL signal	t_F	—	—	—	0.3	µs	*1
38	Data setup time	$t_{SU;DAT}$	—	0.1	—	—	µs	*1
39	Data hold time	$t_{HD;DAT}$	—	0	—	0.9	µs	*1
40	Setup time of stop condition	$t_{SU;STO}$	—	0.6	—	—	µs	*1

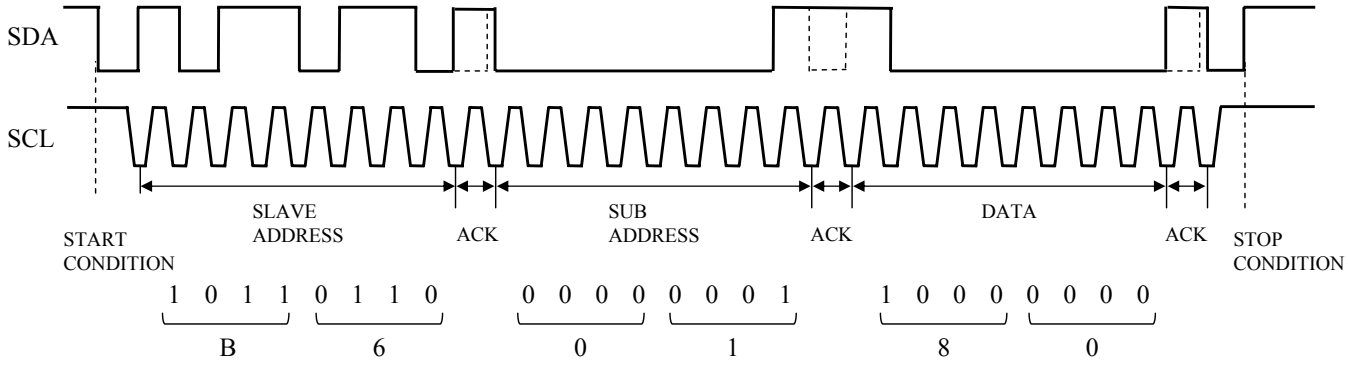
Note) *1: All values are V_{IHmin} (*2) and V_{ILmax} (*3) level standard.
*2: V_{IHmin} is the minimum limit of the signal input high level.
*3: V_{ILmax} is the maximum limit of the signal input low level.



■ Technical Data

- I^2C-bus mode

1. Write mode



Example of transmission messages

Two transmission messages (i.e. the SCL and SDA) are sent in synchronous serial transmission. The SCL is a clock with fixed frequency. The SDA indicates address data for the control of the reception side, and is sent in parallel in synchronization with the SCL. The data is transmitted in 8-bit, 3 octets (bytes) in principle, where every octet has an acknowledge bit. The following description provides information on the structure of the frame.

<Start Conditions>

When the level of the SDA changes to low from high while the level of the SCL is high, the data reception of the receiver will be enabled.

<Stop Conditions>

When the level of the SDA changes to high from low while the level of the SCL is high, the data reception of the receiver will be aborted.

<Slave Address>

The slave address is a specified one unique to each device. When the address of another device is sent, the reception will be aborted.

<Sub-Address>

The sub-address is a specified one unique to each function.

<Data>

Data is information under control.

<Acknowledge Bit>

The acknowledge bit is used to enable the master to acknowledge the reception of data for each octet. The master acknowledges the data reception of the receiver by transmitting a high-level signal to the receiver and receiving a low-level signal returned from the receiver as shown by the dotted lines in the above Fig. The communication will be aborted if the low signal is not returned.

The SDA will not change when the level of the SCL is high except start or stop conditions are enabled.

■ Technical Data (continued)

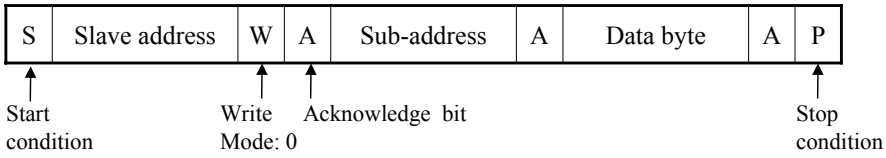
- I²C-bus mode (continued)

1.Write mode (continued)

(a) I²C-bus PROTOCOL

・Slave address: 10110110 (B6Hex)

・Format (Normal)

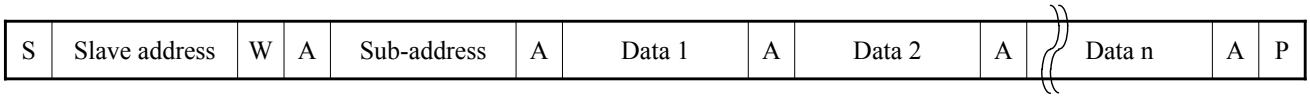


(b) Auto increment

・Sub-address 0*Hex: Auto increment mode

(When the data is sent in sequence, the sub-address will change one by one and the data will be input.)

・Auto increment mode



(c) Initial condition

The initial state of the device is not guaranteed. Therefore, the input of 00Hex resister-D0(Note.1) will be absolutely "0", when the power is turned ON.

(d) Sub-address Byte and Data Byte Format

Sub-address	MSB Data byte LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
*0Hex	GAIN 0 → +20 dB 1 → +26 dB	0 (*1)	0 (*1)	0 (*1)	AGC 0 → OFF 1 → ON	SP Save 0 → ON 1 → OFF	Standby 0 → ON 1 → OFF	0 (*1)
*1Hex	AGC-ON data bit3	AGC-ON data bit2	AGC-ON data bit1	AGC-REC data bit3	AGC-REC data bit2	AGC-REC data bit1	AGC-ATT data bit2	AGC-ATT data bit1
*2Hex	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)

Note) *1: <00Hex Register>

D0, D4, D5, D6: Always set to "0"。

D1: Standby ON/OFF switch

D2: D2: SP Save ON/OFF switch

D3: AGC ON/OFF switch

D7: GAIN +20 dB / +26 dB selection

<01Hex Register>

D0, D1: AGC-attack-time selection

D2, D3, D4: AGC-recovery-time selection

D5, D6, D7: AGC-on-level selection

<02Hex Register>

Always set to "0". (test & adjust mode).

*2: Please use these bit only Data = "0", because they are used by our company's final test and fine-tuning AGC-on level. Note that Data = "1" is not shut-down mode.

■ Technical Data (continued)

- I²C-bus mode (continued)

1. Write Mode (continued)

(e) AGC-attack-time selection

Write 01Hex Register		Attack time
D1	D0	
0	0	0.5 ms
0	1	1 ms
1	0	2 ms
1	1	4 ms

(f) AGC-recovery-time selection

Write 01Hex Register			Recovery time
D4	D3	D2	
0	0	0	1.0 s
0	0	1	1.5 s
0	1	0	2.0 s
0	1	1	3.0 s
1	0	0	4.0 s
1	0	1	6.0 s

(g) AGC-on-level selection at VCC = 3.0 V, VCC_D = 1.8 V, VCC_SP = 6.1 V *1

Write 01Hex Register			AGC On Level	Output (V[p-p])	VCC_SP (Reference) *2
D7	D6	D5			
0	0	0	12.6 dBV	12 V[p-p]	8.5 V ≤
0	0	1	13.2 dBV	13 V[p-p]	9.0 V ≤
0	1	0	13.9 dBV	14 V[p-p]	9.5 V ≤
0	1	1	14.5 dBV	15 V[p-p]	10.0 V ≤
1	0	0	15.1 dBV	16 V[p-p]	10.5 V ≤
1	0	1	15.6 dBV	17 V[p-p]	11.0 V ≤
1	1	0	16.1 dBV	18 V[p-p]	11.0 V ≤ *3
1	1	1	16.6 dBV	19 V[p-p]	11.0 V ≤ *3

Note) *1: At the time of VCC_SP = 6.1 V, output is clipped, excessive clip in AGC OFF can be prevented.
*2: The supply voltage of VCC_SP at which output is not clipped.
*3: Output is clipped a little.

(h) Amp. gain selection at VCC = 3.0 V, VCC_D = 1.8 V, VCC_SP = 6.1 V

Write 00Hex Register	Gain
D7	
0	20 dB
1	26 dB

■ Technical Data (continued)

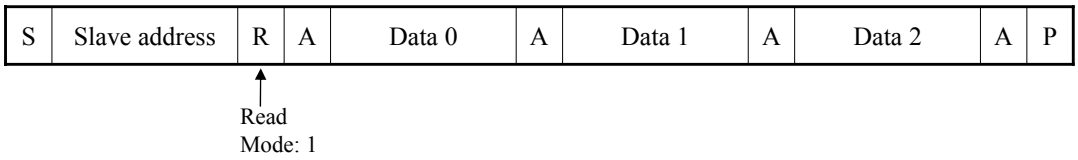
- I²C-bus mode (continued)

2. Read Mode

(a) I²C-bus PROTOCOL

・Slave address 10110111 (B7Hex)

・Format



Note) At the slave address input, it is sequentially output from Data 0. There is no necessity for inputting the sub-address.

(b) Sub-address Byte and Data Byte Format

	MSB			Data byte				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Data 0	Sub-address *0Hex Latch data D7	Sub-address *0Hex Latch data D6	Sub-address *0Hex Latch data D5	Sub-address *0Hex Latch data D4	Sub-address *0Hex Latch data D3	Sub-address *0Hex Latch data D2	Sub-address *0Hex Latch data D1	Sub-address *0Hex Latch data D0
Data 1	Sub-address *1Hex Latch data D7	Sub-address *1Hex Latch data D6	Sub-address *1Hex Latch data D5	Sub-address *1Hex Latch data D4	Sub-address *1Hex Latch data D3	Sub-address *1Hex Latch data D2	Sub-address *1Hex Latch data D1	Sub-address *1Hex Latch data D0
Data 2	Sub-address *2Hex Latch data D7	Sub-address *2Hex Latch data D6	Sub-address *2Hex Latch data D5	Sub-address *2Hex Latch data D4	Sub-address *2Hex Latch data D3	Sub-address *2Hex Latch data D2	Sub-address *2Hex Latch data D1	Sub-address *2Hex Latch data D0

This IC is compatible with I²C-bus format.
Purchase of Panasonic I²C Components conveys a license under the Philips I²C patent right to use these components in an I²C systems, provided that the system conforms to the I²C standard specifications as defined by Philips.

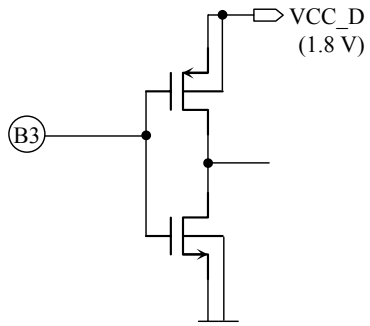
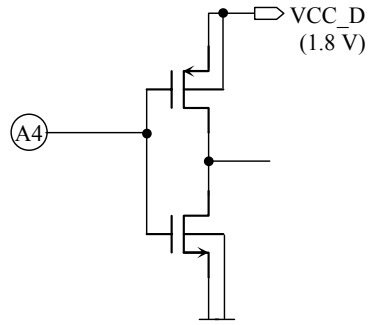
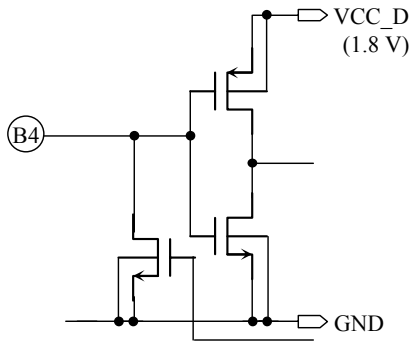
- Operating temperature guarantee of I²C-bus Control

The performance in the ambient temperature of operation is guaranteed theoretically in the design at normal temperature (25°C) by inspecting it at a speed of the clock that is about 50% earlier regarding the operating temperature guarantee of I²C-bus Control. But the following characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Panasonic will respond in good faith to customer concerns.

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions

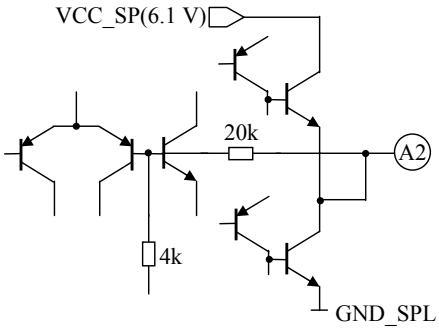
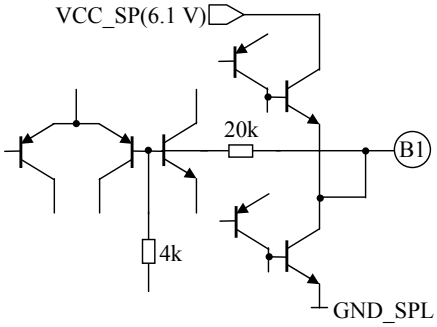
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
B3	S.D Hi-Z		Input impedance = Hi-Z	Shut-down mode pin Please do not make it open, because the open S.D pin is not fixed.
A4	SCL  Hi-Z		Input impedance = Hi-Z	I^2C-BUS SCL pin
B4	SDA  Hi-Z		Input impedance = Hi-Z	I^2C-BUS SDA pin
A3	VCC_D 1.8 V(typ.)	—	—	Power supply pin for I^2C-BUS

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

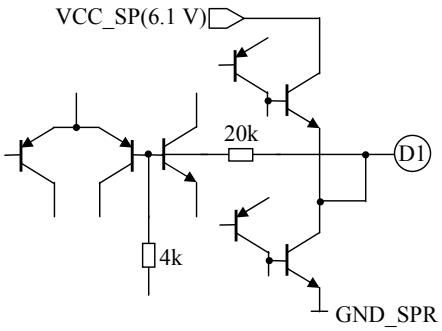
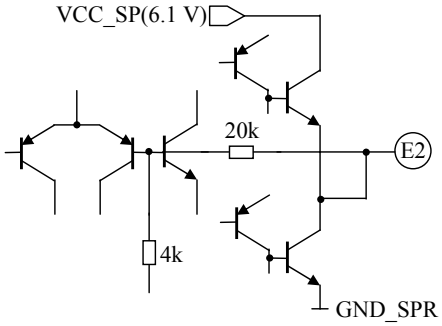
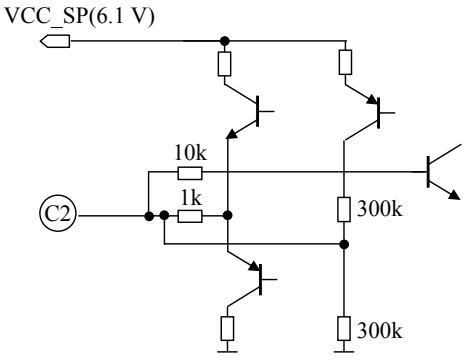
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
A2	LOUT_POS  DC 2.7 V		Output impedance = Equal to or less than 1 Ω	L-channel positive speaker output pin
A1	GND_SPL DC 0 V	—	—	Ground pin for L-channel speaker output
B1	LOUT_NEG  DC 2.7 V		Output impedance = Equal to or less than 1 Ω	L-channel negative speaker output pin
C1	VCC_SP 6.1 V(typ.)	—	—	Power supply pin for speaker output

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

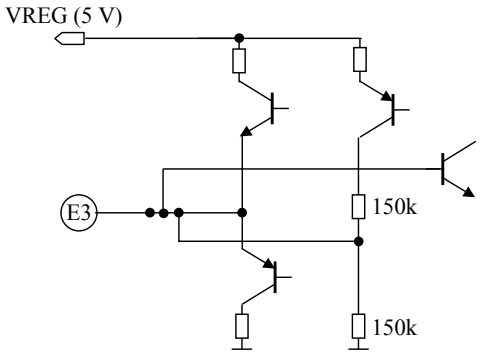
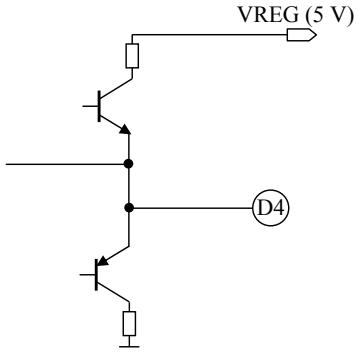
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
D1	ROUT_NEG  DC 2.7 V		Output impedance = Equal to or less than 1 Ω	R-channel negative speaker output pin
E1	GND_SPR DC 0 V	—	—	GND pin for R-channel speaker output
E2	ROUT_POS  DC 2.7 V		Output impedance = Equal to or less than 1 Ω	R-channel positive speaker output pin
C2	VREF_SP DC 2.7 V		Input impedance = About 150 kΩ	The reference voltage terminal for determining DC bias of the output stage of a speaker amplifier system. Please connect an external capacitor to remove a ripple.

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

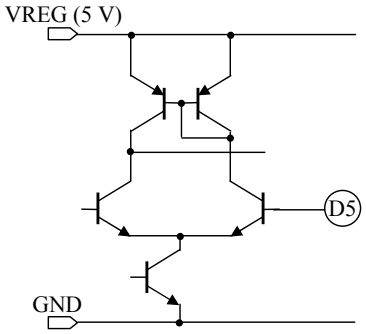
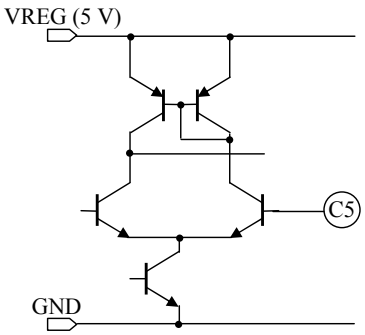
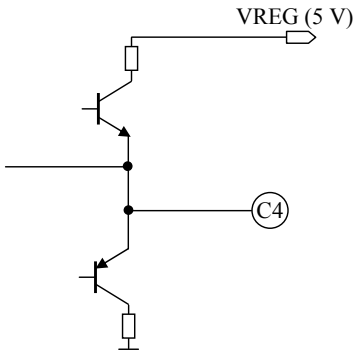
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
A5 E5 D3	GND DC 0 V	—	—	Ground pin
E4	VCC 3.0 V(typ.)	—	—	Power supply pin
E3	VREF DC 2.5 V		Input impedance = About 75 kΩ	The reference voltage terminal for determining DC bias of the input stage of a speaker amplifier system. Please connect an external capacitor to remove a ripple.
D4	PREOUT_R  DC 2.5 V		Output impedance = Equal to or less than 10 Ω	Output terminal of R-channel input amplifier of speaker amplifier system. Please connect external resistance for the gain setting.

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

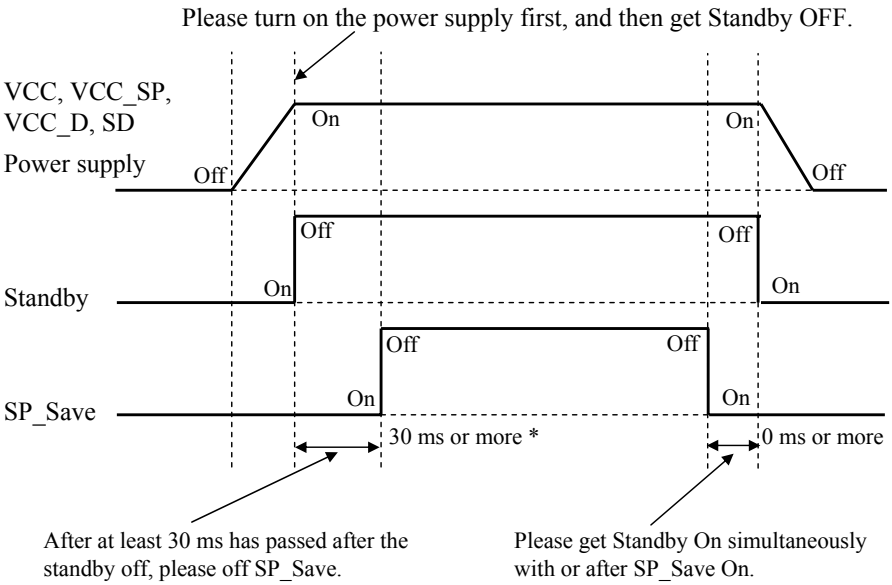
Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
D5	FB_R DC 2.5 V		Input impedance = Hi-Z	Feedback terminal of R-channel input amplifier of speaker amplifier system. The gain of the R-channel input amplifier can be set by connecting an external resistance between Pin D4 and Pin D5.
C5	FB_L DC 2.5 V		Input impedance = Hi-Z	Feedback terminal of L-channel input amplifier of speaker amplifier system. The gain of the L-channel input amplifier can be set by connecting an external resistance between Pin C4 and Pin C5.
C4	PREOUT_L  DC 2.5 V		Output impedance = Equal to or less than 10 Ω	Output terminal of L-channel input amplifier of speaker amplifier system. Please connect external resistance for the gain setting.
B2 C3 D2	N.C.	—	Input impedance = Hi-Z	Feedback terminal of R-channel input amplifier of speaker amplifier system. The gain of the R-channel input amplifier can be set by connecting an external resistance between Pin D4 and Pin D5.

■ Technical Data (continued)

- Power supply and logic sequence

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.
The timing control of power-ON/OFF and each logic according to the procedure below should be recommended for the best pop performance caused in switching.

1. The sequence of the power supply and each logic



The basic procedure at the power-on

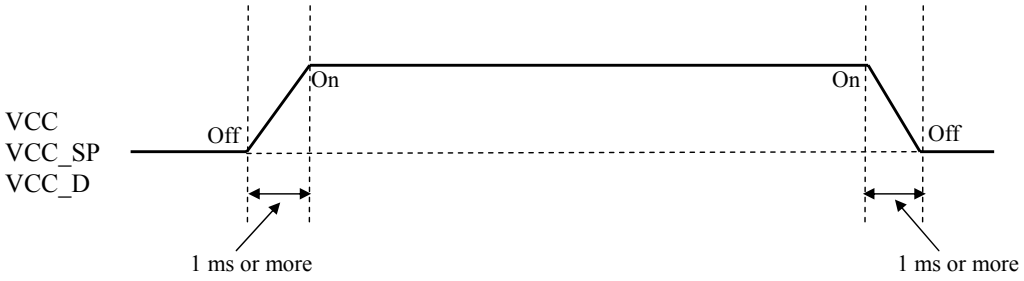
1. The power OFF condition.
   Both the Standby and the SP_Save are in the ON condition.
2. Power ON
3. Standby OFF
4. SP_Save OFF

The basic procedure at the power-off

1. The power ON condition.
   Both the Standby and the SP_Save are in the OFF condition.
2. SP_Save ON (= Standby ON)
3. Standby ON
4. Power OFF

Note) *: This IC contains the pre-charge circuit. It is time until each bias is stabilized from Standby Off. It depends for this time on the capacity value linked to a reference voltage terminal (VREF and VREFSP), and the capacity value and resistance linked to an input terminal (IN_R and IN_L). It is a recommendation value in a constant given in the example of ■ Application Circuit Example (Block Diagram).

2. The sequence of VCC and VCC_SP and VCC_D
   This IC does not have a rising and falling order in VCC, VCC_SP, and VCC_D. Rising and falling times of them are recommended 1 ms or more.



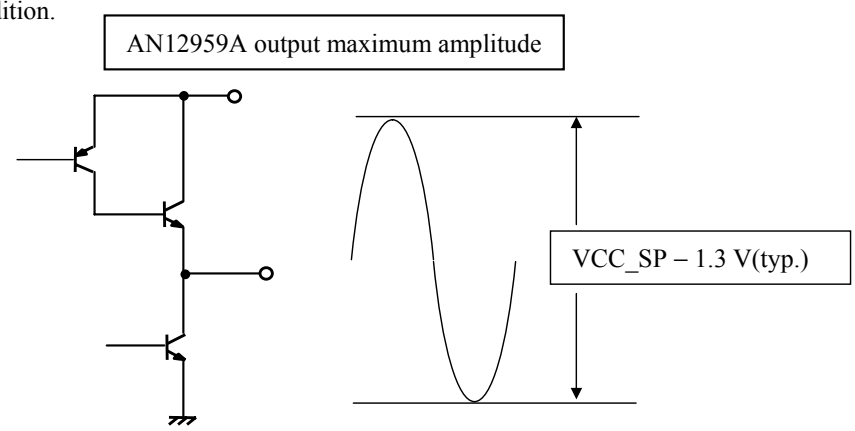
■ Technical Data (continued)

- Explanation on mainly functions

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

1. Power supply

1) Power supply for output amplifier
The output amplifier operates with voltage applied to VCC_SP. When power supply is applied to only VCC_SP in AN12959A, the product does not operate. (In case where voltage is not applied to VCC and VCC_D), it gets in Standby condition.



2) Power supply for control system
The control system operates with power supply applied to VCC pin. (I2C logic, clock generation circuit, etc.)

3) Power supply for signal system
The signal system operates with the internal regulator of 5 V. 5 V, reference voltage of the internal regulator is generated from VCC_SP using VCC power supply. By setting signal voltage at 5 V, the dynamic range of the signal can be secured sufficiently. When the gain of the input amplifier is 0 dB, clip occurs at the amplitude of 3 V[p-p] (typ.) in input signal.

4) Power supply for I2C interface
I^2C interface operates with power supply applied to VCC_D pin. I2C circuit operates with VCC.

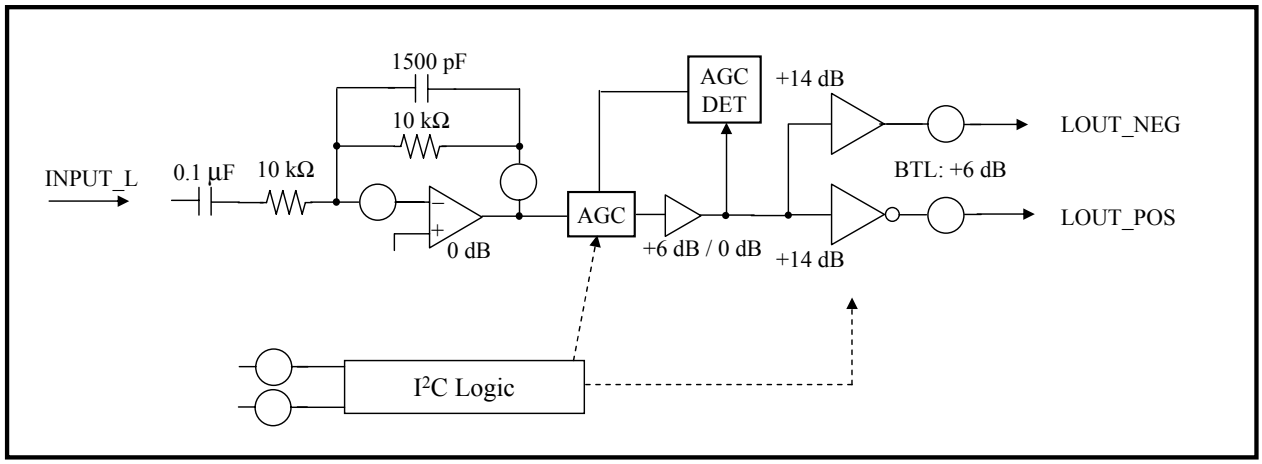
5) High voltage at shut-down pin
Please use the power supply applied to VCC_D or apply voltage from the outside. Threshold voltage depends on the voltage to VCC_D.

■ Technical Data (continued)

- Explanation on mainly functions (continued)

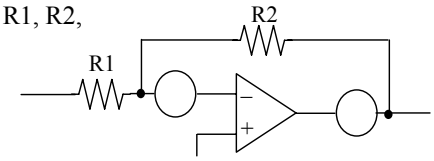
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

2. Speaker amplifier



1) the gain for a input amplifier can be set with an external resistance.
Input impedance is also set with the external resistance. When the gain for the input amplifier is set at ±0 dB, the total gain for the speaker amplifier is +26 dB or +20 dB (It can be selected with I^2C).

When the external resistance for the input amplifier is assumed as R1, R2,



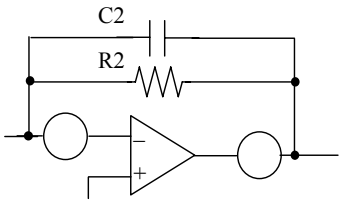
Gain = 20 log (R2 / R1)

Zin = R1

In case of R1 = 10 kΩ, R2 = 10 kΩ with the constants in the above fig, the gain for the input amplifier is ±0 dB and impedance is 10 kΩ. During operation, keep the voltage of R1 and R2 at more than 5 kΩ.

2) With an external capacity added to the input amplifier, LPF, which removes an unwanted high frequency element, can be constructed.

When external resistance is assumed as R2, capacity as C2,



$fc = 1 / (2 \pi \times R2 \times C2)$

In case of R2 = 10 kΩ, C2 = 1500 pF with the constants in the above fig, Cut-off frequency, fc is 10.6 kHz.

■ Technical Data (continued)

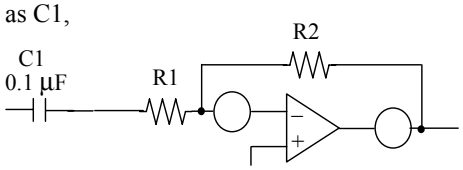
- Explanation on mainly functions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

2. Speaker amplifier (continued)

3) With the smaller capacity of the input AC coupling capacitor, HPF, which removes unwanted low frequency element, can be constructed. When input resistance is assumed as R1, and AC coupling capacitor as C1,

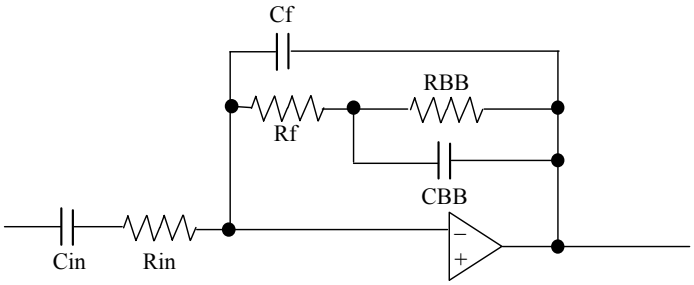
$$fc = 1 / (2 \pi \times R1 \times C1)$$



In case of R1 = 10 kΩ, C1 = 0.1 µF, cut-off frequency, fc is 160 Hz.
In case of R1 = 10 kΩ, C1 = 0.022 µF, cut-of frequency, fc is 720 Hz.

4) Bus Boost circuit can be constructed by adding capacity (RBB) and resistance (CBB) to the input amplifier. The frequency to increase 3 dB is assumed as fo

fo =	$1 / (2 \times \pi \times Rf \times CBB)$
Bus Boost Gain	20 log ((Rf + RBB) / Rf)
Ao =	20 log ((Rf + RBB) / Rin)



3. Protection circuit for speaker amplifier

1) Thermal protection circuit
The thermal protection circuit operates at the Tj of approximately 150°C. The thermal protection circuit is reset automatically when the temperature drops.

2) Output pin short protection circuit
- Output pin-power supply line short protection
- Output-to-output pin short protection
- Output pin-GND line short protection

If short-circuit is no longer detected, it will return automatically.

Note) Operation is not guaranteed although the protection circuit is built in. Moreover, hundred percent inspection is not guaranteed.

■ Technical Data (continued)

- Explanation on mainly functions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

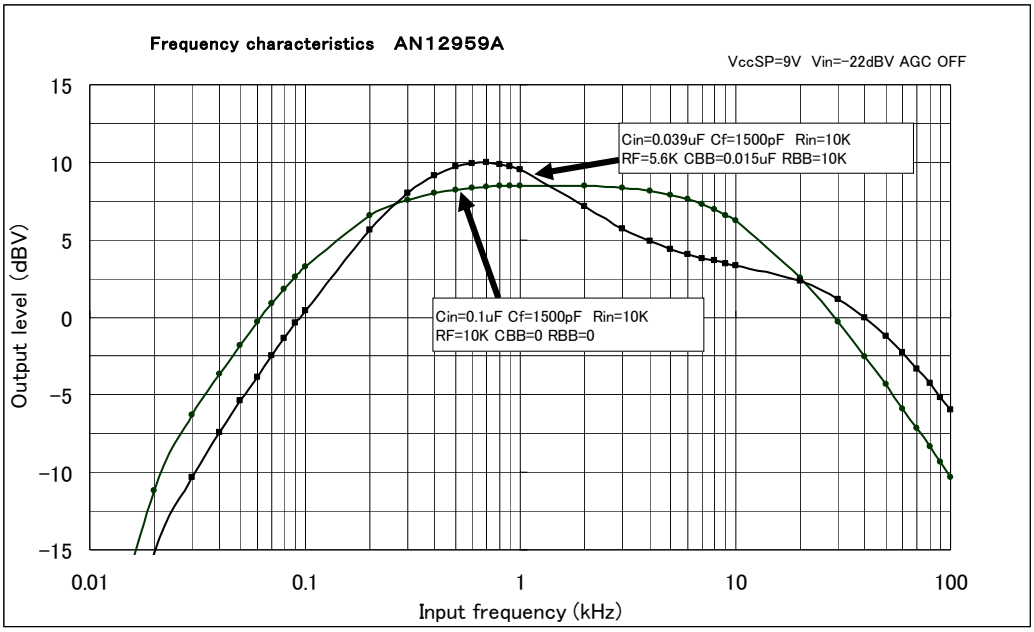
4. Cautions

1) Cautions about AGC

Signal output in the input amplifier is detected and converted to forward current. Compared this forward current with reference voltage, if the forward current is larger, AGC turns ON.
When the frequency band of the speaker is narrower than that of the amplifier.
If maximum input is made in low frequency band, AGC operates to decrease volume. Namely, low sound part is not heard from a speaker, but AGC reacts to low sound part to turn down the volume. Please carefully design so that the frequency bands is synchronized between the speaker and amplifier.

Note) Frequency characteristics should be set not only for the speaker, but in the built-in condition.

The below Graph shows when the values of resistance and capacity are changed.



2) Cautions about VCC_SP ON/OFF

With VCC in AN12959A always on, when VCC_SP is turned ON/OFF, I²C data is retained. When VCC_SP is turned ON → OFF → ON without I2C control, pop sound comes out, as starting time for the amplifier gets significantly long.
(Input amplifier, AGC circuit, and standard voltage are provided by VCC_SP).

Note) Please never fail to turn ON Standby and SP_Save with I²C first, and then turn OFF VCC_SP. Next, turn ON VCC_SP, and turn OFF Standby and SP_Save to operate amplifier with I²C.
If Standby is switched from ON to OFF with I²C, the amplifier starts within a short time, as a circuit runs to quickly charge an external condenser connected to Vref pin.
(When VCC_SP is turned ON → OFF → ON without Standby control, the circuit of fast charge does not run.)
Please space the time of 30 ms from turning Standby ON → OFF to SP_Save OFF.

3) Cautions about shut-down with SD pin

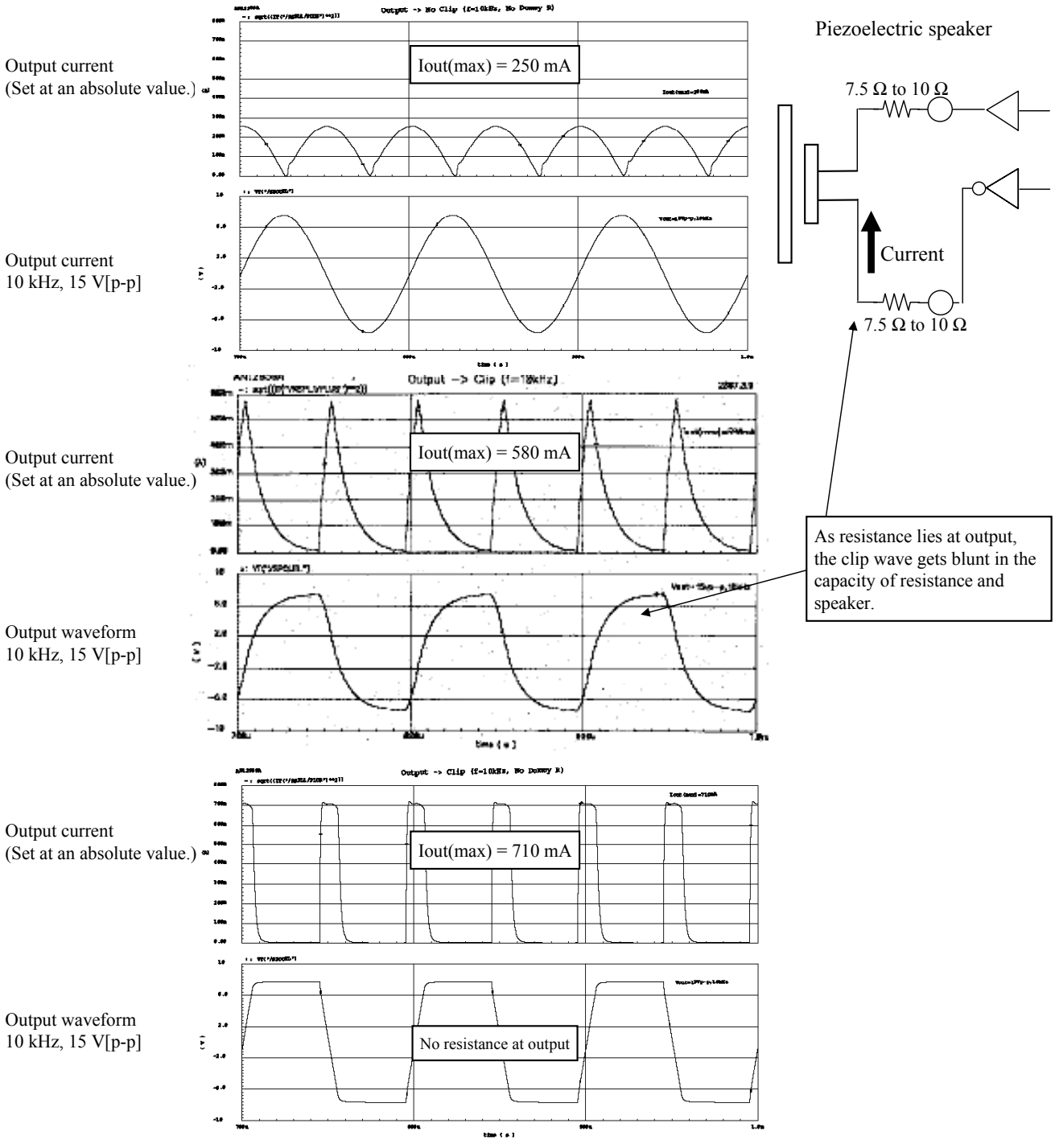
During normal operation, when a shut-down pin is turned Low directly, shock noise comes out.
As SP_Save is set in mute, first turn ON SP_Save, and then turn ON Standby to stop operation. Finally, set shut-down pin to Low.

■ Technical Data (continued)

- Simulation of output current waveform

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

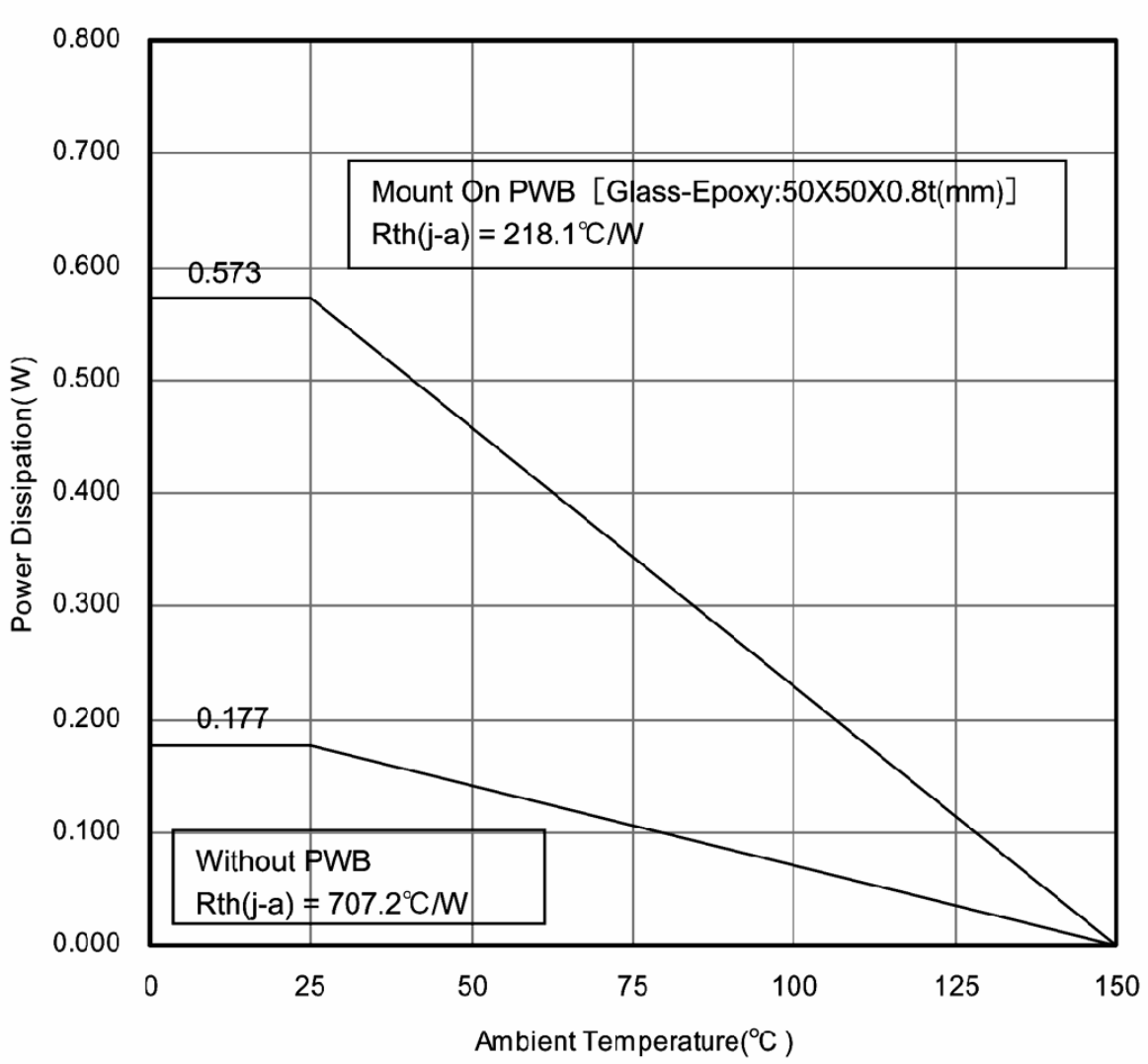
(There is twice as much difference as between current and voltage in a piezoelectric speaker per 1 channel.)
A piezoelectric speaker of ceramic lamination type is used.



If output waveform is clipped without resistance of more than 7.5 Ω × 2 at amplifier output, excessive current runs. Please never fail to insert resistance in use. Excessive current can cause intermittent output signal with load-short protection operated.

■ Technical Data (continued)

• P_D — T_a diagram



■ Usage Notes

1. Please carry out the thermal design with sufficient margin such that the power dissipation will not be exceeded, based on the conditions of power supply, load and surrounding temperature. Although indicated also in the column of the maximum rating, the maximum rating becomes an instant and the marginal value which must not exceed. It sufficiently evaluates, and I use-wish-do so that it may not exceed certainly. Moreover, don't impress neither voltage nor current to PIN which is not indicated. It may destroy in both cases.

2. Please pay attention to the pattern layout in order to prevent damage due to short circuit between pins.
   In addition, for the pin configuration, please refer to the ■ Pin Descriptions.

3. Please absolutely do not mount the LSI in the reverse direction on to the printed-circuit-board.
   It might be damaged when the electricity is turned on.

4. Please do a visual inspection on the printed-circuit-board before turning on the power supply, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device.
   Also perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

5. Please take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as SP output pin (Pin A2, B1, D1, E2)-power supply pin short, SP output pin-GND short, or SP output-to-SP output-pin short (load short).

6. When using the LSI for model deployment or new products, perform fully the safety verification including the long-turn reliability for each product.

7. Please do not make it open, because the open SD pin (Pin B3) is not fixed.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

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- Any applications other than the standard applications intended.

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(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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