DESCRIPTION

This family is a 4M bit dynamic RAM organized 1,048,576 x 4-bit configuration with Extended Data Out mode CMOS DRAMs. Extended data out mode is a kind of page mode which is useful for the read operation. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50, 60 or 70ns) and package type(SOJ or TSOP-II) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Fast Page Mode operation
- Read-modify-write Capability
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- Max. Active power dissipation

Speed	Power
50	550mW
60	495mW
70	440mW

- JEDEC standard pinout
- 20/26-pin SOJ (300mil)
  20/26-pin TSOP-II (300mil)
- Single power supply of 5V ± 10%
- Early Write or output enable controlled write
- Fast access time and cycle time

Speed	tRAC	tCAC	tPC
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- Refresh cycle

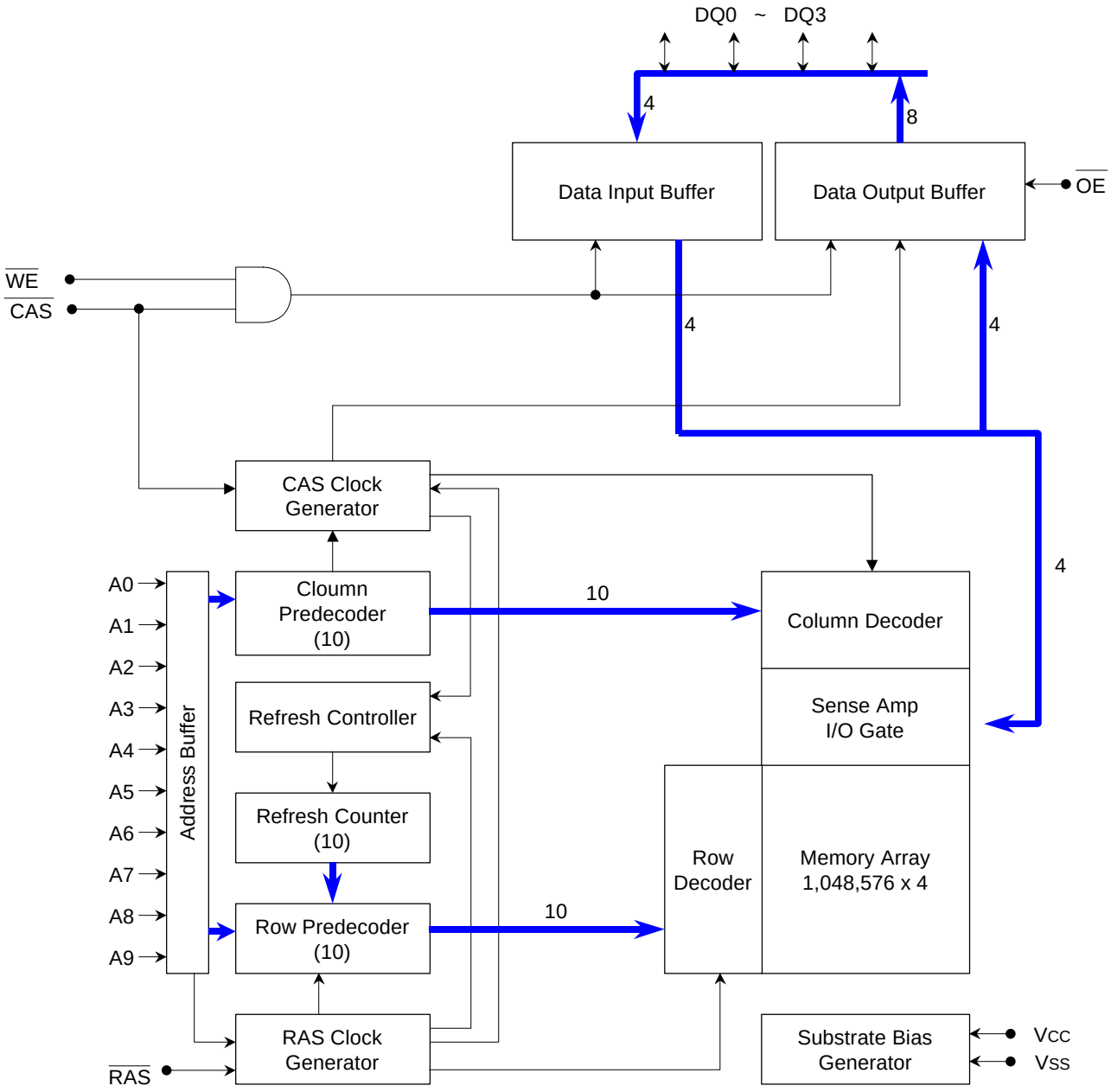
Part number	Refresh	Normal	SL-part
HY514400B	1K	16ms	128ms

ORDERING INFORMATION

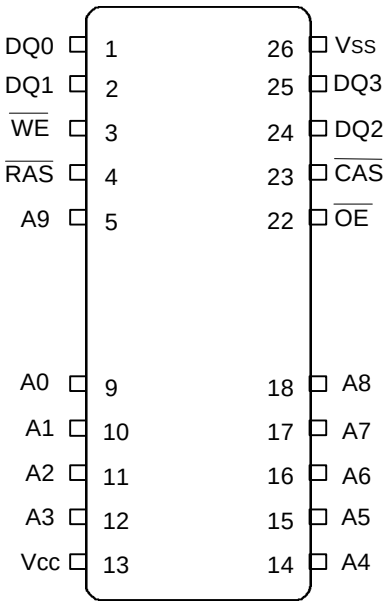
Part Name	Refresh	Power	Package
HY514400BJ	1K		20/26Pin SOJ
HY514400BLJ	1K	L-part	20/26Pin SOJ
HY514400BSLJ	1K	SL-part	20/26Pin SOJ
HY514400BT	1K		20/26Pin TSOP-II
HY514400BLT	1K	L-part	20/26Pin TSOP-II
HY514400BSLT	1K	SL-part	20/26Pin TSOP-II

*SL : Low power with self refresh

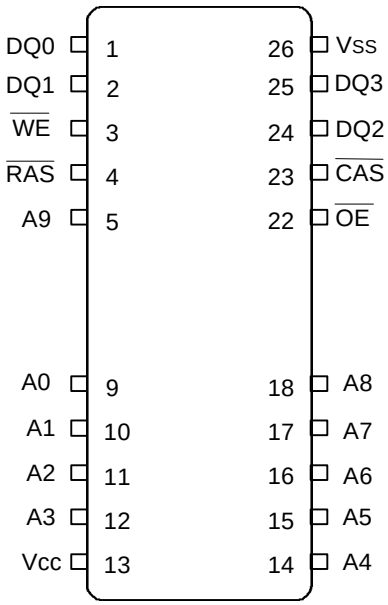
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Marking Side)



20/26 Pin Plastic SOJ (300mil)



20/26 Pin Plastic TSOP- II (300mil)

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A9	Address Input
DQ0~DQ3	Data In/Out
Vcc	Power (5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	0.9	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

Note : All voltages are referenced to V_{SS}.

DC OPERATING CHARACTERISTICS

Symbol	Parameter	Test condition	Min	Max	Unit
I_{LI}	Input Leakage Current (Any input)	$V_{SS} \le V_{IN} \le V_{CC}$ + 1.0 All other pins not under test = V_{SS}	-10	10	µA
I_{LO}	Output Leakage Current (Any input)	$V_{SS} \le V_{OUT} \le V_{CC}$ /RAS & /CAS at V_{IH}	-10	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5.0mA	2.4	-	V

DC CHARACTERISTICS

(T_A = 0°C to 70°C , V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max.	Unit
I_{CC1}	Operating Current	/RAS, /CAS Cycling t_{RC} = $t_{RC(min)}$	50 60 70	100 90 80	mA
I_{CC2}	TTL Standby Current	/RAS, /CAS ≥ $V_{IH(min)}$ Other inputs ≥ V_{SS}		2	mA
I_{CC3}	/RAS-only Refresh Current	/RAS Cycling,/CAS = V_{IH} t_{RC} = $t_{RC(min)}$	50 60 70	100 90 80	mA
I_{CC4}	Fast Page mode Current	/CAS Cycling, /RAS = V_{IL} t_{HPC} = $t_{HPC(min)}$	50 60 70	70 60 50	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V_{CC} - 0.2V	 SL-part	1 200	mA µA
I_{CC6}	/CAS-before-/RAS Refresh Current	/RAS & /CAS = 0.2V t_{RC} = $t_{RC(min.)}$	50 60 70	100 90 80	mA
I_{CC7}	Battery Back-up Current (SL-part)	tRC=125µs /CAS = CBR cycling or 0.2V /OE & /WE = V_{CC} - 0.2V Address = Vcc-0.2V or 0.2V DQ0~DQ3 = Vcc-0.2, 0.2V or Open		300	µA
I_{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as I_{CC7}		200	µA

Note

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(t_{RC} and t_{PC}).
2. Specified values are obtained with output unloaded.
3. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, address can be changed only once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /CAS=V_{IH} within one cycle time t_{PC}.
4. Only tRAS(max) = 1µs is applied to refresh of battery backup but tRAS(max) = 10µs is to applied to normal functional operation.
5. Icc5(max.), Icc7 and Icc8 are applied to SL-part only.

AC CHARACTERISTICS

(T_A = 0 °C to 70 °C, V_{CC} = 5V ± 10% , V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	50ns		60ns		70ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random read or write cycle time	90	-	110	-	130	-	ns	
t_{RWC}	Read-modify-write cycle time	130	-	155	-	185	-	ns	
t_{PC}	Fast Page mode cycle time	35	-	40	-	45	-	ns	
t_{PRWC}	Fast Page mode read-modify-write cycle time	75	-	80	-	95	-	ns	
t_{RAC}	Access time from /RAS	-	50	-	60	-	70	ns	4,9,10
t_{CAC}	Access time from /CAS	-	15	-	15	-	20	ns	4,9
t_{AA}	Access time from column address	-	25	-	30	-	35	ns	4,10
t_{CPA}	Access time from /CAS precharge	-	30	-	35	-	40	ns	4,15
t_{CLZ}	/CAS to output low impedance	0	-	0	-	0	-	ns	4
t_T	Transition time(rise and fall)	3	50	3	50	3	50	ns	3
t_{RP}	/RAS precharge time	30	-	40	-	50	-	ns	
t_{RAS}	/RAS pulse width	50	10K	60	10K	70	10K	ns	
t_{RASP}	/RAS pulse width(FP mode)	50	200K	60	200K	70	200K	ns	
t_{RSH}	/RAS hold time	15	-	15	-	20	-	ns	
t_{CSH}	/CAS hold time	50	-	60	-	70	-	ns	
t_{CAS}	/CAS pulse width	15	10K	15	10K	20	10K	ns	
t_{RCD}	/RAS to /CAS delay time	15	35	20	45	20	50	ns	9
t_{RAD}	/RAS to column address delay time	10	25	15	30	15	35	ns	10
t_{CRP}	/CAS to /RAS precharge time	5	-	5	-	5	-	ns	15
t_{CP}	/CAS precharge time	10	-	10	-	10	-	ns	17
t_{ASR}	Row address set-up time	0	-	0	-	0	-	ns	
t_{RAH}	Row address hold time	8	-	10	-	10	-	ns	
t_{ASC}	Column address set-up time	0	-	0	-	0	-	ns	14
t_{CAH}	Column address hold time	15	-	15	-	15	-	ns	14
t_{AR}	Column address hold time from /CAS	40	-	50	-	55	-	ns	
t_{RAL}	Column address to /RAS lead time	25	-	30	-	35	-	ns	
t_{RCS}	Read command set-up time	0	-	0	-	0	-	ns	14
t_{RCH}	Read command hold time referenced to /CAS	0	-	0	-	0	-	ns	6,14
t_{RRH}	Read command hold time referenced to /RAS	0	-	0	-	0	-	ns	6
t_{WCH}	Write command hold time	10	-	10	-	15	-	ns	14
t_{WCR}	Write command hold time from /RAS	40	-	45	-	55	-	ns	
t_{WP}	Write command pulse width	10	-	10	-	15	-	ns	
t_{RWL}	Write command to /RAS lead time	15	-	15	-	20	-	ns	

AC CHARACTERISTICS

Continued

Symbol	Parameter	50ns		60ns		70ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tCWL	Write command to /CAS lead time	15	-	15	-	20	-	ns	16
tDS	Data-in set-up time	0	-	0	-	0	-	ns	7
tDH	Data-in hold time	15	-	15	-	15	-	ns	7
tDHR	Data-in hold time Referenced to /RAS	40	-	45	-	55	-	ns	
tREF	Refresh period(1024 cycles)	16	-	16	-	16	-	ms	12
	Refresh period(SL-part)	128	-	128	-	128	-	ms	11
tWCS	Write command set-up time	0	-	0	-	0	-	ns	84
tCWD	/CAS to /WE delay time	35	-	40	-	50	-	ns	8
tRWD	/RAS to /WE delay time	70	-	85	-	100	-	ns	8
tAWD	Column address to /WE delay time	45	-	55	-	65	-	ns	8
tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	5	-	ns	14
tCHR	/CAS hold time(CBR cycle)	10	-	10	-	10	-	ns	15
tRPC	/RAS to /CAS precharge time	5	-	5	-	5	-	ns	14
tCPT	/CAS precharge time(CBR counter test)	20	-	20	-	25	-	ns	17
tROH	/RAS hold time referenced to /OE	10	-	10	-	10	-	ns	
tOEA	/OE access time	-	15	-	15	-	20	ns	
tOED	/OE to data delay	15	-	15	-	20	-	ns	
tOEZ	Output buffer turn-off delay time from /OE	0	15	0	15	0	20	ns	5
tOEH	/OE command hold time	15	-	15	-	20	-	ns	
tCPWD	/WE delay time from /CAS precharge	50	-	55	-	65	-	ns	8
tRHCP	/RAS hold time from /CAS precharge	30	-	35	-	40	-	ns	
tRASS	/RAS pulse width(self refresh)	100	-	100	-	100	-	ns	
tRPS	/RAS Precharge Time (Self refresh)	120	-	130	-	150	-	ns	
tCHS	/CAS Hold Time (Self refresh)	-50	-	-50	-	-50	-	ns	
tWRP	/WE to /RAS Precharge time (CBR cycle)	10	-	10	-	10	-	ns	
tWRH	/WE to /RAS Hold time (CBR cycle)	10	-	10	-	10	-	ns	
tWTS	Write Command Set-up time (Test Mode In)	10	-	10	-	10	-	ns	
tWTH	Write Command Hole time (test Mode In)	10	-	10	-	10	-	ns	

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. If /RAS=Vss during power-up,the HY514400B could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid VIH in other to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.),and are assumed to be 5ns for all inputs.
4. Measured at V_{OH}=2.0V and V_{OL}=0.8V with a load equivalent to 2TTL loads and 100pF.
5. tOFF(max.) and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. t_{CEZ} and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD(min.)}$, $t_{CWD} \geq t_{CWD(min.)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPWD} \geq t_{CPWD(min.)}$, the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the $t_{RCD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA}.
11. tREF(max.)=128ms is applied to SL-parts only.
12. A burst of 1024 CBR refresh cycles must be executed within 16ms (128ms for SL-part) after exiting self refresh.
13. When CAS goes low at the same time, 4bits data are written into the device.
14. These parameters are determined by the earlier falling edge of /CAS.
15. These parameters are determined by the later rising edge of /CAS.
16. tCWL must be satisfied by /CAS for 4bits access cycle.
17. tCP and tCPT are measured when /CAS and is high state.

CAPACITANCE

(T_A = 25°C, V_{CC} = 5V ± 10%, V_{SS} = 0V and f=1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Input Capacitance (A0~A9)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input / Output Capacitance (DQ0~DQ3)	-	7	pF