OCTAL BUFFER/LINE DRIVE; 3-STATE

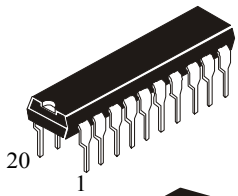
KK74LV240

The KK74LV240 is a low-voltage Si-gate CMOS device and is pin and function compatible with KK74HC/HCT240.

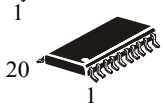
The KK74LV240 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on nOE causes the outputs to assume a high impedance OFF-state.

The KK74LV240 is identical to the KK74LV244 but has inverting outputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 3.6 V
- Low Input Current: 1.0 μA, 0.1 μA at T = 25 °C
- Output Current: 8 mA at V_{CC} = 3.0 V
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC DIP



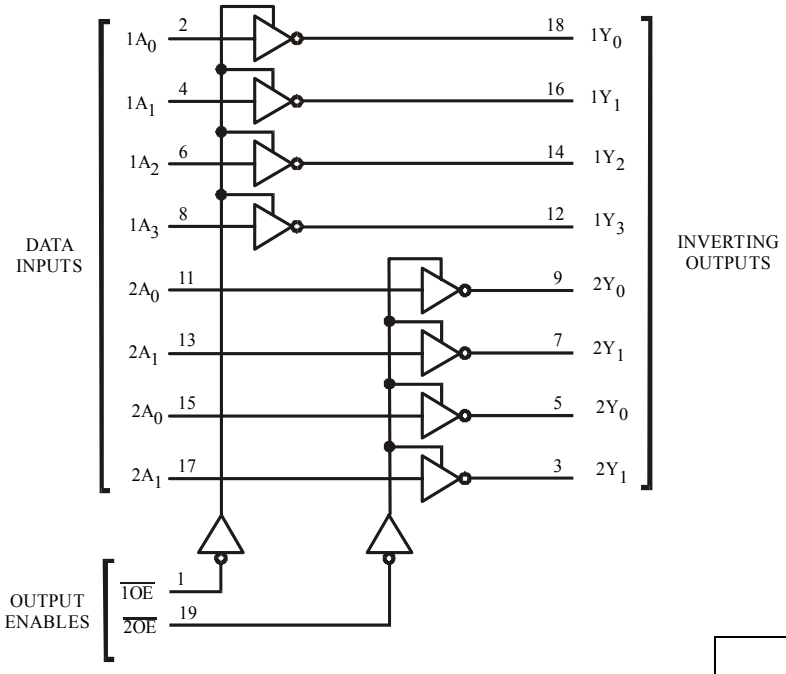
DW SUFFIX
SO

ORDERING INFORMATION

KK74LV240N	Plastic
KK74LV240DW	SOIC

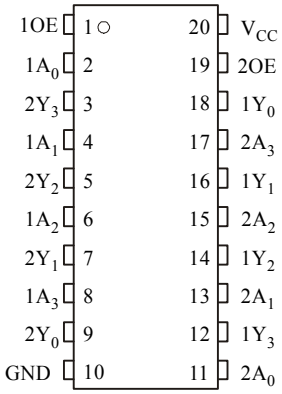
T_A = -40° to 125° C for all packages

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Input		Output
$\overline{nOE}$	**nAn**	**nYn**
L	L	H
L	H	L
H	X	Z

H= high level
L = low level
X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK} *1	DC Input diode current	±20	mA
I_{OK} *2	DC Output diode current	±50	mA
I_O *3	DC Output source or sink current	±35	mA
I_{CC}	DC V_{CC} current	±70	mA
I_{GND}	DC GND current	±70	mA
P_D	Power dissipation per package: *4 Plastic DIP SO	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	3.6	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =1.2 V V_{CC} =2.0 V V_{CC} =3.0 V V_{CC} =3.6 V	0 0 0 0	1000 700 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2 2.0 3.0 3.6	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	V
V_{IL}	LOW level input voltage		1.2 2.0 3.0 3.6	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -50 µA	1.2 2.0 3.0 3.6	1.1 1.92 2.92 3.52	- - - -	1.0 1.9 2.9 3.5	- - - -	1.0 1.9 2.9 3.5	- - - -	V
		$V_I = V_{IH}$ or V_{IL} I_O = -8 mA	3.0	2.48	-	2.34	-	2.20	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 50 µA	1.2 2.0 3.0 3.6	- - - -	0.09 0.09 0.09 0.09	- - - -	0.1 0.1 0.1 0.1	- - - -	0.1 0.1 0.1 0.1	V
		$V_I = V_{IH}$ or V_{IL} I_O = 8 mA	3.0	-	0.33	-	0.4	-	0.5	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	*	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	Three state leakage current	3-state outputs V_I (01,19) = V_{IH} V_O =V_{CC} or 0 V	1.2 *	-	±0.5	-	±5	-	±10	µA
I_{CC}	Supply current	V_I =V_{CC} or 0 V I_O = 0 µA	*	-	8.0	-	80	-	160	µA

* V_{CC} = 3.3 ± 0.3 V

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_r=t_f=6.0 ns)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay , 1An to 1Yn, 2An to 2Yn	V_I = 0 V or V_{CC} Figure 1 and 3	1.2 2.0 *	- - -	100 24 15	- - -	125 30 19	- - -	150 36 23	ns
t_{PHZ} t_{PLZ}	Propagation delay, 1OE to 1Yn, 2OE to 2Yn	V_I = 0 V or V_{CC} Figure 2 and 4	1.2 2.0 *	- - -	140 30 20	- - -	175 35 24	- - -	210 41 28	ns
t_{PZH} t_{PZL}	Propagation delay, 1OE to 1Yn, 2OE to 2Yn	V_I = 0 V or V_{CC} Figure 2 and 4	1.2 2.0 *	- - -	140 32 20	- - -	175 40 25	- - -	210 48 30	ns
t_{THL}, t_{TLH}	Output Transition Time, Any Output	V_I = 0 V or V_{CC} Figure 1 and 3	1.2 2.0 *	- - -	60 16 10	- - -	75 20 13	- - -	90 24 15	ns
C_I	Input capacitance		3.0	-	7.0	-	7.0	-	7.0	pF
C_{PD}	Power dissipation capacitance (per one channel)	V_I = 0 V or V_{CC}		-	50	-	-	-	-	pF

* V_{CC} = 3.3 ± 0.3 V

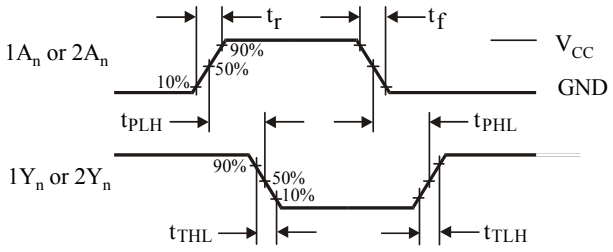


Figure 1. Switching Waveforms

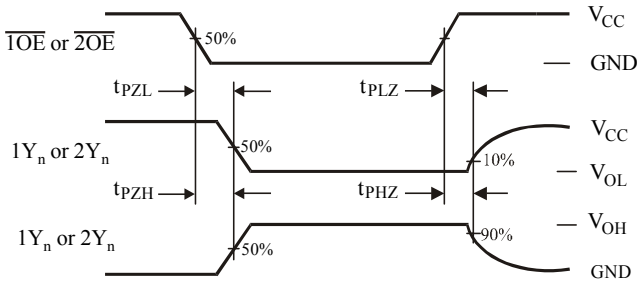
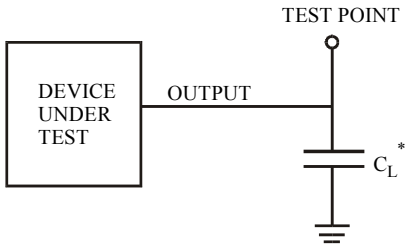
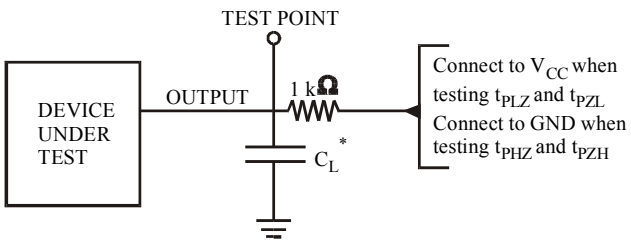


Figure 2. Switching Waveforms



* Includes all probe and jig capacitance

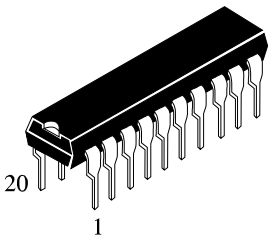
Figure 3. Test Circuit

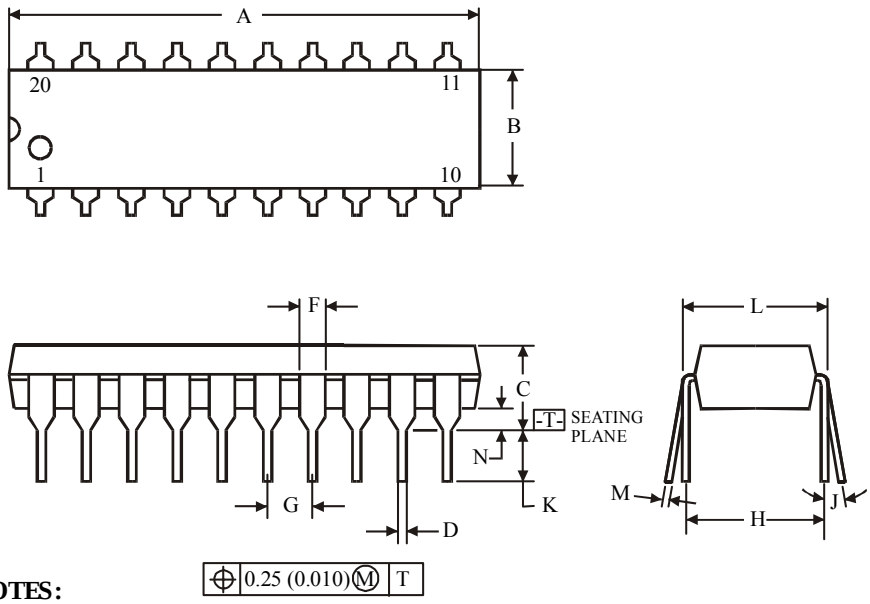


* Includes all probe and jig capacitance

Figure 4. Test Circuit

N SUFFIX PLASTIC DIP
(MS - 001AD)





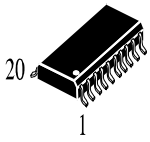
	Dimension, mm	
Symbol	MIN	MAX
A	24.89	26.92
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

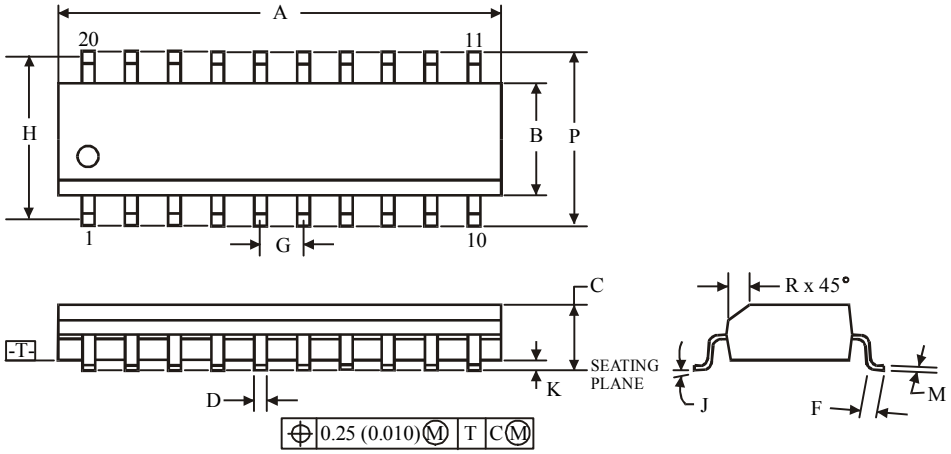
NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 013AC)





	Dimension, mm	
Symbol	MIN	MAX
A	12.6	13
B	7.4	7.6
C	2.35	2.65
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.1	0.3
M	0.23	0.32
P	10	10.65
R	0.25	0.75

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B – 0.25 mm (0.010) per side.