S76121P,S76121S

47A, 30V, 0.021 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative SUNTAC process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76121.

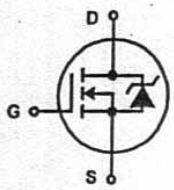
Features

- Logic Level Gate Drive
- 47A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.021\Omega$
- Temperature Compensating PSPICE® Model
- Temperature Compensating SABER© Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature

Ordering Information

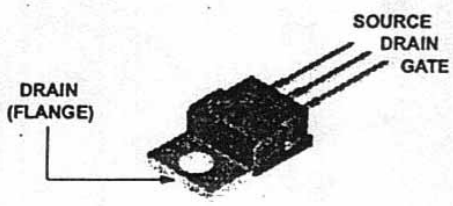
PART NUMBER	PACKAGE	BRAND
76121P	TO-220AB	76121P
76121S	TO-263AB	76121S

Symbol

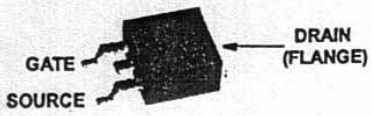


Packaging

TO-220AB



TO-263AB



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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous ($T_C = 25^oC$, V_{GS} = 10V) (Figure 2)	I_D	47	A
Continuous ($T_C = 100^oC$, V_{GS} = 5V)	I_D	25	A
Continuous ($T_C = 100^oC$, V_{GS} = 4.5V) (Figure 2)	I_D	24	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 17,18	
Power Dissipation	P_D	75	W
Derate Above 25^oC		0.6	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-40 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 25V, V_{GS} = 0V, $T_C = 150^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 11)	1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 47A, V_{GS} = 10V (Figures 9, 10)	-	0.015	0.021	Ω
		I_D = 25A, V_{GS} = 5V (Figure 9)	-	0.019	0.028	Ω
		I_D = 24A, V_{GS} = 4.5V (Figure 9)	-	0.021	0.031	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	1.66	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220 and TO-263	-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 4.5V)						
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 24A, R_L = 0.63Ω, V_{GS} = 4.5V, R_{GS} = 10.0Ω (Figures 15, 21, 22)	-	-	265	ns
Turn-On Delay Time	$t_{d(ON)}$		-	15	-	ns
Rise Time	t_r		-	160	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	14	-	ns
Fall Time	t_f		-	31	-	ns
Turn-Off Time	t_{OFF}		-	-	70	ns

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Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 47A, R_L = 0.32Ω, V_{GS} = 10V, R_{GS} = 12.5Ω (Figures 16, 21, 22)		-	-	80	ns
Turn-On Delay Time	$t_{d(ON)}$			-	6	-	ns
Rise Time	t_r			-	47	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	47	-	ns
Fall Time	t_f			-	42	-	ns
Turn-Off Time	t_{OFF}			-	-	135	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 15V, $I_D \cong$ 25A, R_L = 0.6Ω $I_{g(REF)}$ = 1.0mA (Figures 14, 19, 20)	-	24	30	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	13	16	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	1.0	1.2	nC
Gate to Source Gate Charge	Q_{gs}			-	2.50	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	7.80	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 13)		-	850	-	pF
Output Capacitance	C_{OSS}			-	465	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 25A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 25A, dI_{SD}/dt = 100A/μs	-	-	65	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 25A, dI_{SD}/dt = 100A/μs	-	-	100	nC

Typical Performance Curves

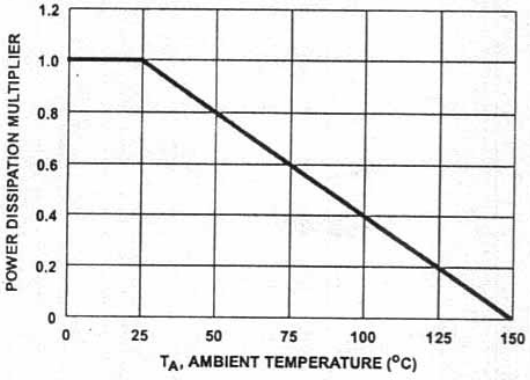

FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

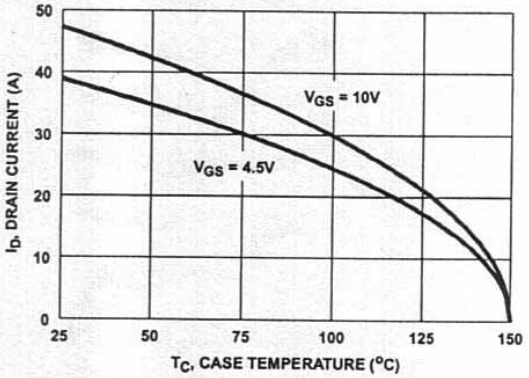

FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

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Typical Performance Curves **(Contiuned)**

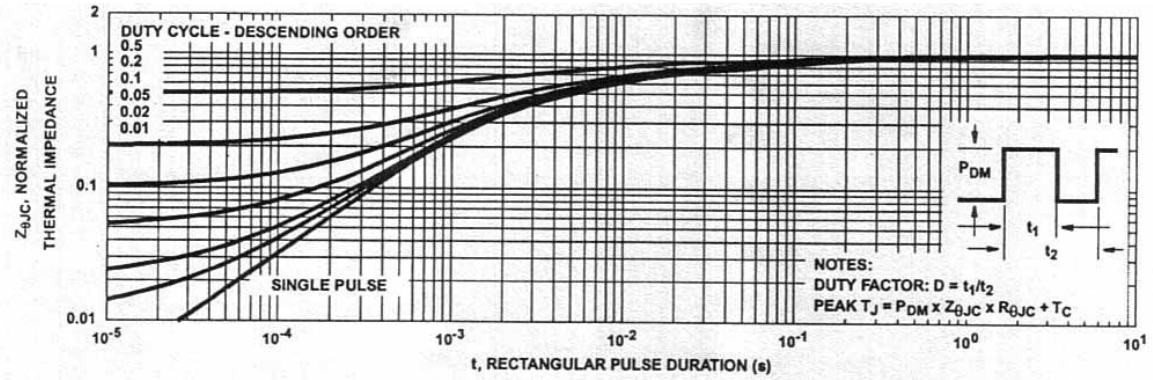


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

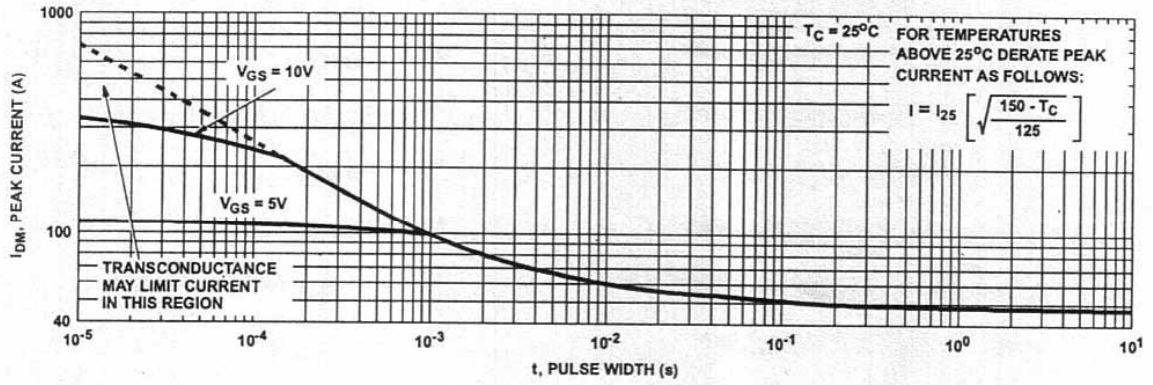


FIGURE 4. PEAK CURRENT CAPABILITY

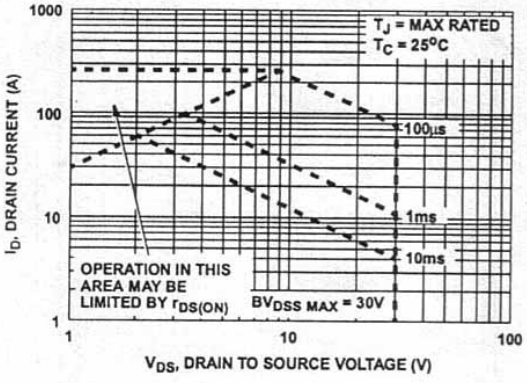
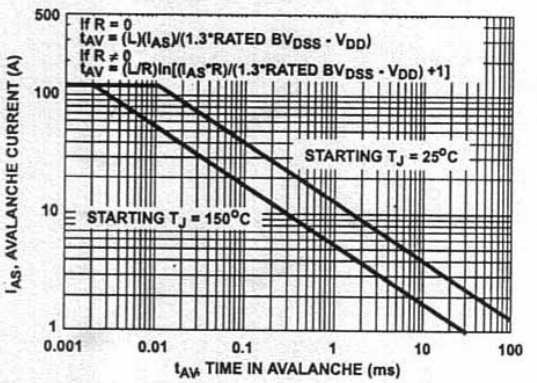


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

S76121P,S76121S

Typical Performance Curves **(Contiuned)**

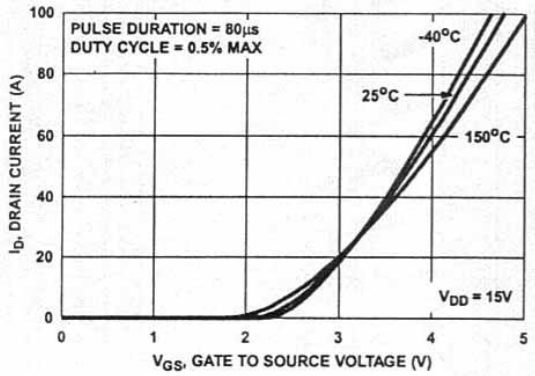


FIGURE 7. TRANSFER CHARACTERISTICS

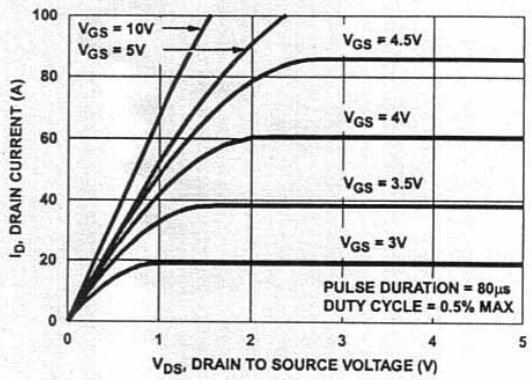


FIGURE 8. SATURATION CHARACTERISTICS

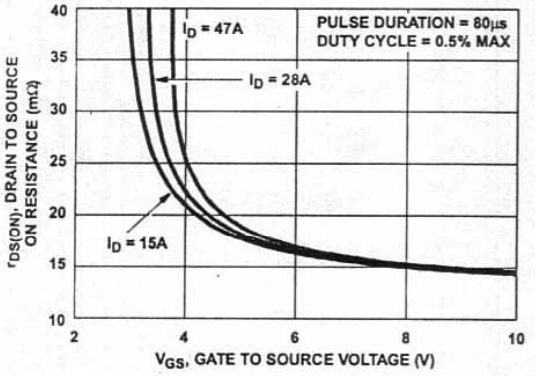


FIGURE 9. SOURCE TO DRAIN ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

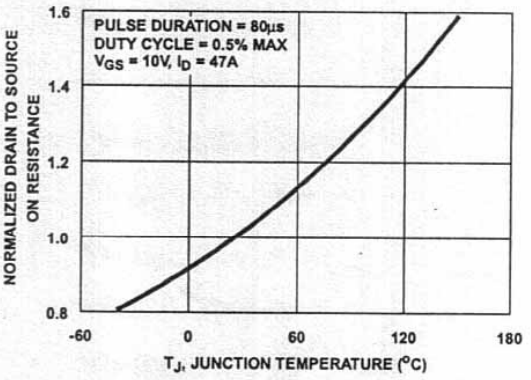


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

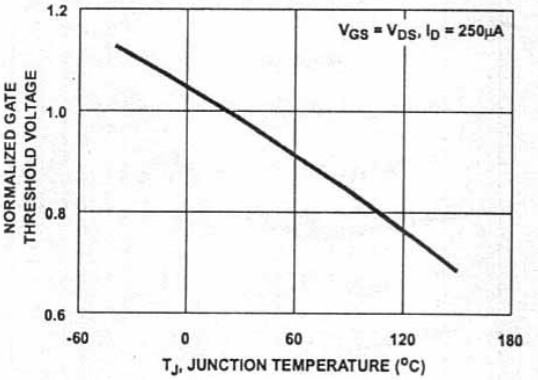


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

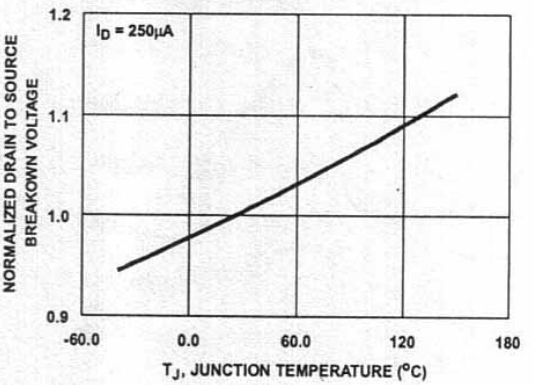


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

S76121P,S76121S

Typical Performance Curves **(Contiuned)**

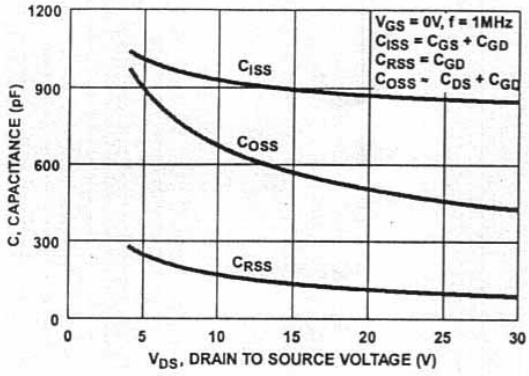
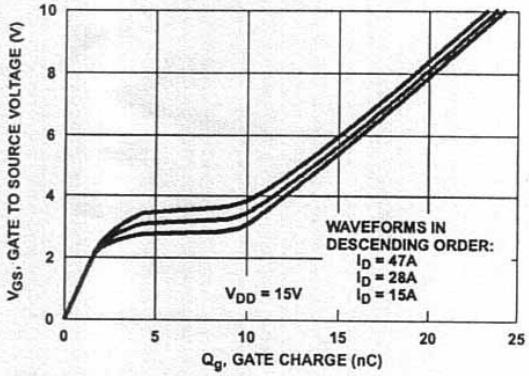


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

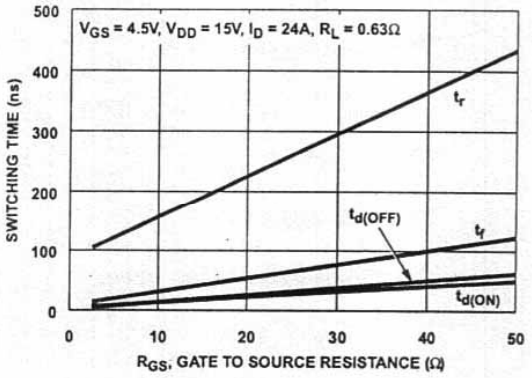


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

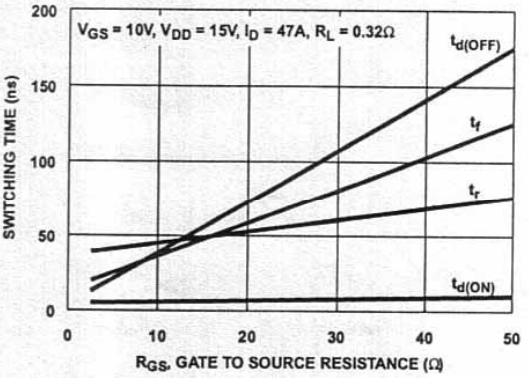


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

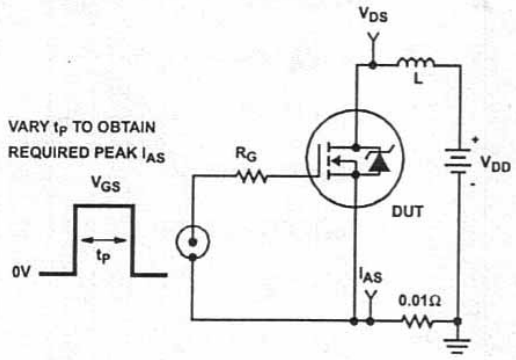


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

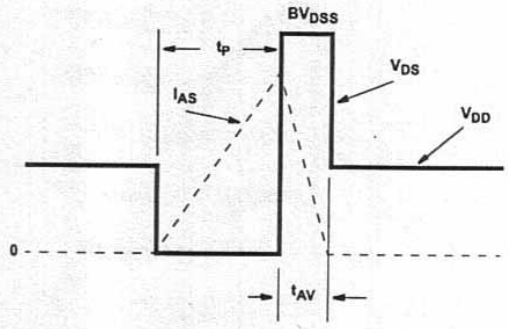


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

S76121P,S76121S

Test Circuits and Waveforms **(Continued)**

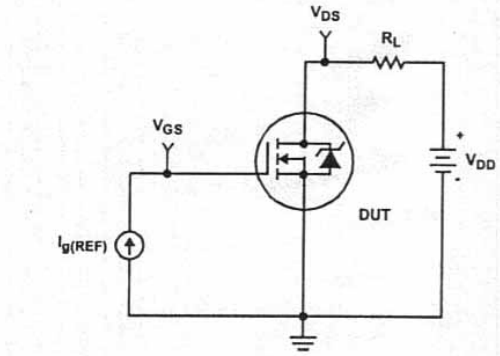


FIGURE 19. GATE CHARGE TEST CIRCUIT

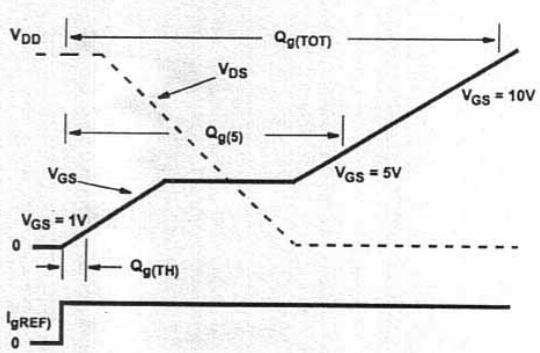


FIGURE 20. GATE CHARGE WAVEFORMS

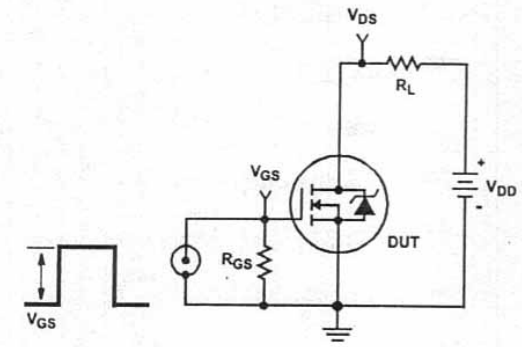


FIGURE 21. SWITCHING TIME TEST CIRCUIT

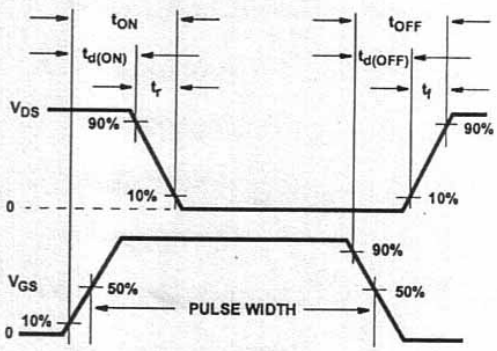


FIGURE 22. SWITCHING TIME WAVEFORM