ELPIDA

PRELIMINARY DATA SHEET

256MB Unbuffered DDR SDRAM DIMM

EBD25EC8AAFA-6B (32M words × 72 bits, 1 Rank)

Description

The EBD25EC8AAFA-6B is 32M words × 72 bits, 1 rank Double Data Rate (DDR) SDRAM unbuffered module, mounting 9 pieces of 256M bits DDR SDRAM sealed in TSOP package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

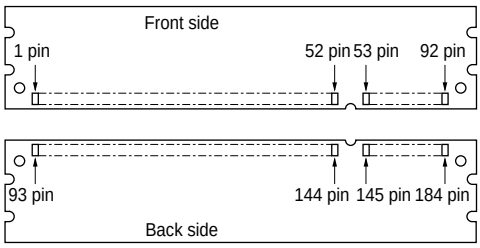
- 184-pin socket type dual in line memory module (DIMM)
  - PCB height: 31.75mm
  - Lead pitch: 1.27mm
- 2.5V power supply
- Data rate: 333Mbps (max.)
- 2.5 V (SSTL_2 compatible) I/O
- Double Data Rate architecture; two data transfers per clock cycle
- Bi-directional, data strobe (DQS) is transmitted /received with data, to be used in capturing data at the receiver
- Data inputs and outputs are synchronized with DQS
- 4 internal banks for concurrent operation (Component)
- DQS is edge aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data referenced to both edges of DQS
- Auto precharge option for each burst access
- Programmable burst length: 2, 4, 8
- Programmable /CAS latency (CL): 2, 2.5
- Refresh cycles: (8192 refresh cycles /64ms)
  - 7.8μs maximum average periodic refresh interval
- 2 variations of refresh
  - Auto refresh
  - Self refresh

Document No. E0391E10 (Ver. 1.0)
Date Published June 2003 (K) Japan
URL: http://www.elpida.com

Ordering Information

Part number	Data rate Mbps (max.)	Component JEDEC speed bin (CL-tRCD-tRP)	Package	Contact pad	Mounted devices
EBD25EC8AAFA-6B	333	DDR333B (2.5-3-3)	184-pin DIMM	Gold	M2S56D30ATP-60

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	47	DQS8	93	VSS	139	VSS
2	DQ0	48	A0	94	DQ4	140	DM8/DQS17
3	VSS	49	CB2	95	DQ5	141	A10
4	DQ1	50	VSS	96	VDD	142	CB6
5	DQS0	51	CB3	97	DM0/DQS9	143	VDD
6	DQ2	52	BA1	98	DQ6	144	CB7
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDD	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	58	VSS	104	VDD	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDD	61	DQ40	107	DM1/DQS10	153	DQ44
16	CK1	62	VDD	108	VDD	154	/RAS
17	/CK1	63	/WE	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDD
19	DQ10	65	/CAS	111	NC	157	/CS0
20	DQ11	66	VSS	112	VDD	158	NC
21	CKE0	67	DQS5	113	NC	159	DM5/DQS14
22	VDD	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDD
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	/CK2	121	DQ22	167	NC
30	VDD	76	CK2	122	A8	168	VDD

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
31	DQ19	77	VDD	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDD
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDD	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	CB4	180	VDD
43	A1	89	VSS	135	CB5	181	SA0
44	CB0	90	NC	136	VDD	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	/CK0	184	VDDSPD

Pin Description

Pin name	Function
A0 to A12	Address input Row address A0 to A12 Column address A0 to A9
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0	Chip select
CKE0	Clock enable
CK0 to CK2	Clock input
/CK0 to /CK2	Differential clock input
DQS0 to DQS8	Input and output data strobe
DM0 to DM8/DQS9 to DQS17	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0 to SA2	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREF	Input reference voltage
VSS	Ground
VDDID	VDD identification flag
NC	No connection

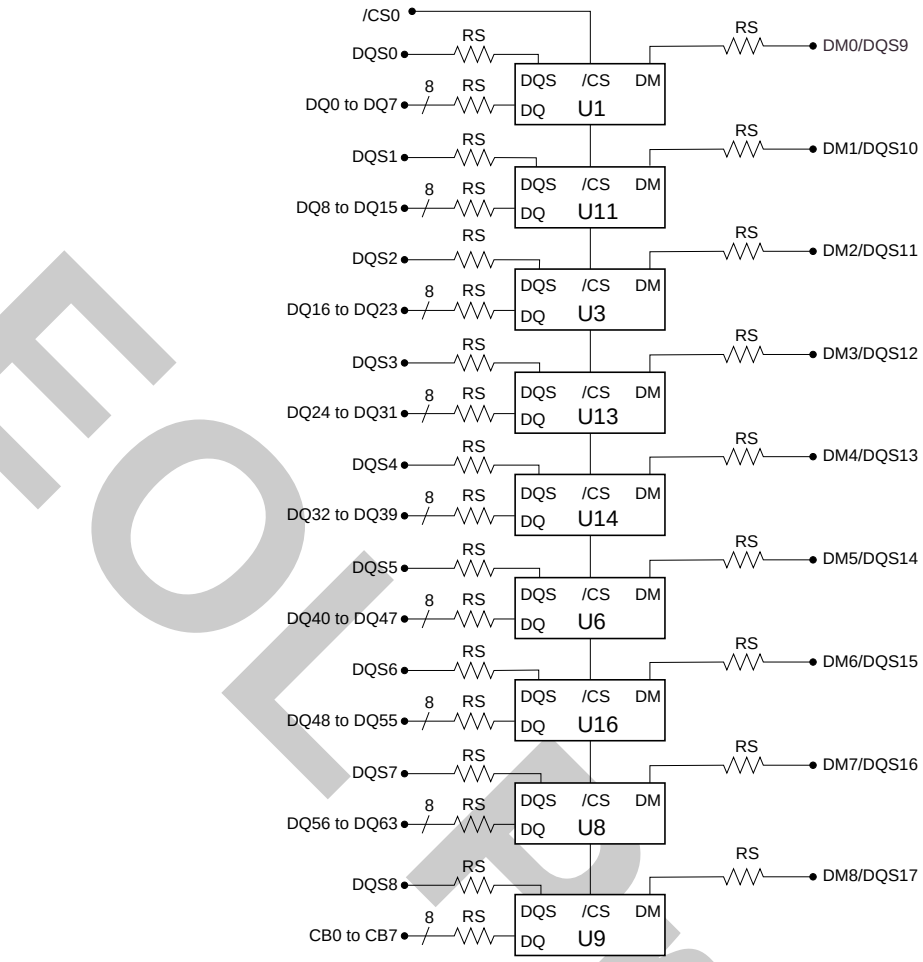
Serial PD Matrix

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80H	128 bytes
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08H	256 bytes
2	Memory type	0	0	0	0	0	1	1	1	07H	DDR SDRAM
3	Number of row address	0	0	0	0	1	1	0	1	0DH	13
4	Number of column address	0	0	0	0	1	0	1	0	0AH	10
5	Number of DIMM ranks	0	0	0	0	0	0	0	1	01H	1
6	Module data width	0	1	0	0	1	0	0	0	48H	72 bits
7	Module data width continuation	0	0	0	0	0	0	0	0	00H	0
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04H	SSTL2
9	DDR SDRAM cycle time, CL = 2.5	0	1	1	0	0	0	0	0	60H	6.0ns[*1]
10	SDRAM access from clock (tAC)	0	1	1	1	0	0	0	0	70H	0.70ns[*1]
11	DIMM configuration type	0	0	0	0	0	0	1	0	02H	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82H	7.6μs
13	Primary SDRAM width	0	0	0	0	1	0	0	0	08H	× 8
14	Error checking SDRAM width	0	0	0	0	1	0	0	0	08H	× 8
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01H	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0EH	2,4,8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04H	4
18	SDRAM device attributes: /CAS latency	0	0	0	0	1	1	0	0	0CH	2, 2.5
19	SDRAM device attributes: /CS latency	0	0	0	0	0	0	0	1	01H	0
20	SDRAM device attributes: /WE latency	0	0	0	0	0	0	1	0	02H	1
21	SDRAM module attributes	0	0	1	0	0	0	0	0	20H	Differential Clock
22	SDRAM device attributes: General	1	1	0	0	0	0	0	0	C0H	VDD ± 0.2V
23	Minimum clock cycle time at CL = 2	0	1	1	1	0	1	0	1	75H	7.5ns[*1]
24	Maximum data access time (tAC) from clock at CL = 2	0	1	1	1	0	0	0	0	70H	0.70ns[*1]
25 to 26		0	0	0	0	0	0	0	0	00H	
27	Minimum row precharge time (tRP)	0	1	0	0	1	0	0	0	48H	18ns
28	Minimum row active to row active delay (tRRD)	0	0	1	1	0	0	0	0	30H	12ns
29	Minimum /RAS to /CAS delay (tRCD)	0	1	0	0	1	0	0	0	48H	18ns
30	Minimum active to precharge time (tRAS)	0	0	1	0	1	0	1	0	2AH	42ns
31	Module rank density	0	1	0	0	0	0	0	0	40H	256M bytes
32	Address and command setup time before clock (tIS)	1	0	0	0	0	0	0	0	80H	0.80ns[*1]
33	Address and command hold time after clock (tIH)	1	0	0	0	0	0	0	0	80H	0.80ns[*1]
34	Data input setup time before clock (tDS)	0	1	0	0	0	1	0	1	45H	0.45ns[*1]

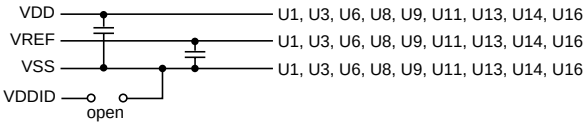
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
35	Data input hold time after clock (tDH)	0	1	0	0	0	1	0	1	45H	0.45ns[*1]
36 to 40	Superset information	0	0	0	0	0	0	0	0	00H	Future use
41	Active command period (tRC)	0	0	1	1	1	1	0	0	3CH	60ns[*1]
42	Auto refresh to active/ Auto refresh command cycle (tRFC)	0	1	0	0	1	0	0	0	48H	72ns[*1]
43	SDRAM tCK cycle max. (tCK max.)	0	0	1	1	1	1	0	0	3CH	15ns[*1]
44	Dout to DQS skew	0	0	1	0	1	1	0	1	2DH	0.45ns[*1]
45	Data hold skew (tQHS)	0	1	0	1	0	1	0	1	55H	0.55ns[*1]
46 to 61	Superset information	0	0	0	0	0	0	0	0	00H	Future use
62	SPD Revision	0	0	0	0	0	0	0	0	00H	
63	Checksum for bytes 0 to 62	0	0	1	1	0	1	0	0	34H	
64 to 65	Manufacturer's JEDEC ID code	0	1	1	1	1	1	1	1	7FH	Continuation code
66	Manufacturer's JEDEC ID code	1	1	1	1	1	1	1	0	FEH	Elpida Memory
67 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	(ASCII-8bit code)
73	Module part number	0	1	0	0	0	1	0	1	45H	E
74	Module part number	0	1	0	0	0	0	1	0	42H	B
75	Module part number	0	1	0	0	0	1	0	0	44H	D
76	Module part number	0	0	1	1	0	0	1	0	32H	2
77	Module part number	0	0	1	1	0	1	0	1	35H	5
78	Module part number	0	1	0	0	0	1	0	1	45H	E
79	Module part number	0	1	0	0	0	0	1	1	43H	C
80	Module part number	0	0	1	1	1	0	0	0	38H	8
81	Module part number	0	1	0	0	0	0	0	1	41H	A
82	Module part number	0	1	0	0	0	0	0	1	41H	A
83	Module part number	0	1	0	0	0	1	1	0	46H	F
84	Module part number	0	1	0	0	0	0	0	1	41H	A
85	Module part number	0	0	1	0	1	1	0	1	2DH	—
86	Module part number	0	0	1	1	0	1	1	0	36H	6
87	Module part number	0	1	0	0	0	0	1	0	42H	B
88 to 90	Module part number	0	0	1	0	0	0	0	0	20H	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30H	Initial
92	Revision code	0	0	1	0	0	0	0	0	20H	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (HEX)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (HEX)
95 to 98	Module serial number										
99 to 127	Manufacture specific data										

Note: 1.These specifications are defined based on component specification, not module.

Block Diagram



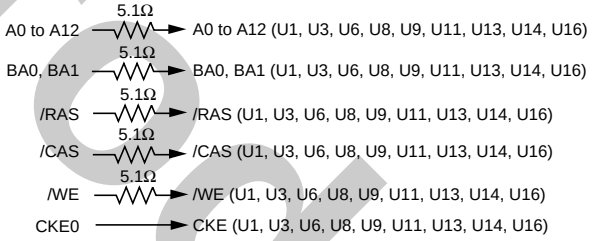
* U1, U3, U6, U8, U9, U11, U13, U14, U16 : 256M bits DDR SDRAM
U20: 2k bits EEPROM
RS: 22Ω

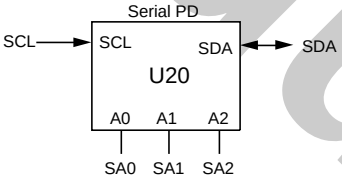


Clock wiring

Clock input	DDR SDRAMS
CK0, /CK0	3DRAM loads
CK1, /CK1	3DRAM loads
CK2, /CK2	3DRAM loads

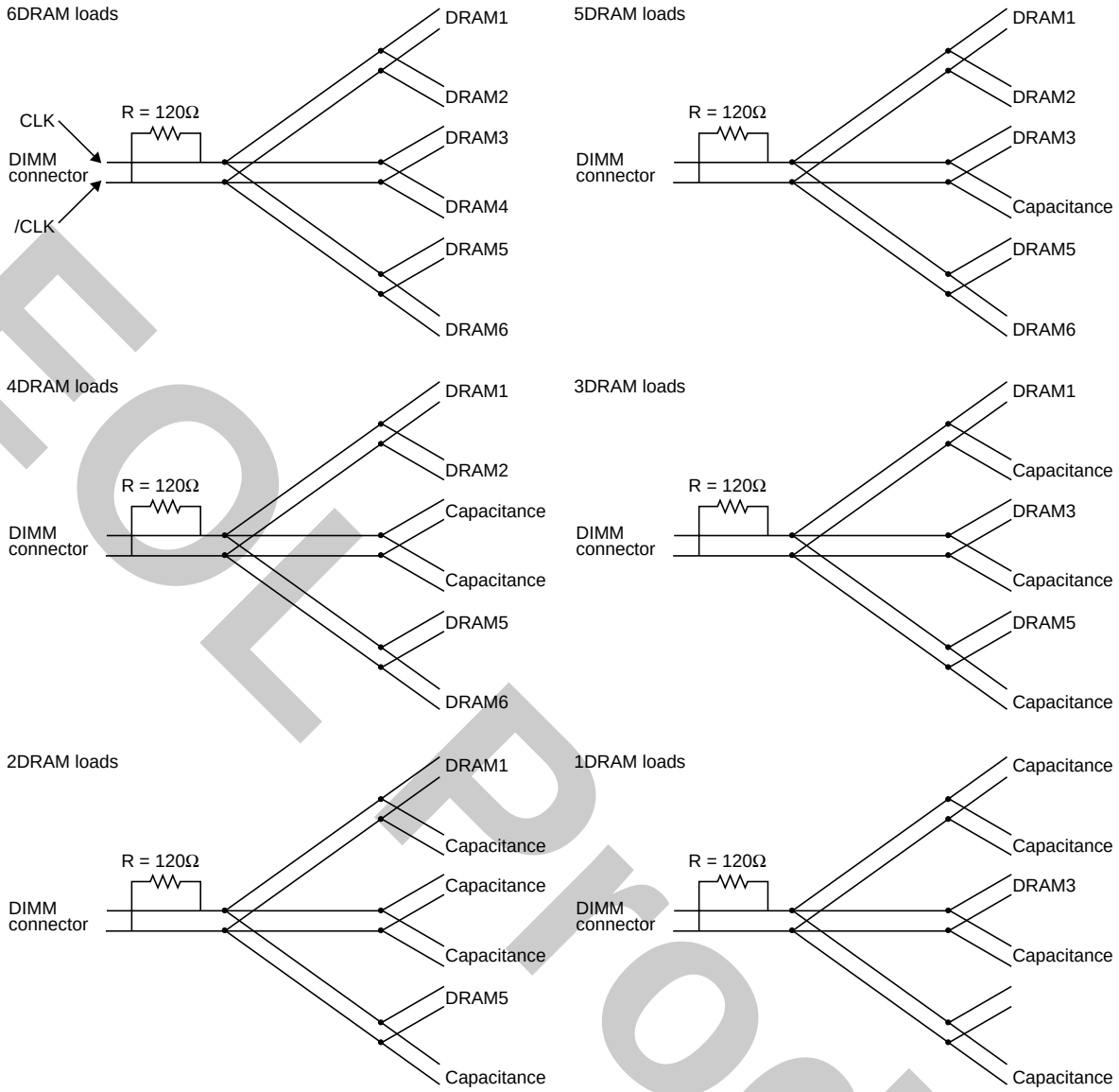
Note: Wire per Clock loading table/Wiring diagrams.





Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

Logical Clock Net Structure



Electrical Specifications

- All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to +3.6	V	
Supply voltage relative to VSS	VDD	–0.5 to +3.6	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	9	W	
Operating ambient temperature	TA	0 to +70	°C	1
Storage temperature	Tstg	–40 to +100	°C	

Notes: 1. DDR SDRAM component specification.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Operating Conditions (TA = 0 to +70°C) (DDR SDRAM Component Specification)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	VDD,VDDQ	2.3	2.5	2.7	V	1
	VSS	0	0	0	V	
Input reference voltage	VREF	0.49 × VDDQ	0.50 × VDDQ	0.51 × VDDQ	V	
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	
Input high voltage	VIH (DC)	VREF + 0.15	—	VDDQ + 0.3	V	2
Input low voltage	VIL (DC)	–0.3	—	VREF – 0.15	V	3
Input voltage level, CK and /CK inputs	VIN (DC)	–0.3	—	VDDQ + 0.3	V	4
Input differential cross point voltage, CK and /CK inputs	VIX (DC)	0.5 × VDDQ – 0.2V	0.5 × VDDQ	0.5 × VDDQ + 0.2V	V	
Input differential voltage, CK and /CK inputs	VID (DC)	0.36	—	VDDQ + 0.6	V	5, 6

Notes: 1. VDDQ must be lower than or equal to VDD.
2. VIH is allowed to exceed VDD up to 3.6V for the period shorter than or equal to 5ns.
3. VIL is allowed to outreach below VSS down to –1.0V for the period shorter than or equal to 5ns.
4. VIN (DC) specifies the allowable DC execution of each differential input.
5. VID (DC) specifies the input differential voltage required for switching.
6. VIH (CK) min assumed over VREF + 0.18V, VIL (CK) max assumed under VREF – 0.18V if measurement.

DC Characteristics 1 (TA = 0 to +70°C, VDD = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current (ACTV-PRE)	IDD0		900	mA	CKE ≥ VIH, tRC = tRC (min.)	1, 2, 9
Operating current (ACTV-READ-PRE)	IDD1		1080	mA	CKE ≥ VIH, BL = 4, CL = 2.5, tRC = tRC (min.)	1, 2, 5
Idle power down standby current	IDD2P		90	mA	CKE ≤ VIL	4
Floating idle Standby current	IDD2F		315	mA	CKE ≥ VIH, /CS ≥VIH DQ, DQS, DM = VREF	4, 5
Active power down standby current	IDD3P		180	mA	CKE ≤ VIL	3
Active standby current	IDD3N		495	mA	CKE ≥ VIH, /CS ≥ VIH tRAS = tRAS (max.)	3, 5, 6
Operating current (Burst read operation)	IDD4R		1710	mA	CKE ≥ VIH, BL = 2, CL = 2.5	1, 2, 5, 6
Operating current (Burst write operation)	IDD4W		1710	mA	CKE ≥ VIH, BL = 2, CL = 2.5	1, 2, 5, 6
Auto refresh current	IDD5		1350	mA	tRFC = tRFC (min.), Input ≤ VIL or ≥ VIH	
Self refresh current	IDD6		27	mA	Input ≥ VDD – 0.2 V Input ≤ 0.2 V	
Operating current (4 banks interleaving)	IDD7A		2610	mA	BL = 4	5, 6, 7

Notes. 1. These IDD data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. Data/Data mask transition twice per one cycle.
7. 4 banks active. Only one bank is running at tRC = tRC (min.)
8. The IDD data on this table are measured with regard to tCK = tCK (min.) in general.
9. Command/Address transition once per one every two clock cycles.

DC Characteristics 2 (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–18	18	µA	VDD ≥ VIN ≥ VSS	
Output leakage current	ILO	–5	5	µA	VDD ≥ VOUT ≥ VSS	
Output high current	IOH	–16.8	—	mA	VOUT = VTT + 0.84V	1
Output low current	IOL	16.8	—	mA	VOUT = VTT – 0.84V	1

Note: 1. DDR SDRAM component specification.

Pin Capacitance (TA = 25°C, VDD = 2.5V ± 0.2V)

Parameter	Symbol	Pins	max.	Unit	Notes
Input capacitance	CI1	Address, /RAS, /CAS, /WE, /CS, CKE	80	pF	
Input capacitance	CI2	CK, /CK	60	pF	
Data and DQS input/output capacitance	CO	DQ, CB, DQ	15	pF	

AC Characteristics (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS = 0V)

(DDR SDRAM Componen Specification)

Parameter	Symbol	min.	max	Unit	Notes
Clock cycle time (CL = 2)	tCK	7.5	15	ns	
(CL = 2.5)	tCK	6	15	ns	
CK high-level width	tCH	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	tCK	
CK half period	tHP	min (tCH, tCL)	—	tCK	
DQ output access time from CK, /CK	tAC	–0.70	0.70	ns	
DQS output access time from CK, /CK	tDQSCK	–0.60	0.60	ns	
DQS to DQ skew	tDQSQ	—	0.45	ns	
DQ/DQS output hold time from DQS	tQH	tHP – 0.55	—	ns	
Data-out high-impedance time from CK, /CK	tHZ	–0.70	0.70	ns	1
Data-out low-impedance time from CK, /CK	tLZ	–0.70	0.70	ns	1
Read preamble	tRPRE	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	tCK	
DQ and DM input setup time	tDS	0.45	—	ns	
DQ and DM input hold time	tDH	0.45	—	ns	
DQ and DM input pulse width	tDIPW	1.75	—	ns	
Write preamble setup time	tWPRES	0	—	ns	3
Write preamble	tWPRE	0.25	—	tCK	
Write postamble	tWPST	0.4	0.6	tCK	2
Write command to first DQS latching transition	tDQSS	0.75	1.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	—	tCK	
DQS falling edge hold time from CK	tDSH	0.2	—	tCK	
DQS input high pulse width	tDQSH	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	tCK	
Address and control input setup time	tIS	0.8	—	ns	6
Address and control input hold time	tIH	0.8	—	ns	6
Mode register set command cycle time	tMRD	12	—	ns	
Active to Precharge command period	tRAS	42	120000	ns	
Active to Active/Auto refresh command period	tRC	60	—	ns	
Auto refresh to Active/Auto refresh command period	tRFC	72	—	ns	
Active to Read/Write delay	tRCD	18	—	ns	
Precharge to active command period	tRP	18	—	ns	

Parameter	Symbol	min.	max	Unit	Notes
Active to active command period	tRRD	12	—	ns	
Write recovery time	tWR	15	—	ns	
Auto precharge write recovery and precharge time	tDAL	35	—	ns	
Internal write to Read command delay	tWTR	1	—	tCK	
Exit self refresh to non-read command	tXSNR	75	—	ns	
Exit self refresh to read command	tXSRD	200	—	tCK	
Exit power down to any non-read command	tXPNR	1	—	tCK	
Exit precharge power down to read command	tXPRD	1	—	tCK	5
Average periodic refresh interval	tREF	—	7.8	µs	4

Notes: 1 tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).

2. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
3. The specific requirement is that DQS be valid (High, Low, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic Low. If a previous write was in progress, DQS could be High, Low, or transitioning from High to Low at this time, depending on tDQSS.
4. A maximum of eight auto refresh commands can be posted to any given DDR SDRAM device.
5. tXPRD should be 200 tCK in the condition of the unstable CK operation during the power down mode.
6. For command/address and CK and /CK slew rate ≥ 1.0V/ns

Pin Functions

CK, /CK (input pin)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CK and the /CK.

/CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins)

Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY9) is loaded via the A0 to the A9 at the cross point of the CK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = high when a precharge command is issued, all banks are precharged. If A10 = low when a precharge command is issued, only the bank that is selected by BA1, BA0 is precharged. If A10 = high when read or write command, auto-precharge function is enabled. While A10 = low, auto-precharge function is disabled.

BA0, BA1 (input pin)

BA0, BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven low and exited when it resumes to high.

The CKE level must be kept for 1 CK cycle at least, that is, if CKE changes at the cross point of the CK rising edge and the VREF level with proper setup time tIS, at the next CK rising edge CKE level must be kept with proper hold time tIH.

DQ, CB (input and output pins)

Data are input to and output from these pins.

DQS (input and output pin)

DQS provide the read data strobes (as output) and the write data strobes (as input).

DM (input pins): DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and VREF

VDD (power supply pins)
2.5V is applied. (VDD is for the internal circuit.)

VDDSPD (power supply pin)
2.5V is applied (For serial EEPROM).

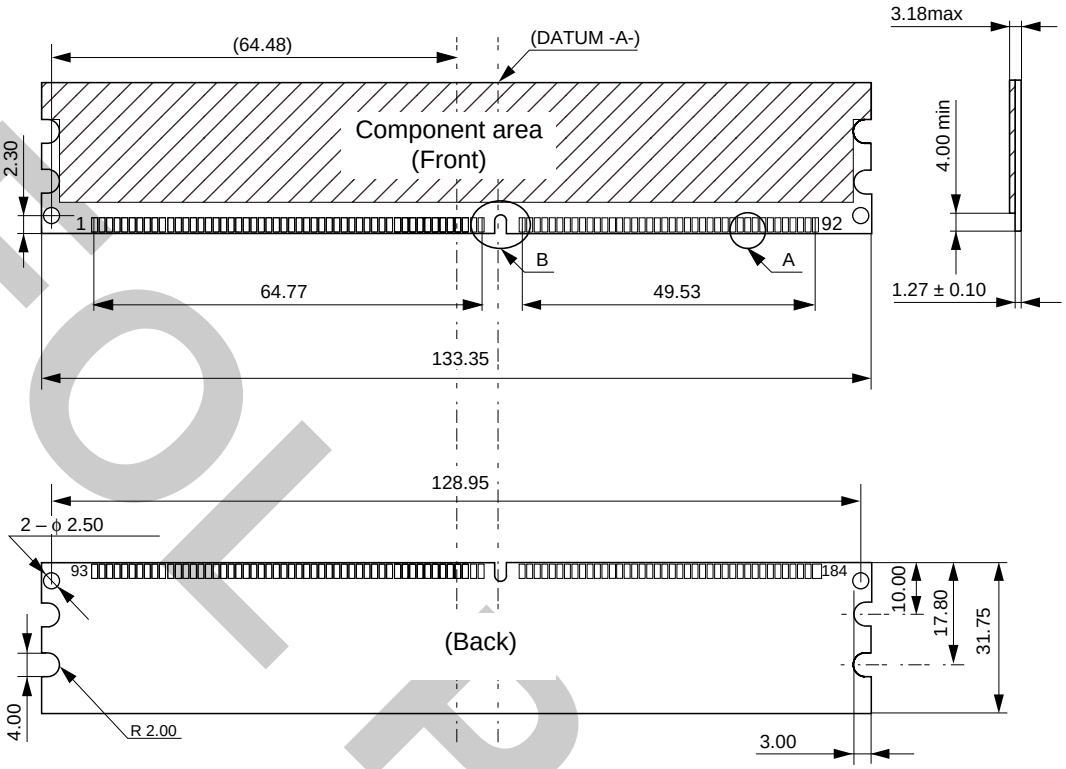
VSS (power supply pin)
Ground is connected.

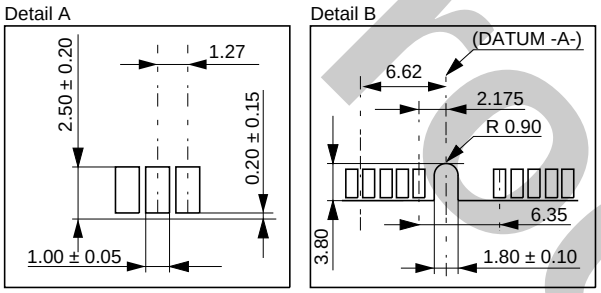
Detailed Operation Part and Timing Waveforms

Refer to M2S56D20/30/40ATP datasheet.

Physical Outline

Unit: mm





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CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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