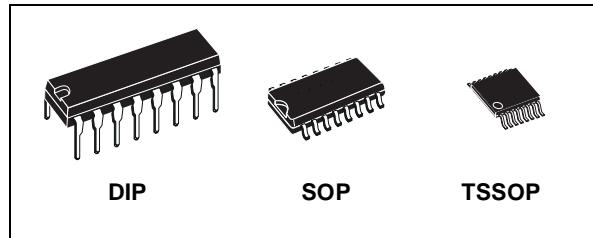


4 WORD x 4 BIT REGISTER FILE (3 STATE)

- HIGH SPEED :
 $t_{PD} = 22 \text{ ns (TYP.)}$ at $V_{CC} = 6V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}(\text{MAX.})$ at $T_A=25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28 \% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OHI}| = I_{OL} = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH
74 SERIES 670



ORDER CODES

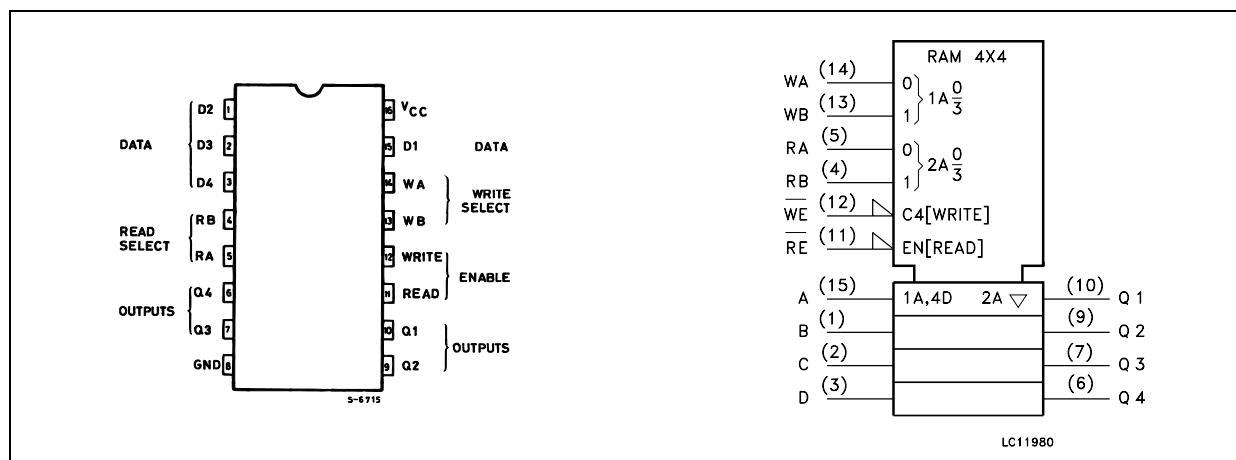
PACKAGE	TUBE	T & R
DIP	M74HC670B1R	
SOP	M74HC670M1R	M74HC670RM13TR
TSSOP		M74HC670TTR

DESCRIPTION

The M74HC670 is an high speed CMOS 4-WORD x 4 BIT REGISTER FILE (3 STATE) fabricated with silicon gate C²MOS technology. The M74HC670 is 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The

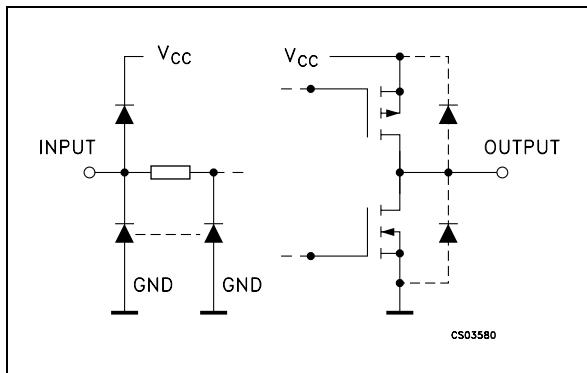
3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



M74HC670

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
5, 4	RA, RB	Read Address Inputs
10, 9, 7, 6	Q1 to Q4	Data Outputs
11	\overline{RE}	3 - State Output Read Enable Input
12	\overline{WE}	Write Enable Input (Active LOW)
14, 13	WA, WB	Write Address Inputs
15, 1, 2, 3	D1 to D4	Data Inputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

WRITE FUNCTION TABLE

WRITE INPUTS			WORDS			
WB	WA	\overline{WE}	0	1	2	3
L	L	L	Q = D	Q0	Q0	Q0
L	H	L	Q0	Q = D	Q0	Q0
H	L	L	Q0	Q0	Q = D	Q0
H	H	L	Q0	Q0	Q0	Q = D
X	X	H	Q0	Q0	Q0	Q0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
RB	RA	\overline{RE}	Q0	Q1	Q2	Q3
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

X : Don't Care

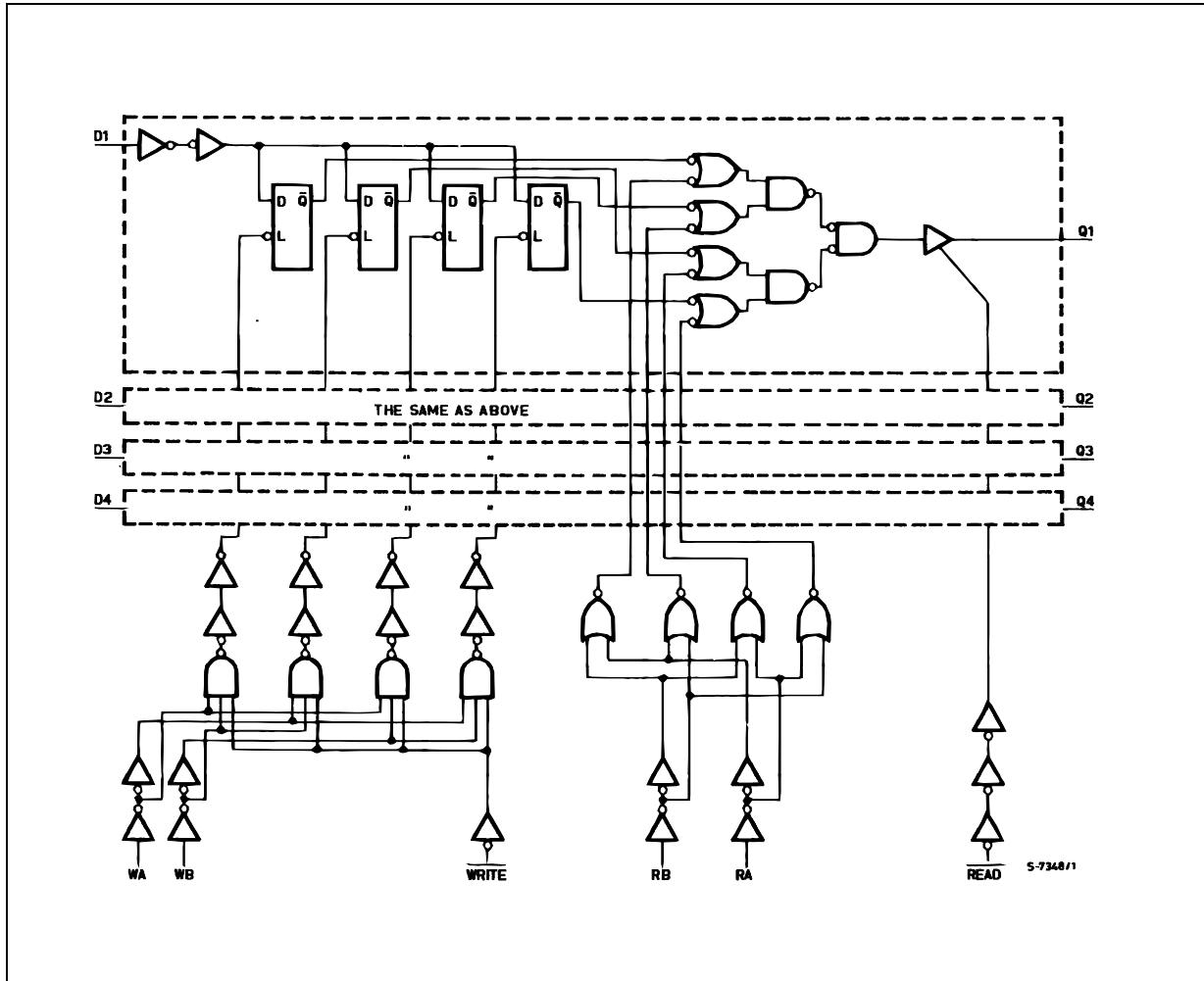
Z : High Impedance

(Q = D) = The four select internal flip-flop outputs will assume the states applied to the four external data inputs.

Q0 = The level of Q before the indicated input conditions were established.

W0B1 = The first bit of word 0, etc.

LOGIC DIAGRAM



This logic diagram has not been used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Value		Unit
V_{CC}	Supply Voltage			2 to 6		V
V_I	Input Voltage			0 to V_{CC}		V
V_O	Output Voltage			0 to V_{CC}		V
T_{op}	Operating Temperature			-55 to 125		°C
t_r, t_f	Input Rise and Fall Time		$V_{CC} = 2.0V$	0 to 1000		ns
			$V_{CC} = 4.5V$	0 to 500		ns
			$V_{CC} = 6.0V$	0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ C$			$-40 \text{ to } 85^\circ C$		$-55 \text{ to } 125^\circ C$		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	$I_O = -20 \mu A$	1.9	2.0		1.9		1.9		V
		4.5	$I_O = -20 \mu A$	4.4	4.5		4.4		4.4		
		6.0	$I_O = -20 \mu A$	5.9	6.0		5.9		5.9		
		4.5	$I_O = -4.0 mA$	4.18	4.31		4.13		4.10		
		6.0	$I_O = -5.2 mA$	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	V
		4.5	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	
		6.0	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	
		4.5	$I_O = 4.0 mA$		0.17	0.26		0.33		0.40	
		6.0	$I_O = 5.2 mA$		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC} \text{ or GND}$			± 0.1		± 1		± 1	μA
I_{OZ}	High Impedance Output Leakage Current	6.0	$V_I = V_{IH} \text{ or } V_{IL}$ $V_O = V_{CC} \text{ or GND}$			± 0.5		± 5		± 5	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC} \text{ or GND}$			4		40		80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		
$t_{TLH} t_{THL}$	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{PLH} t_{PHL}$	Propagation Delay Time (RA, RB - Qn)	2.0			96	185		230		280	ns
		4.5			24	37		46		56	
		6.0			20	31		39		48	
$t_{PLH} t_{PHL}$	Propagation Delay Time (WE - Qn)	2.0			108	220		275		330	ns
		4.5			27	44		55		66	
		6.0			23	37		47		56	
$t_{PLH} t_{PHL}$	Propagation Delay Time (Dn - Qn)	2.0			104	185		230		280	ns
		4.5			26	37		46		56	
		6.0			22	31		39		48	
$t_{PZL} t_{PZH}$	High Impedance Output Enable Time	2.0	$R_L = 1 \text{ k}\Omega$		42	110		140		165	ns
		4.5			13	22		28		33	
		6.0			11	19		24		28	
$t_{PLZ} t_{PHZ}$	High Impedance Output Disable Time	2.0	$R_L = 1 \text{ k}\Omega$		25	95		120		145	ns
		4.5			13	19		24		29	
		6.0			11	16		20		25	
$t_{W(L)}$	Minimum Pulse Width (WE)	2.0			16	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
t_s	Minimum Set-up Time (Dn - WE) (WA, WB - WE)	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			3	9		11		13	
t_h	Minimum Hold Time (Dn - WE)	2.0			0		0	0		0	ns
		4.5			0		0	0		0	
		6.0			0		0	0		0	
t_h	Minimum Hold Time (WA, WB - WE)	2.0			5		5		5		ns
		4.5			5		5		5		
		6.0			5		5		5		
t_{latch}	Minimum Latch Time (WE - RA, RB)	2.0			5		5		5		ns
		4.5			5		5		5		
		6.0			5		5		5		

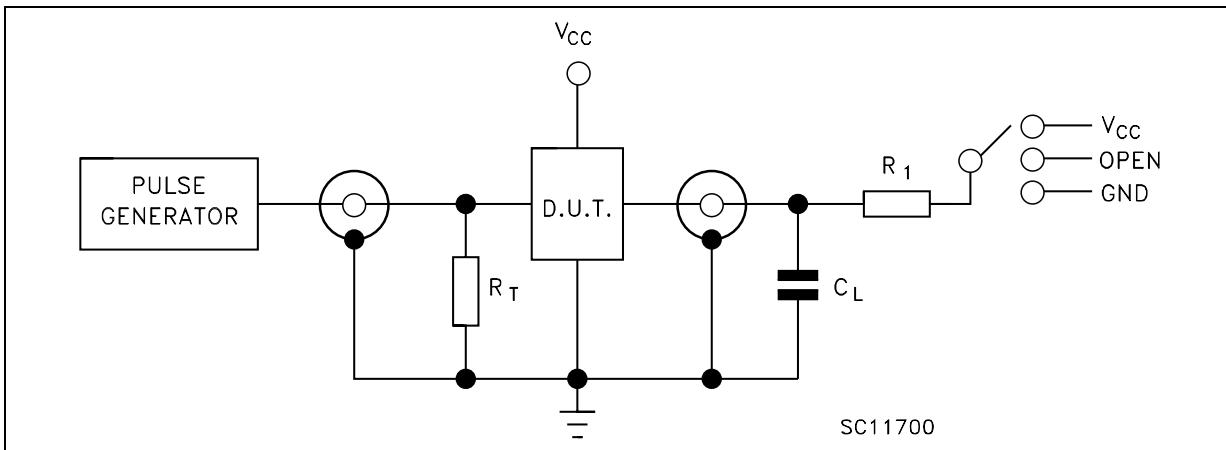
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			96						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

M74HC670

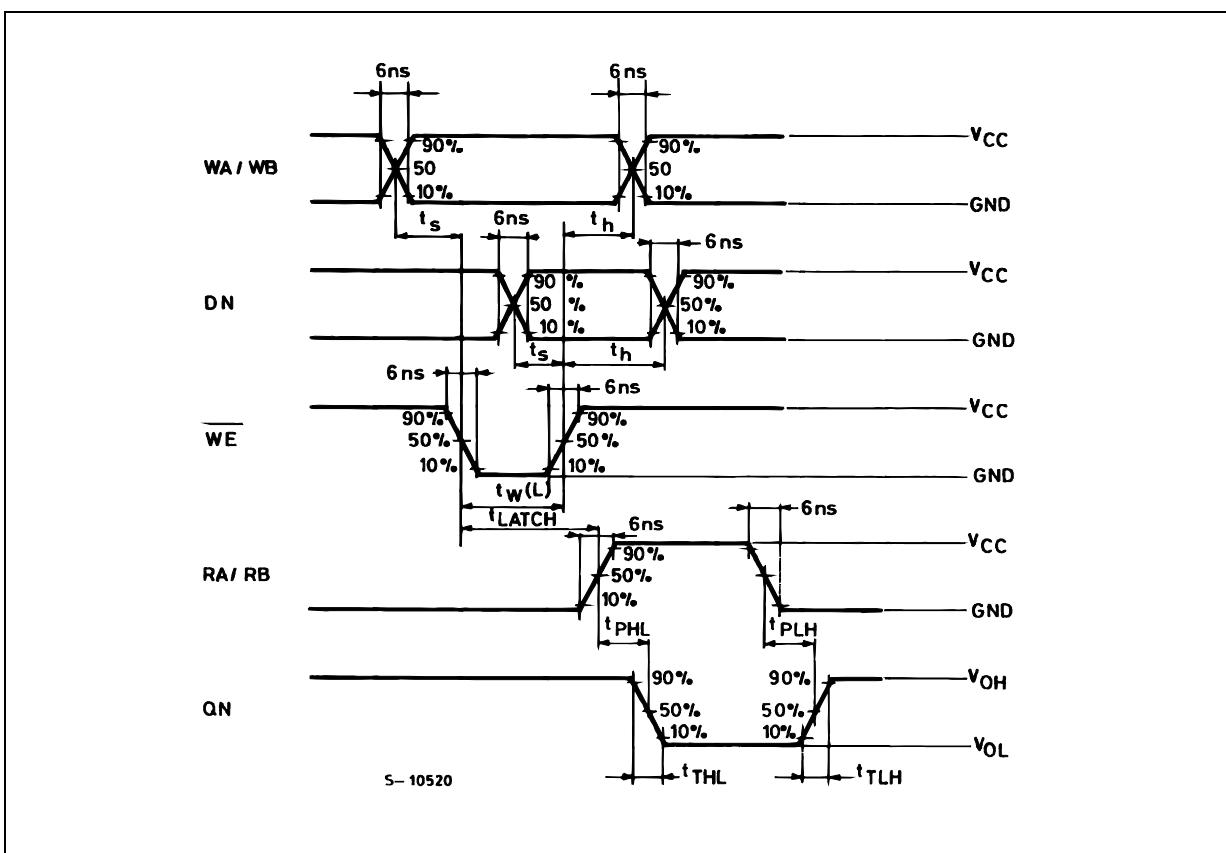
TEST CIRCUIT



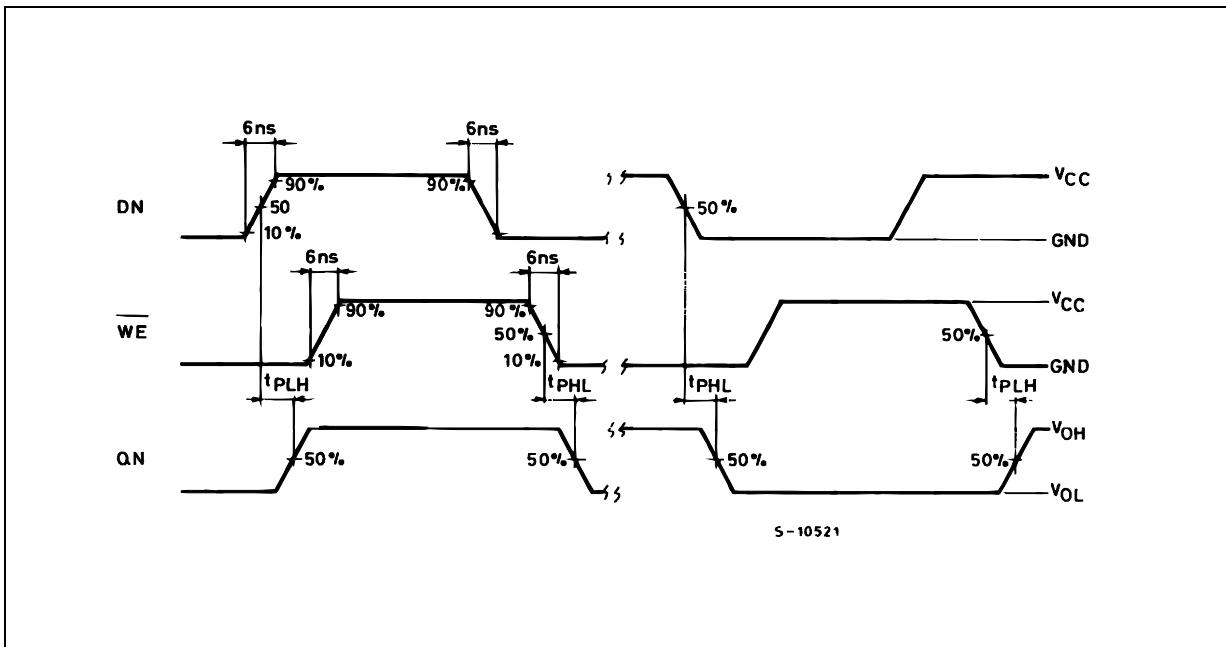
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

$C_L = 50\text{pF}/150\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_1 = 1\text{k}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

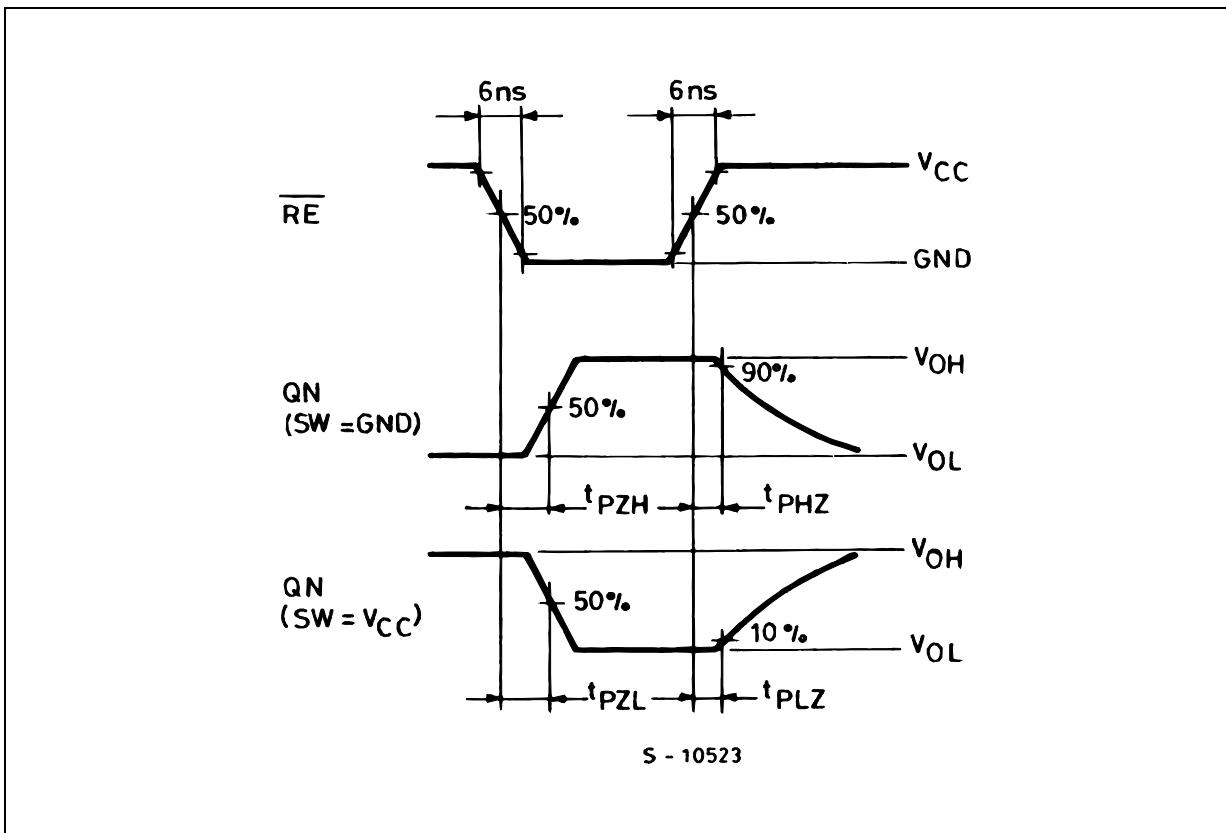
WAVEFORM 1 : PROPAGATION DELAY, MINIMUM PULSE WIDTH, SETUP AND HOLD TIME, MINIMUM LATCH TIME ($f=1\text{MHz}$; 50% duty cycle)



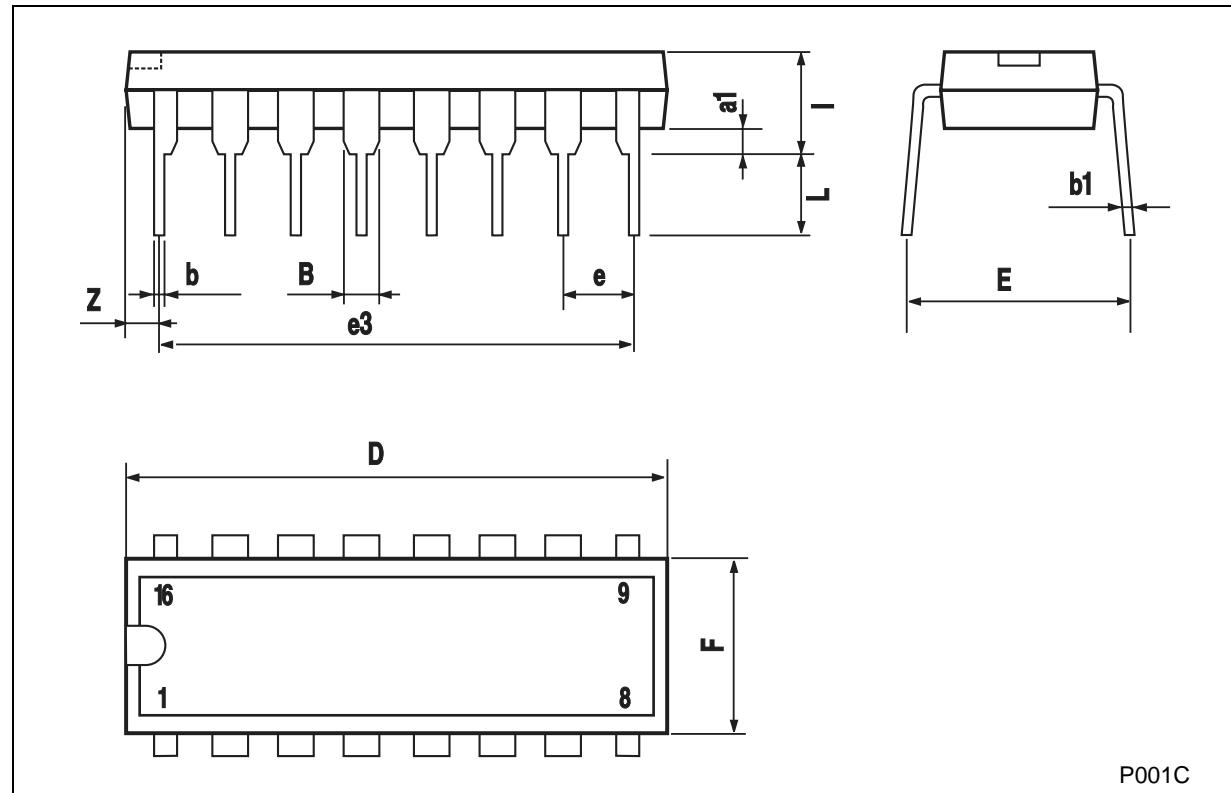
WAVEFORM 2 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



WAVEFORM 3 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

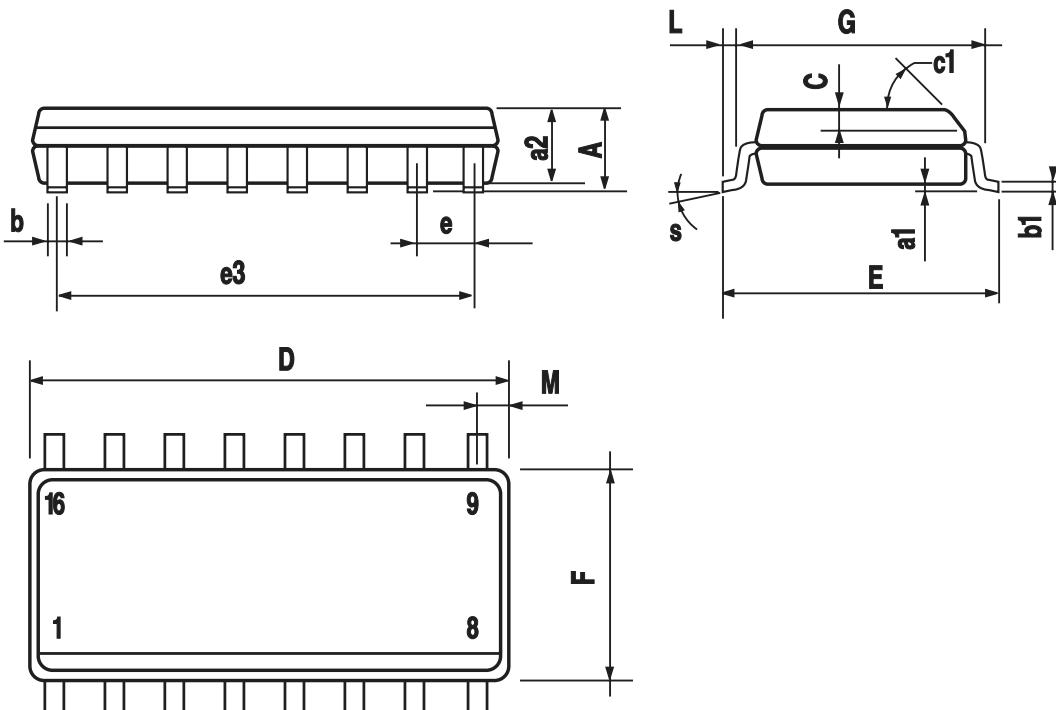


Plastic DIP-16 (0.25) MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

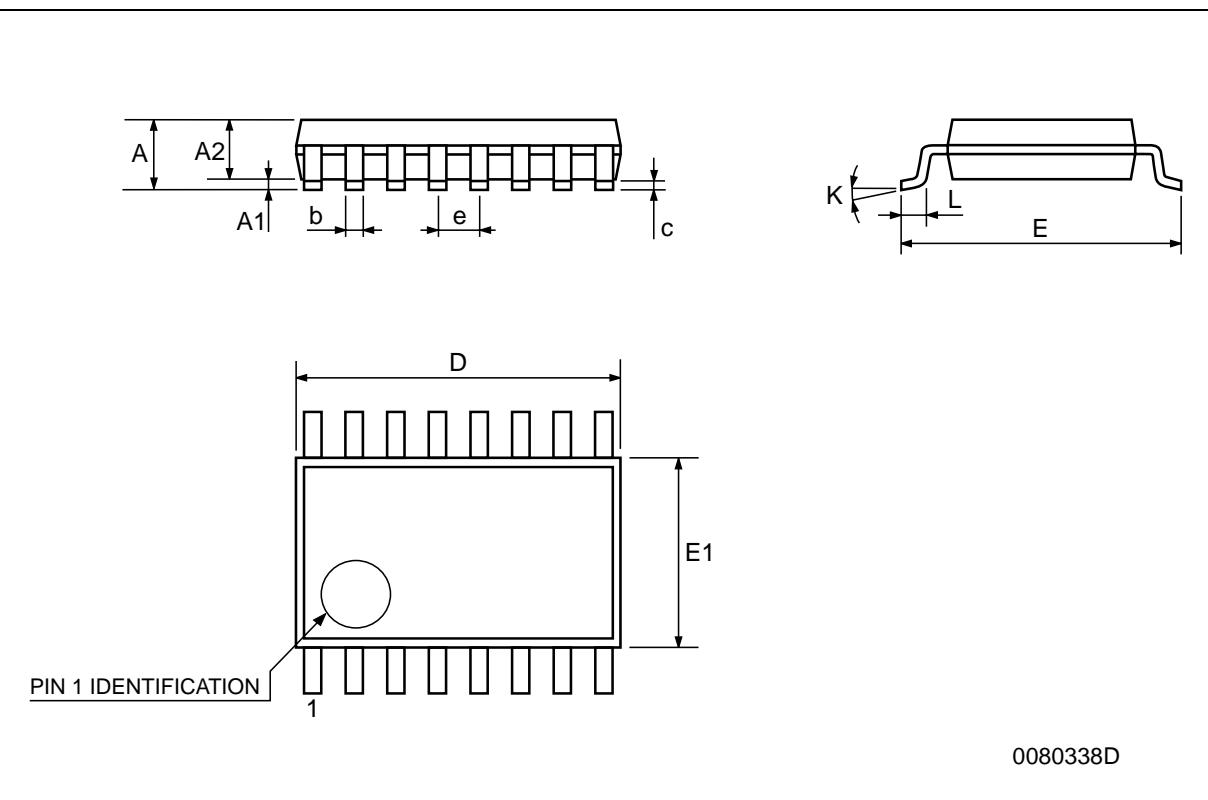
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1		45° (typ.)				
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S		8° (max.)				



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

