

BUJD103AD

NPN power transistor with integrated diode

Rev. 02 — 6 October 2009

Product data sheet

1. Product profile

1.1 General description

High voltage, high speed, planar passivated NPN power switching transistor with integrated anti-parallel E-C diode in a SOT428 (DPAK) surface-mountable plastic package.

1.2 Features and benefits

- Fast switching
- High voltage capability
- Integrated anti-parallel E-C diode
- Very low switching and conduction losses

1.3 Applications

- DC-to-DC converters
- Electronic lighting ballasts
- Inverters
- Motor control systems

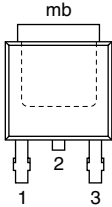
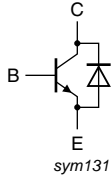
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_C	collector current		-	-	4	A
P_{tot}	total power dissipation	see Figure 4 $T_{mb} \leq 25\text{ °C}$	-	-	80	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$	-	-	700	V
Static characteristics						
h_{FE}	DC current gain	$I_C = 500\text{ mA}$; $V_{CE} = 5\text{ V}$; see Figure 12 $T_j = 25\text{ °C}$	13	22	32	
		$V_{CE} = 5\text{ V}$; $I_C = 3\text{ A}$; $T_{mb} = 25\text{ °C}$; see Figure 12	-	12.5	-	

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base		
2	C	collector [1]		
3	E	emitter		

**SOT428
(DPAK)**

[1] it is not possible to make a connection to pin 2 of the SOT428 (DPAK) package

3. Ordering information

Table 3. Ordering information

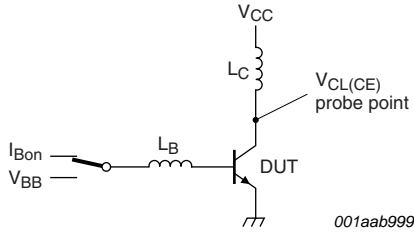
Type number	Package		Version
	Name	Description	
BUJD103AD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

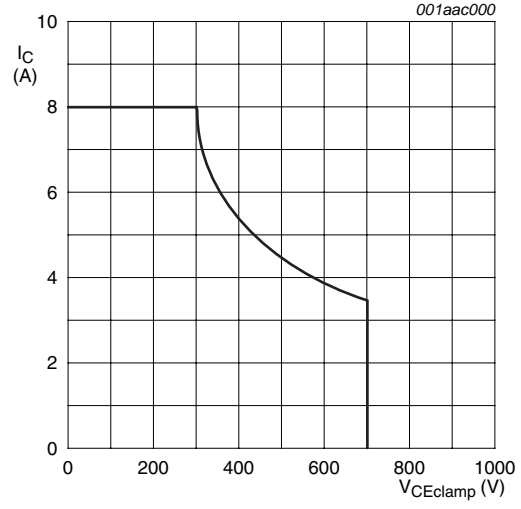
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$	-	700	V
V_{CBO}	collector-base voltage	$I_E = 0\text{ A}$	-	700	V
V_{CEO}	collector-emitter voltage	$I_B = 0\text{ A}$	-	400	V
I_C	collector current		-	4	A
I_{CM}	peak collector current	see Figure 1 , 2 and 3	-	8	A
I_B	base current		-	2	A
I_{BM}	peak base current		-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ °C}$; see Figure 4	-	80	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-	150	°C



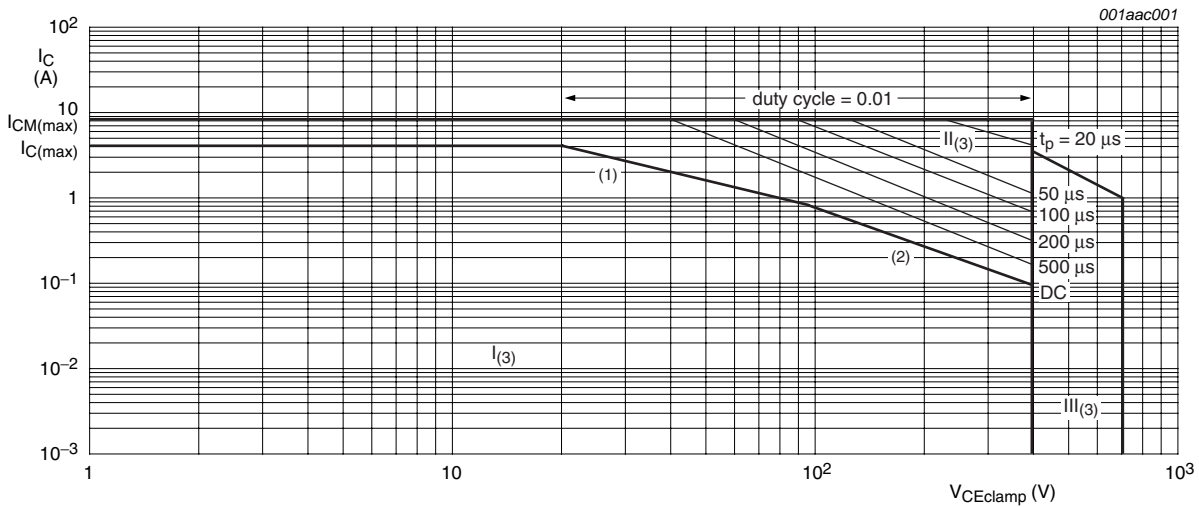
$V_{CEclamp} \leq 1000 \text{ V}; V_{CC} = 150 \text{ V};$
 $V_{BB} = -5 \text{ V}; L_B = 1 \mu\text{H}; L_C = 200 \mu\text{H}$

Fig 1. Test circuit for reverse bias safe operating area



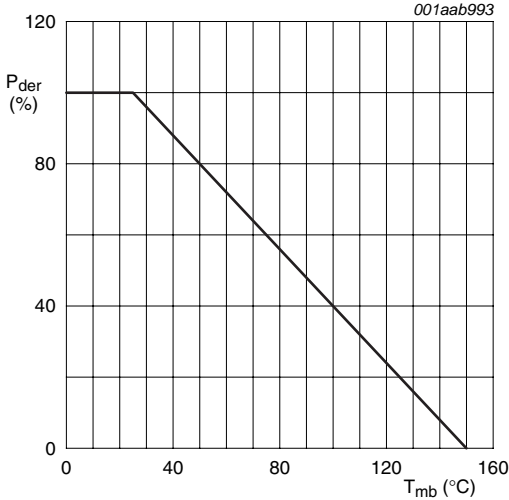
$T_j \leq T_{j(max)} \text{ } ^\circ\text{C}$

Fig 2. Reverse bias safe operating area



- (1) P_{tot} maximum and P_{tot} peak maximum lines
- (2) Second breakdown limits
- (3) I = Region of permissible DC operation
 II = Extension for repetitive pulse operation
 III = Extension during turn-on in single transistor converters provided that $R_{BE} \leq 100 \Omega$ and $t_p = 0.6 \mu\text{s}$

Fig 3. Forward bias safe operating area for $T_{mb} \leq 25 \text{ } ^\circ\text{C}$



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 4. Normalized total power dissipation as a function of mounting base temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed-circuit-board mounted; minimum footprint; see Figure 6	-	75	-	K/W

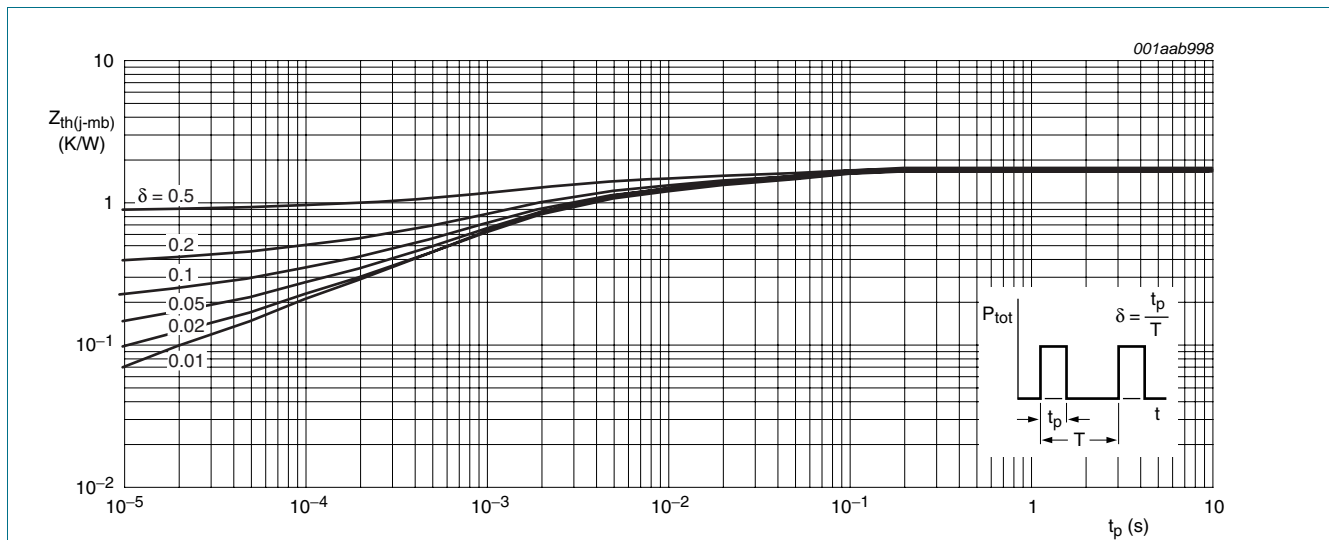


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse width

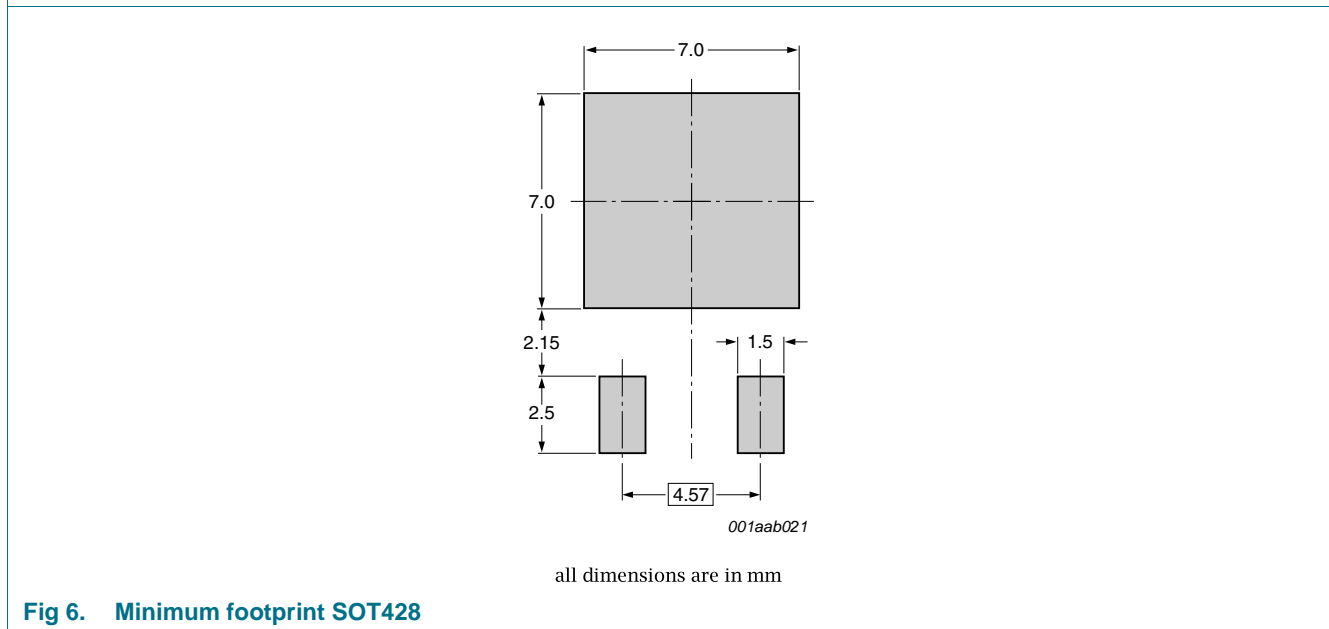


Fig 6. Minimum footprint SOT428

6. Characteristics

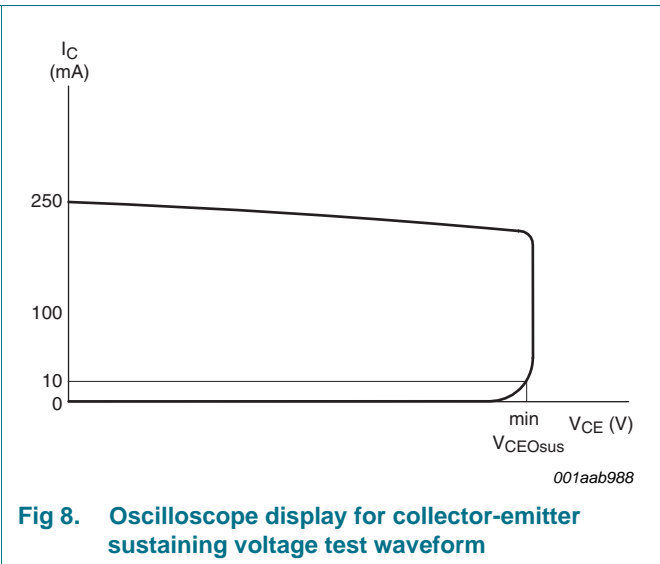
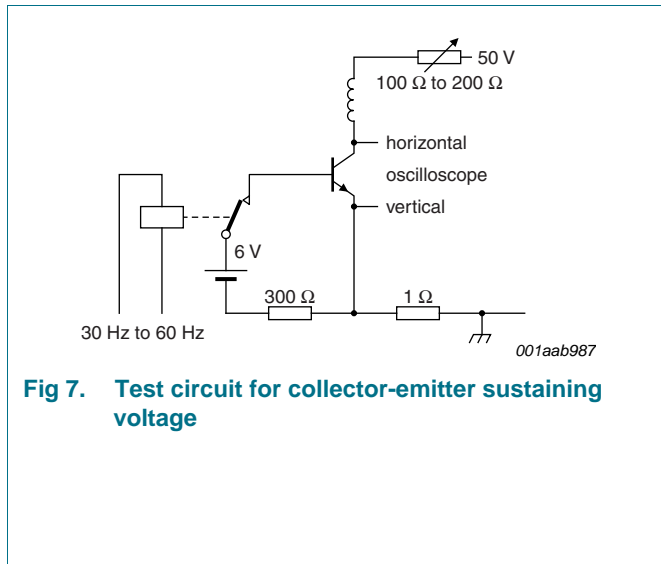
Table 6. Characteristics

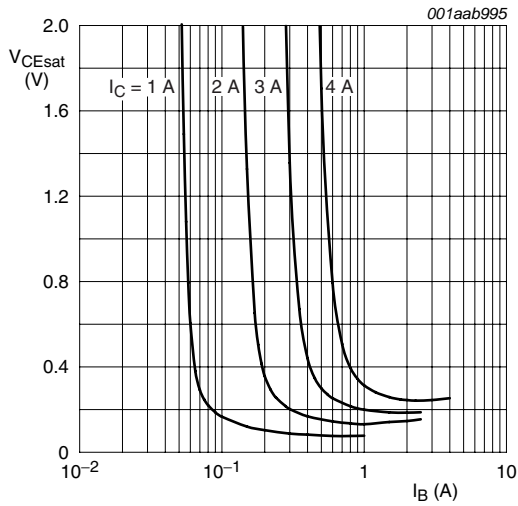
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{CES}	collector-emitter cut-off current	$V_{BE} = 0\text{ V}; V_{CE} = 700\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-	1	mA
		$V_{BE} = 0\text{ V}; V_{CE} = 700\text{ V}; T_j = 125\text{ }^\circ\text{C};$	[1]	-	2	mA
		$V_{BE} = 0\text{ V}; V_{CE} = 700\text{ V}; T_j = 25\text{ }^\circ\text{C};$	[1]	-	1	mA
		$V_{BE} = 0\text{ V}; V_{CE} = 700\text{ V}; T_j = 100\text{ }^\circ\text{C}$	-	-	5	mA
I_{CBO}	collector-base cut-off current	$V_{CB} = 700\text{ V}; I_E = 0\text{ A};$	[1]	-	1	mA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 400\text{ V}; I_B = 0\text{ A};$	[1]	-	0.1	mA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 9\text{ V}; I_C = 0\text{ A}$	-	-	1	mA
		$V_{EB} = 7\text{ V}; I_C = 0\text{ A}$	-	-	10	mA
V_{CEOsus}	collector-emitter sustaining voltage	$I_B = 0\text{ A}; I_C = 10\text{ mA}; L_C = 25\text{ mH};$ see Figure 7 and 8	400	-	-	V
V_{CEsat}	collector-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 0.2\text{ A};$ see Figure 9 and 10	-	0.1	0.5	V
		$I_C = 2\text{ A}; I_B = 0.5\text{ A};$ see Figure 9 and 10	-	0.2	0.6	V
		$I_C = 3\text{ A}; I_B = 0.6\text{ A};$ see Figure 9 and 10	-	0.25	1	V
		$I_C = 4\text{ A}; I_B = 1\text{ A};$ see Figure 9 and 10	-	0.3	1	V
V_{BEsat}	base-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 0.2\text{ A};$ see Figure 11	-	0.85	1.2	V
		$I_C = 2\text{ A}; I_B = 0.5\text{ A};$ see Figure 11	-	0.92	1.6	V
		$I_C = 3\text{ A}; I_B = 0.6\text{ A};$ see Figure 11	-	0.97	1.5	V
V_F	forward voltage	$I_F = 2\text{ A}$	-	1.04	1.5	V
h_{FE}	DC current gain	$I_C = 1\text{ mA}; V_{CE} = 5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C};$ see Figure 12	10	17	32	
		$I_C = 500\text{ mA}; V_{CE} = 5\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 12	13	22	32	
		$I_C = 1\text{ A}; V_{CE} = 5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C};$ see Figure 12	12	20	40	
		$I_C = 2\text{ A}; V_{CE} = 5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C};$ see Figure 12	11	16	22	
		$I_C = 3\text{ A}; V_{CE} = 5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C};$ see Figure 12	-	12.5	-	
Dynamic characteristics						
t_{on}	turn-on time	$I_C = 2.5\text{ A}; I_{Bon} = 0.5\text{ A}; I_{Boff} = -0.5\text{ A};$ $R_L = 75\text{ }^\circ\Omega; T_j = 25\text{ }^\circ\text{C};$ resistive load; see Figure 13 and 14	-	0.52	0.6	μs

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_s	storage time	$I_C = 2.5 \text{ A}$; $I_{B\text{on}} = 0.5 \text{ A}$; $I_{B\text{off}} = -0.5 \text{ A}$; $R_L = 75 \text{ } \Omega$; $T_j = 25 \text{ } ^\circ\text{C}$; resistive load; see Figure 13 and 14	-	2.7	3.3	μs
		$I_C = 2 \text{ A}$; $I_{B\text{on}} = 0.4 \text{ A}$; $V_{BB} = -5 \text{ V}$; $L_B = 1 \text{ } \mu\text{H}$; $T_j = 25 \text{ } ^\circ\text{C}$; inductive load; see Figure 15 and 16	-	1.2	1.4	μs
		$I_C = 2 \text{ A}$; $I_{B\text{on}} = 0.4 \text{ A}$; $V_{BB} = -5 \text{ V}$; $L_B = 1 \text{ } \mu\text{H}$; $T_j = 100 \text{ } ^\circ\text{C}$; inductive load; see Figure 15 and 16	-	-	1.8	μs
t_f	fall time	$I_C = 2.5 \text{ A}$; $I_{B\text{on}} = 0.5 \text{ A}$; $I_{B\text{off}} = -0.5 \text{ A}$; $R_L = 75 \text{ } \Omega$; $T_j = 25 \text{ } ^\circ\text{C}$; resistive load; see Figure 17 and 14	-	0.3	0.35	μs
		$I_C = 2 \text{ A}$; $I_{B\text{on}} = 0.4 \text{ A}$; $V_{BB} = -5 \text{ V}$; $L_B = 1 \text{ } \mu\text{H}$; $T_j = 100 \text{ } ^\circ\text{C}$; inductive load; see Figure 15 and 16	-	-	120	ns
		$I_C = 2 \text{ A}$; $I_{B\text{on}} = 0.4 \text{ A}$; $V_{BB} = -5 \text{ V}$; $L_B = 1 \text{ } \mu\text{H}$; $T_j = 25 \text{ } ^\circ\text{C}$; inductive load; see Figure 18 and 16	-	30	60	ns

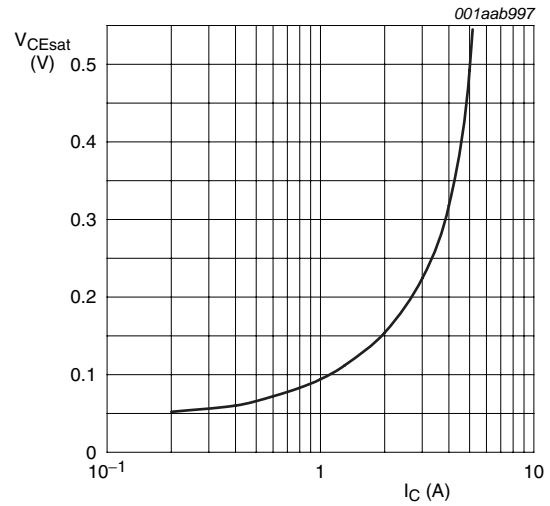
[1] Measured with half sine-wave voltage (curve tracer)





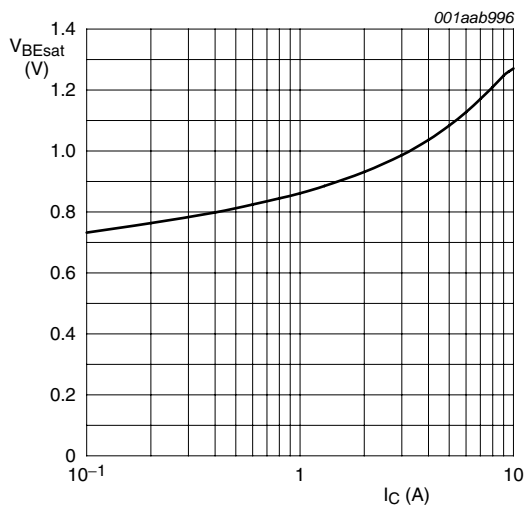
$T_j = 25\text{ }^\circ\text{C}$

Fig 9. Collector-emitter saturation voltage as a function of base current; typical values



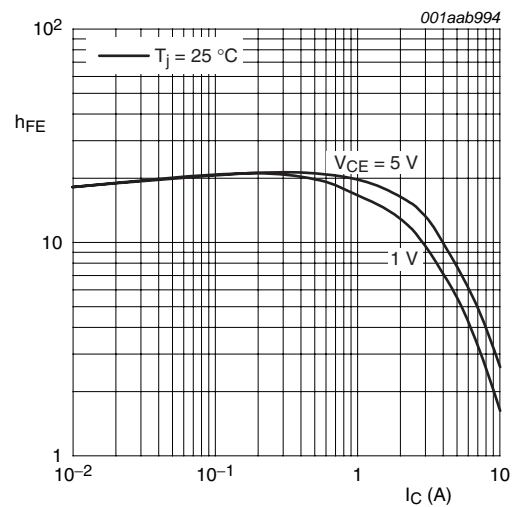
$I_C / I_B = 4$

Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



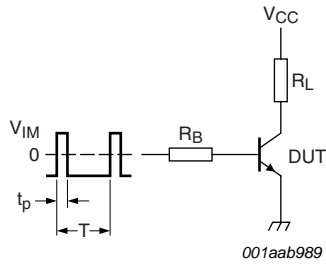
$I_C / I_B = 4$

Fig 11. Base-emitter saturation voltage as a function of collector current; typical values



$I_C / I_B = 4$

Fig 12. DC current gain as a function of collector current; typical values



$V_{IM} = -6 \text{ to } +8 \text{ V}$; $V_{CC} = 250 \text{ V}$; $t_p = 20 \mu\text{s}$; $\delta = \frac{t_p}{T} = 0.01$
 R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig 13. Test circuit for resistive load switching

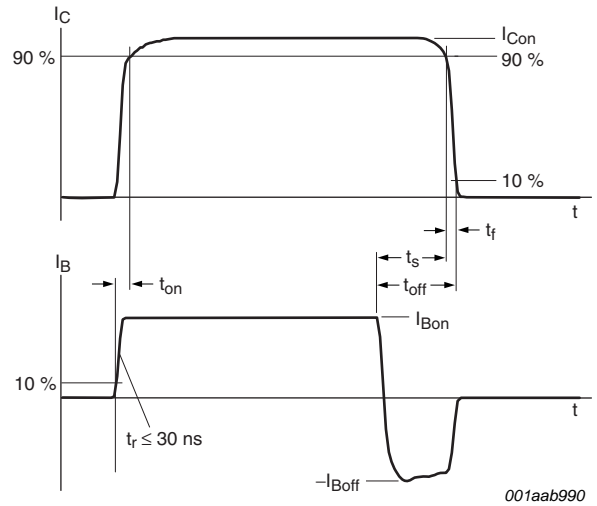
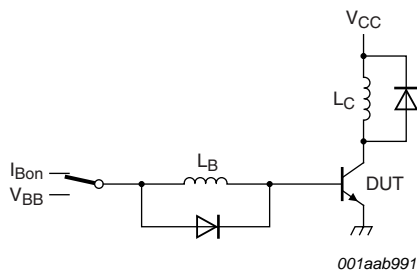


Fig 14. Switching times waveforms for resistive load



$V_{CC} = 300 \text{ V}$; $V_{BB} = -5 \text{ V}$; $L_C = 200 \mu\text{H}$; $L_B = 1 \mu\text{H}$

Fig 15. Test circuit for inductive load switching

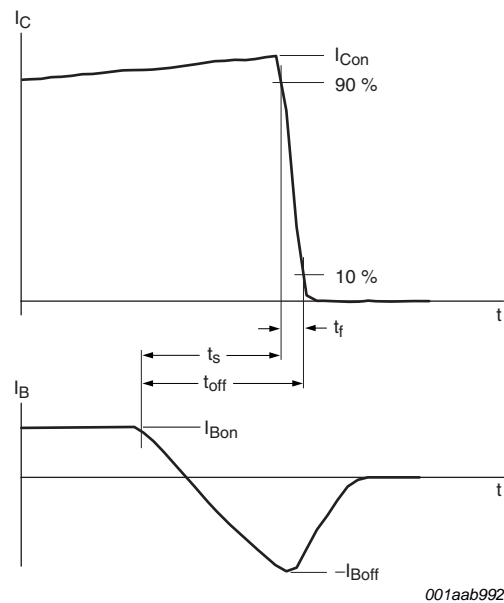
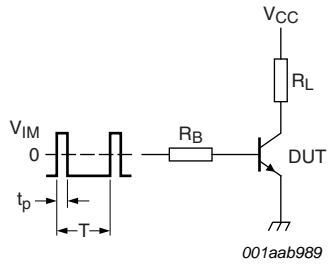
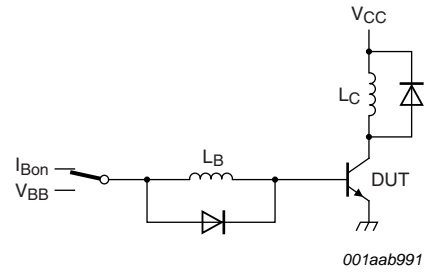


Fig 16. Switching times waveforms for inductive load



$V_{IM} = -6\text{ V to }+8\text{ V}; V_{CC} = 250\text{ V};$
 $t_p = 20\text{ }\mu\text{s}; \delta = t_p/T = 0.01R_B$ and R_L
 calculated from I_{Con} and I_{Bon} requirements

Fig 17. Test circuit for resistive load switching



$V_{CC} = 300\text{ V}; V_{BB} = -5\text{ V}; L_C = 200\text{ }\mu\text{H}; L_B = 1\text{ }\mu\text{H}$

Fig 18. Test circuit for inductive load switching

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

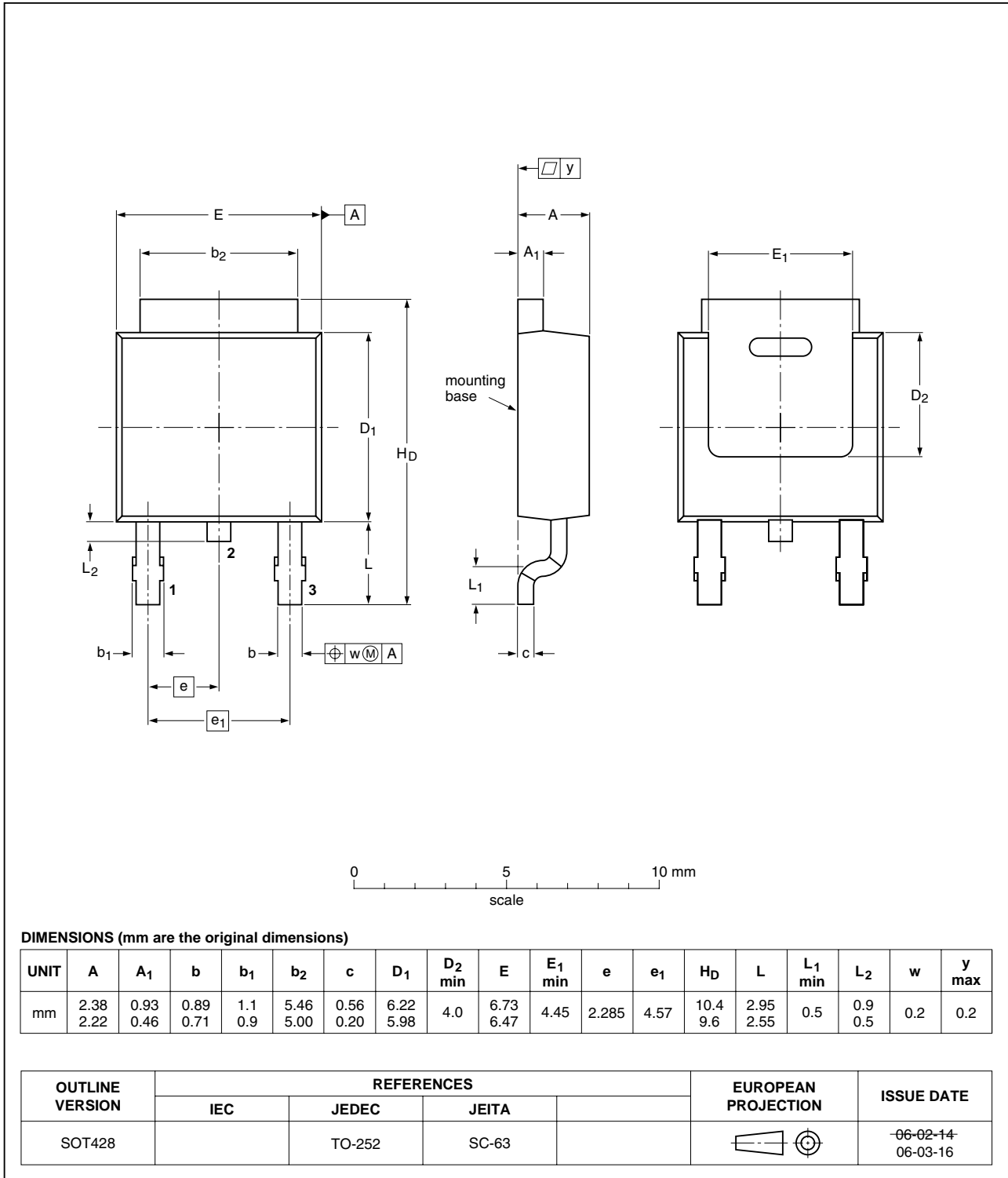


Fig 19. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUJD103AD_2	20091006	Product data sheet	-	BUJD103AD_1
Modifications:	• Various changes to content.			
BUJD103AD_1	20090508	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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