

N-Channel Enhancement Mode Power MOSFET

MTN2N60I3

 $BV_{DSS} : 650V @ T_j=150^{\circ}C$ **$R_{DS(ON)} : 4.7 \Omega$** **$I_D : 1.9A$**

Description

The MTN2N60I3 is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-251 package is universally preferred for all commercial-industrial applications

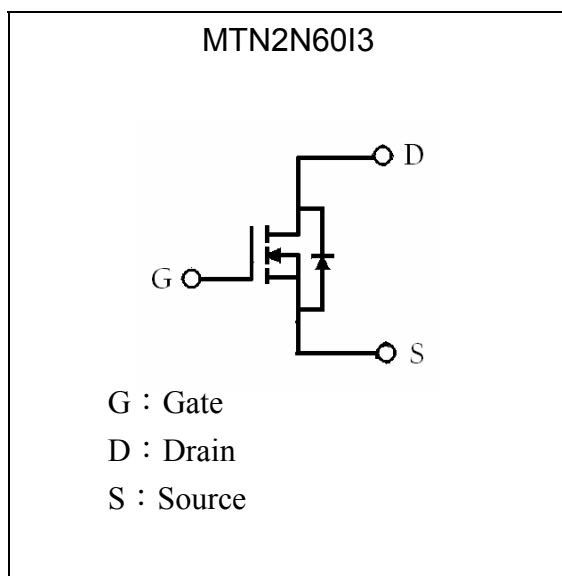
Features

- $BV_{DSS}=650V$ typically @ $T_j=150^{\circ}C$
- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- RoHS compliant package

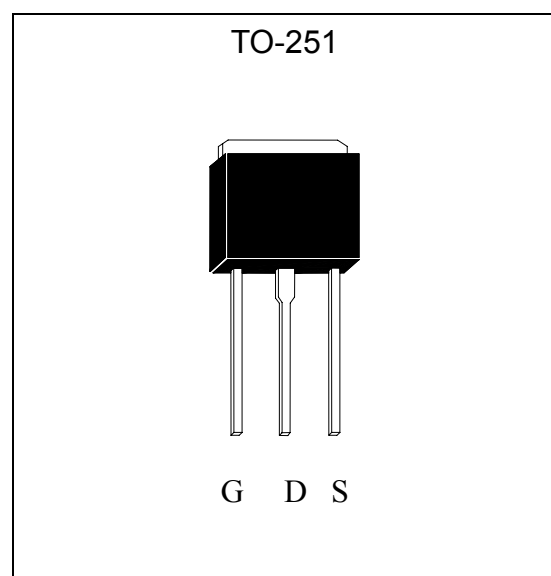
Applications

- Open Framed Power Supply
- Adapter
- STB

Symbol



Outline



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	1.9	A
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$	I_D	1.14	A
Pulsed Drain Current @ $V_{GS}=10\text{V}$ (Note 1)	I_{DM}	7.6	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	60	mJ
Avalanche Current (Note 1)	I_{AR}	1.9	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	4.4	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Maximum Temperature for Soldering @ Lead at 0.125 in(0.318mm) from case for 10 seconds	T_L	300	$^{\circ}\text{C}$
Total Power Dissipation ($T_A=25^{\circ}\text{C}$)	P_D	1.5	W
Total Power Dissipation ($T_C=25^{\circ}\text{C}$)		44	W
Linear Derating Factor		0.35	W/ $^{\circ}\text{C}$
Operating Junction and Storage Temperature	T_j, T_{stg}	-55~+150	$^{\circ}\text{C}$

Note : 1.Repetitive rating; pulse width limited by maximum junction temperature.

2. $I_{AS}=1.2\text{A}$, $V_{DD}=50\text{V}$, $L=80\text{mH}$, $R_G=25\Omega$, starting $T_J=+25^{\circ}\text{C}$.

3. $I_{SD}\leq 2\text{A}$, $di/dt\leq 100\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, starting $T_J=+25^{\circ}\text{C}$.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	2.87	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	83.3	$^{\circ}\text{C}/\text{W}$



Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	600	-	-	V	V _{GS} =0, I _D =250μA, T _j =25°C
BV _{DSS}	-	650	-	V	V _{GS} =0, I _D =250μA, T _j =150°C
ΔBV _{DSS} /ΔT _j	-	0.6	-	V/°C	Reference to 25°C, I _D =250μA
BV _{DS}	-	700	-	V	V _{GS} =0, I _D =1.2A
V _{GS(th)}	2.0	-	4.0	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	5	-	S	V _{DS} =15V, I _D =0.95A
I _{GSS}	-	-	±100	nA	V _{GS} =±30
I _{DSS}	-	-	1	μA	V _{DS} =600V, V _{GS} =0
	-	-	10	μA	V _{DS} =480V, V _{GS} =0, T _C =125°C
*R _{DS(ON)}	-	-	4.7	Ω	V _{GS} =10V, I _D =0.95A
Dynamic					
*Q _g	-	8.5	12	nC	I _D =2A, V _{DD} =480V, V _{GS} =10V
*Q _{gs}	-	1.3	-		
*Q _{gd}	-	4.1	-		
*t _{d(ON)}	-	9	28	ns	V _{DD} =300V, I _D =2A, V _{GS} =10V, R _G =25Ω, R _D =150Ω
*t _r	-	25	60		
*t _{d(OFF)}	-	24	58		
*t _f	-	28	66		
C _{iss}	-	180	235	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
C _{oss}	-	20	25		
C _{rss}	-	4.3	5.6		
Source-Drain Diode					
*V _{SD}	-	-	1.4	V	I _S =1.9A, V _{GS} =0V
*I _S	-	-	1.9	A	
*I _{SM}	-	-	7.6		
*t _{rr}	-	230	-	ns	V _{GS} =0, I _F =2A, dI/dt=100A/μs
*Q _{rr}	-	1	-	μC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

Device	Package	Shipping	Marking
MTN2N60I3	TO-251 (RoHS compliant)	80 pcs / tube, 50 tubes / box	2N60

Characteristic Curves

Figure 1. On-Region Characteristics

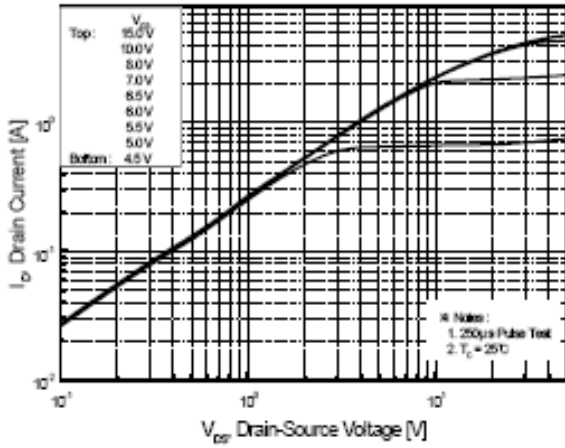


Figure 2. Transfer Characteristics

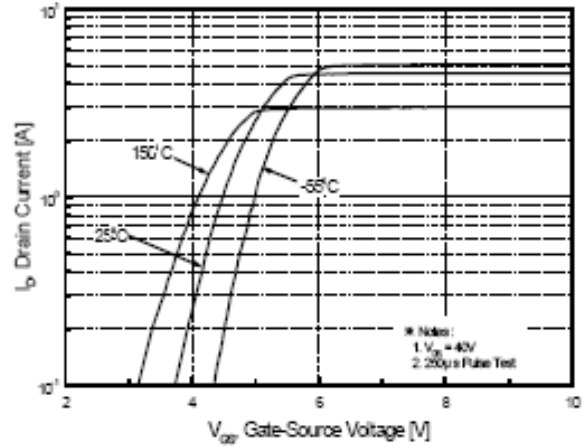


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

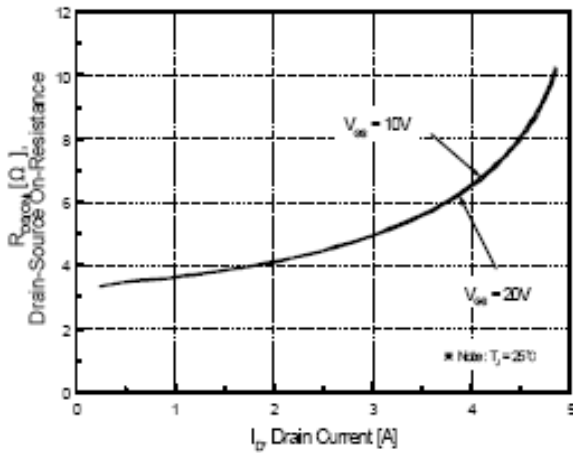


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

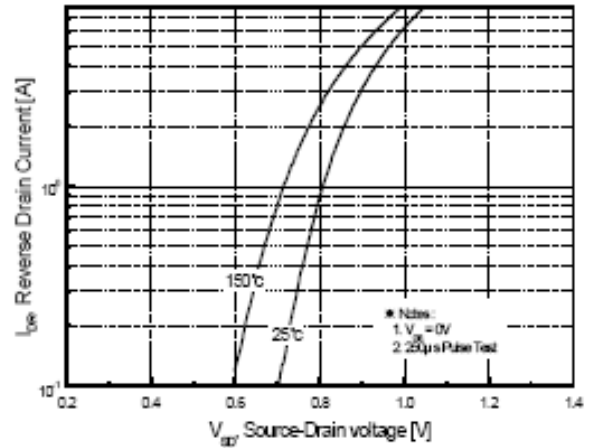


Figure 5. Capacitance Characteristics

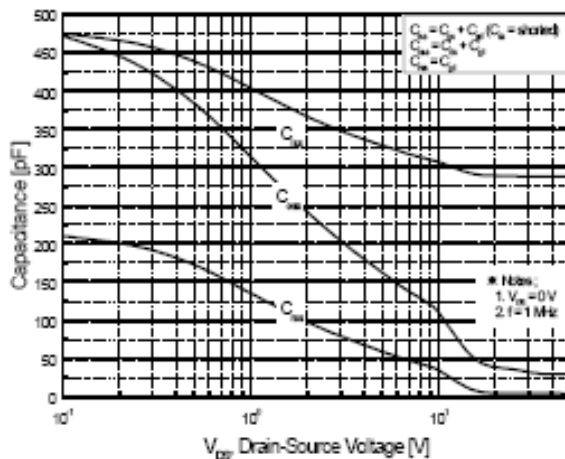
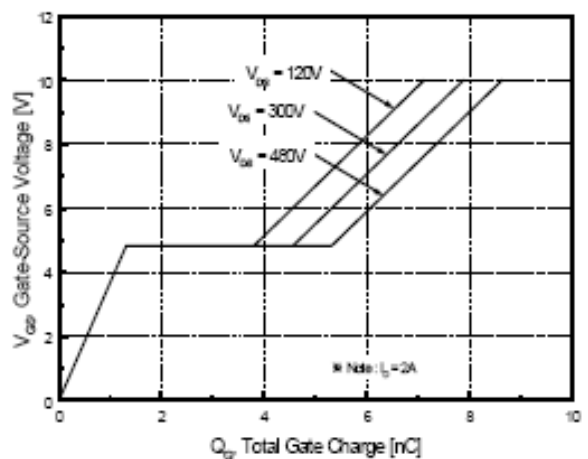


Figure 6. Gate Charge Characteristics



Characteristic Curves(Cont.)

Figure 7. Breakdown Voltage Variation vs. Temperature

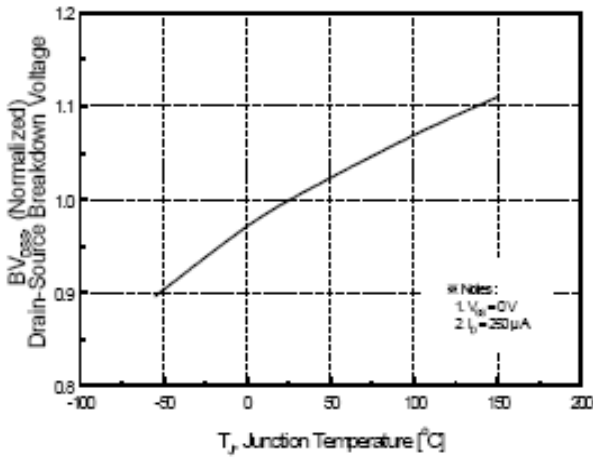


Figure 8. On-Resistance Variation vs. Temperature

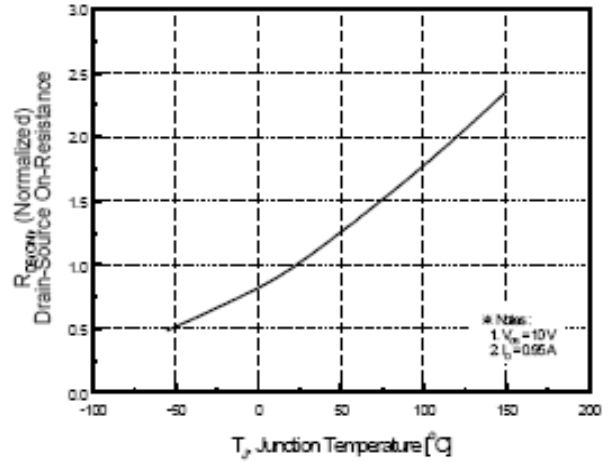


Figure 9. Maximum Safe Operating Area

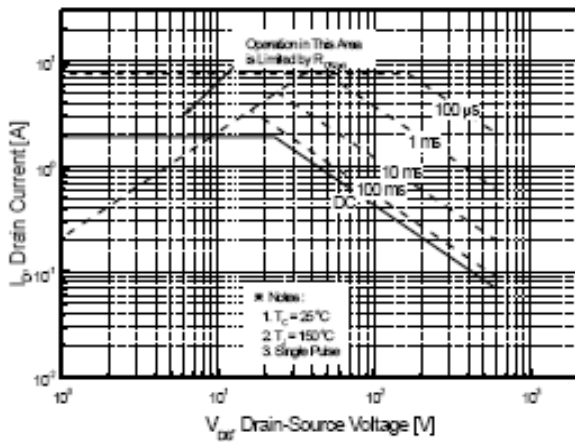


Figure 10. Maximum Drain Current vs. Case Temperature

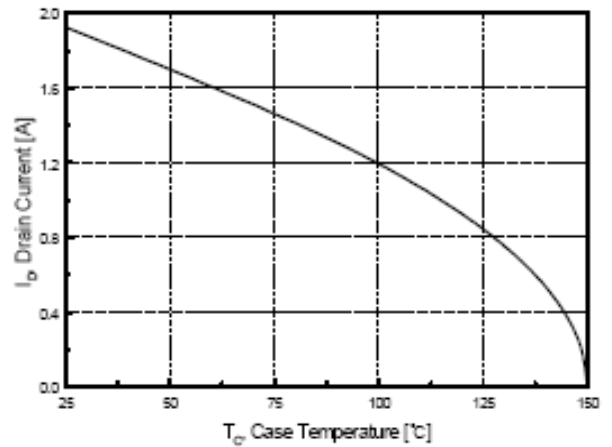
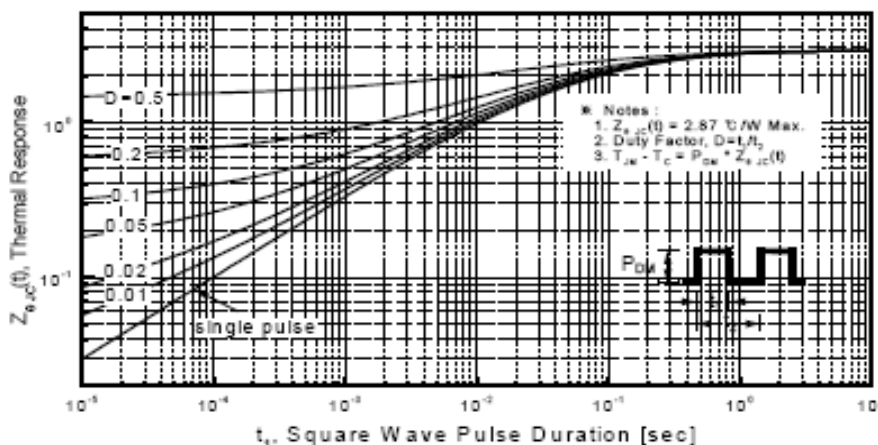


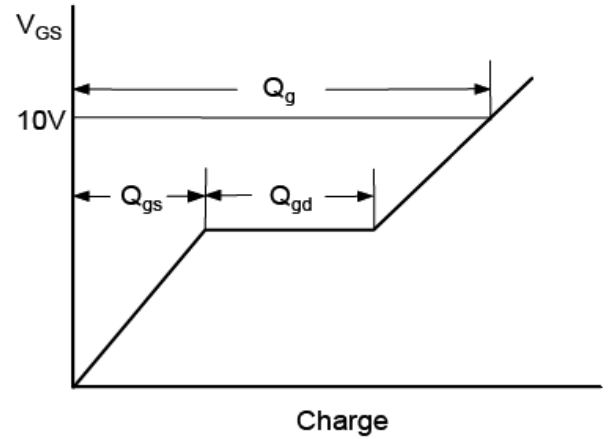
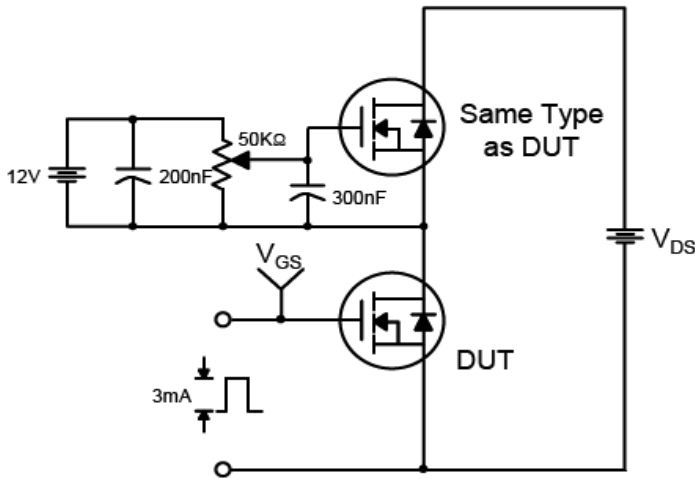
Figure 11. Typical Drain Current Slope vs. Gate Resistance

Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance

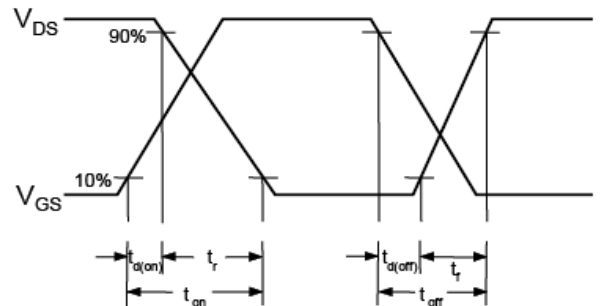
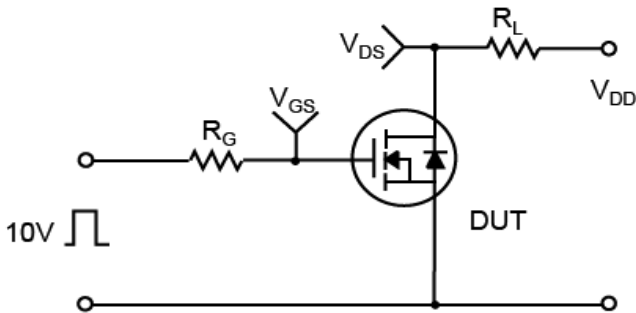


Test Circuits and Waveforms

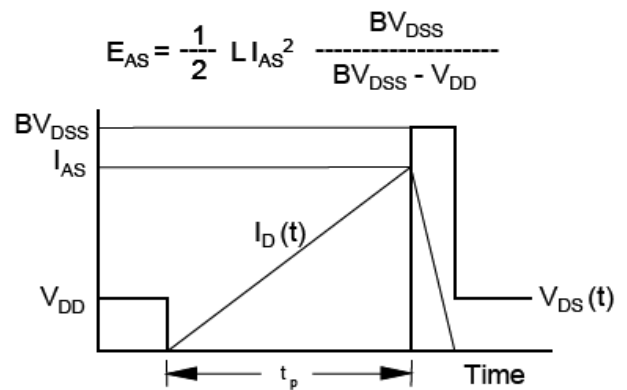
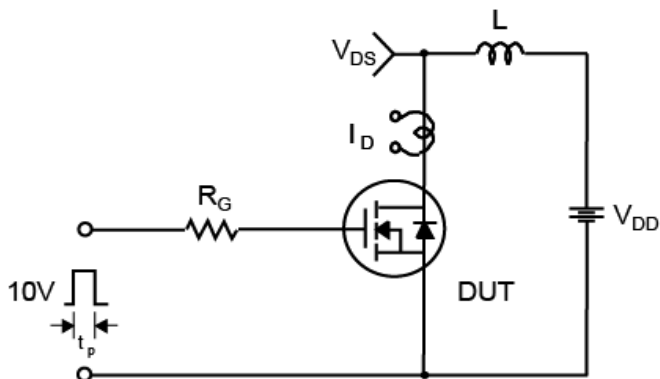
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

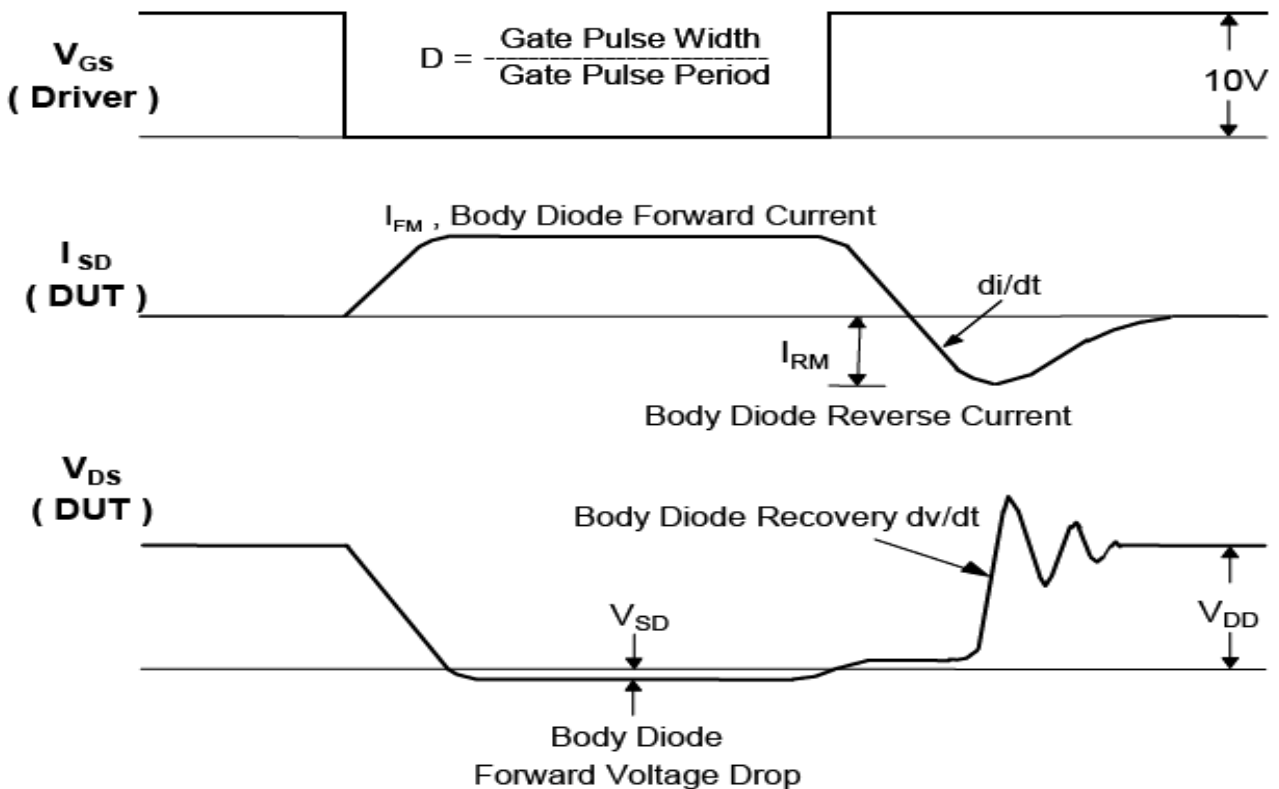
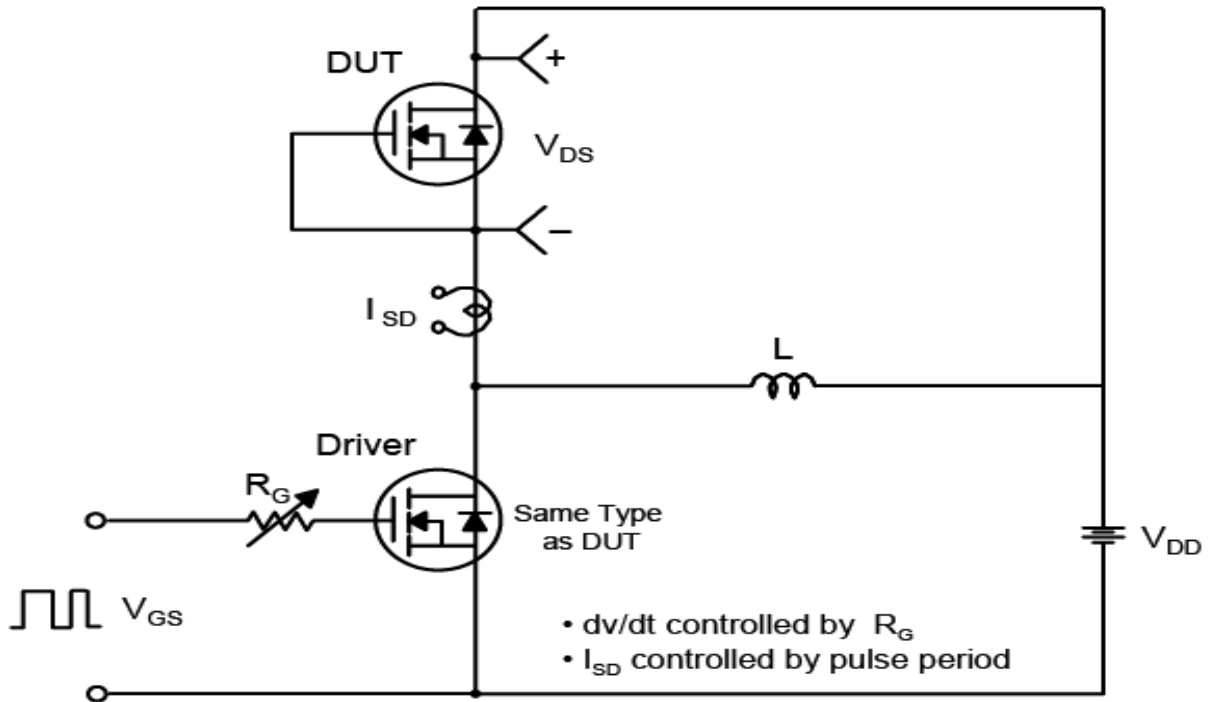


Unclamped Inductive Switching Test Circuit & Waveforms



Test Circuits and Waveforms(Cont.)

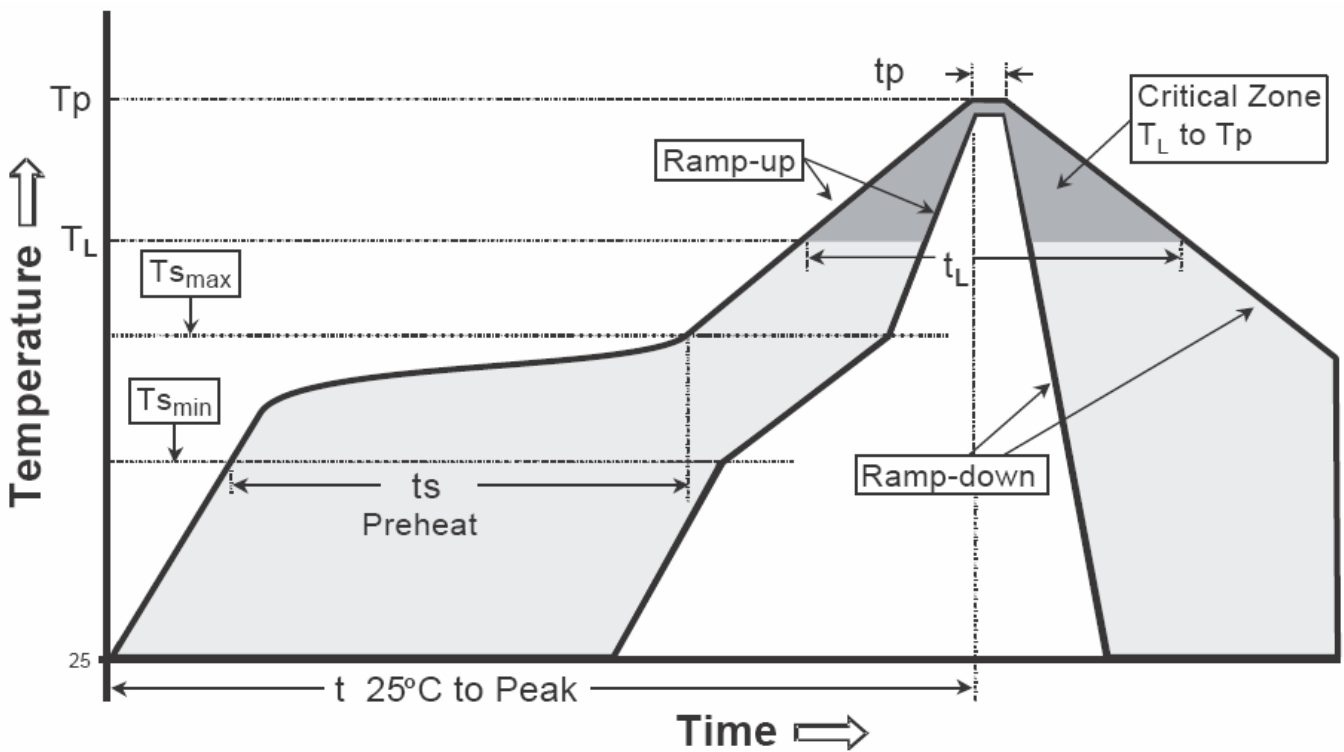
Peak Diode Recovery dv/dt Test Circuit & Waveforms



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

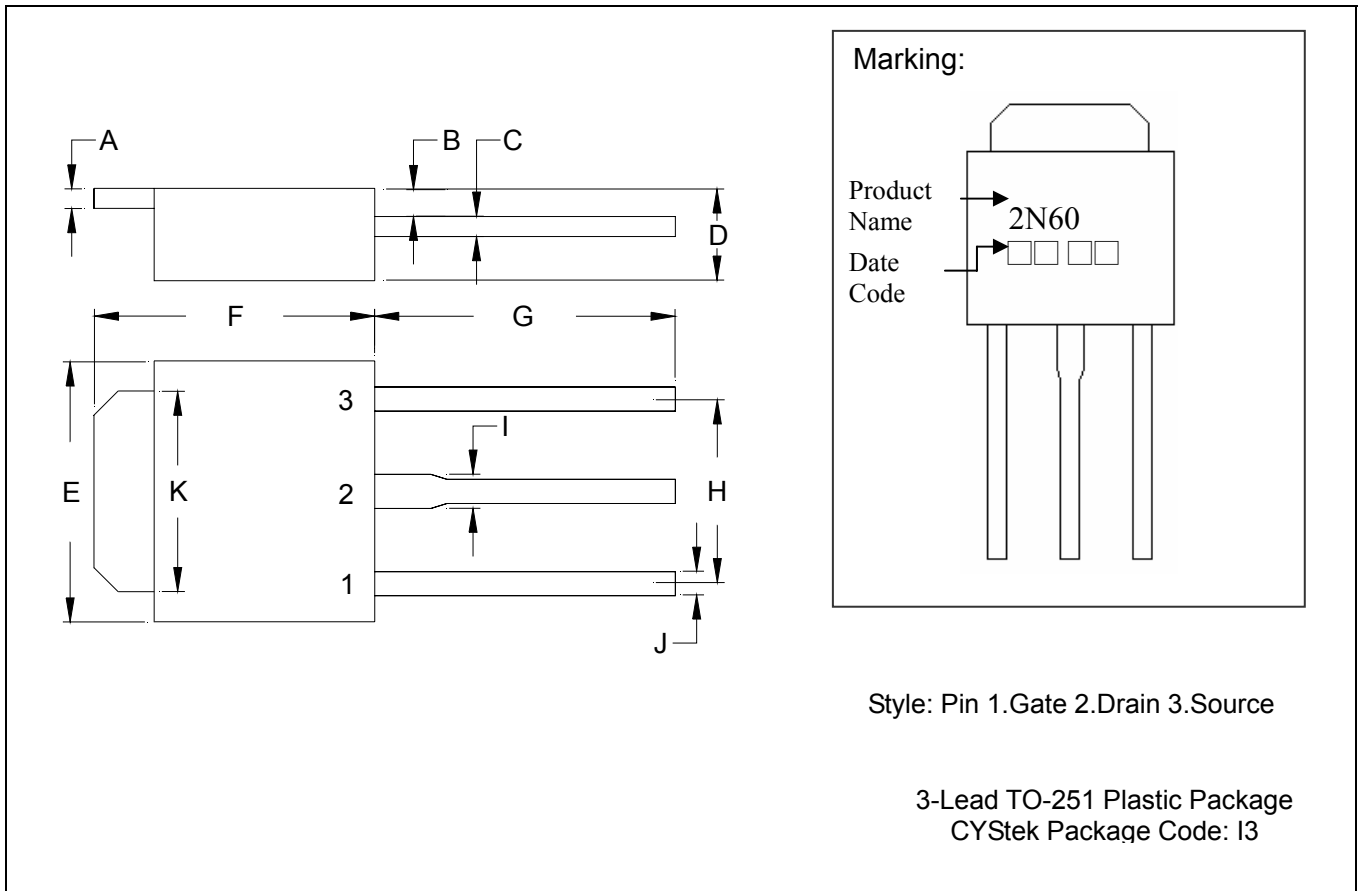
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-251 Dimension



Marking:

Product Name → 2N60
 Date Code → □ □ □ □

Style: Pin 1.Gate 2.Drain 3.Source

3-Lead TO-251 Plastic Package
 CYStek Package Code: I3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0177	0.0217	0.45	0.55	G	0.2559	-	6.50	-
B	0.0354	0.0591	0.90	1.50	H	-	*0.1811	-	*4.60
C	0.0177	0.0236	0.45	0.60	I	-	0.0449	-	1.14
D	0.0866	0.0945	2.20	2.40	J	-	0.0346	-	0.88
E	0.2441	0.2677	6.20	6.80	K	0.2047	0.2165	5.20	5.50
F	0.2677	0.2835	6.80	7.20					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: KFC; pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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