

2.5V Single Data Rate 1:5 Clock Buffer Terabuffer

Features

- Optimized for 2.5V LVTTTL
- Guaranteed Low Skew < 25pS (max)
- Very low duty cycle distortion < 300pS (max)
- High speed propagation delay < 1.8nS. (max)
- Up to 200MHz operation
- Very low CMOS power levels
- Hot Insert able and over-voltage tolerant inputs
- 1:5 fan-out buffer
- 2.5V Supply Voltage
- Available in TSSOP Package

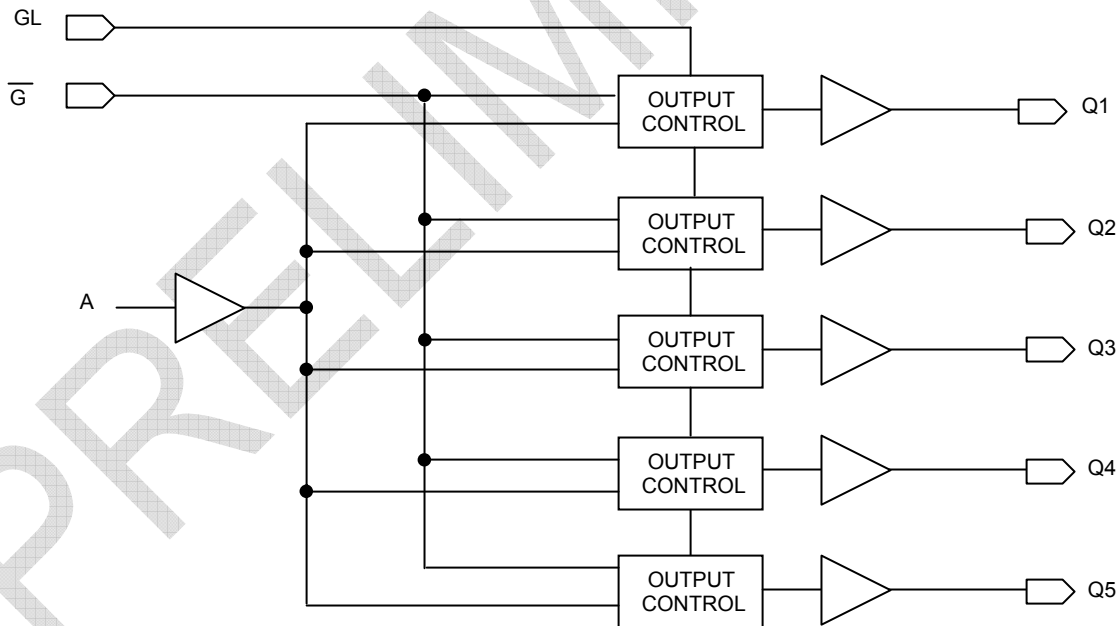
The PCS2P5T9050A 2.5V single data rate (SDR) clock buffer is a single-ended input to five single-ended outputs buffer built on advanced metal CMOS technology. The SDR clock buffer fan-out from a single input to five single-ended outputs reduces the loading on the preceding driver and provides an efficient clock distribution network. Multiple power and grounds reduce noise.

Applications:

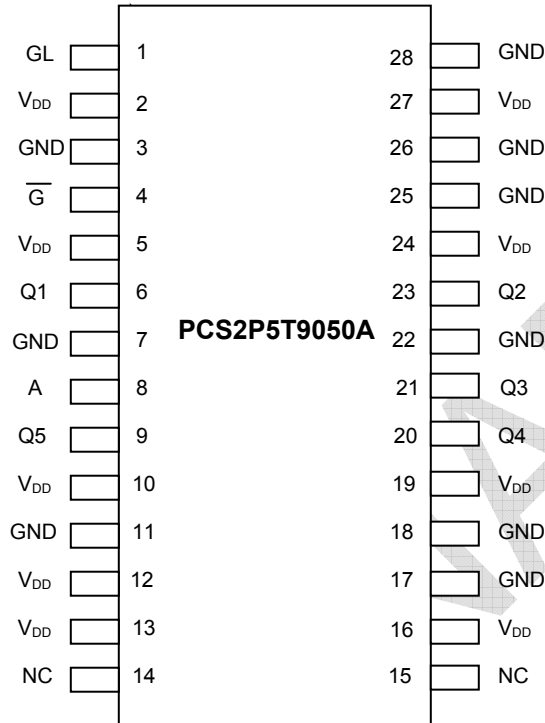
PCS2P5T9050A is targeted towards Clock and signal distribution applications.

Functional Description

Block Diagram



Pin Configuration- Top View – TSSOP Package



Pin Description

Symbol	I/O	Type	Description
A	I	LVTTL	Clock input
\bar{G}	I	LVTTL	Gate control for Qn outputs. When \bar{G} is LOW, these outputs are enabled. When \bar{G} is HIGH, these outputs are asynchronously disabled to the level designated by GL ¹ .
GL	I	LVTTL	Specifies output disable level. If HIGH, the outputs disable HIGH. If LOW, the outputs disable LOW.
Qn	O	LVTTL	Clock outputs
V _{DD}		PWR	Power supply for the device core, inputs, and outputs
GND		PWR	Power supply return for power

NOTE:

1. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.

November 2006

rev 0.2

Absolute Maximum Ratings

Symbol	Description	Max	Unit
V _{DD}	Power Supply Voltage	-0.5 to +3.6	V
V _I	Input Voltage	-0.5 to +3.6	V
V _O	Output Voltage	-0.5 to V _{DD} +0.5	V
T _{STG}	Storage Temperature	-65 to +165	°C
T _J	Junction Temperature	150	°C

Note:

1. These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Capacitance¹ (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Typ	Max	Unit
C _{IN}	Input Capacitance		6		pF

NOTE:

1. This parameter is measured at characterization but not tested.

Recommended Operating Range

Symbol	Description	Min	Typ	Max	Unit
T _A	Ambient Operating Temperature	-40	+25	+85	°C
V _{DD}	Internal Power Supply Voltage	2.3	2.5	2.7	V

DC Electrical Characteristics Over Operating Range¹

Symbol	Parameter	Test Conditions	Min	Typ ⁴	Max	Unit
I _{IH}	Input HIGH Current	V _{DD} = 2.7V V _I = V _{DD} /GND			±5	µA
I _{IL}	Input LOW Current	V _{DD} = 2.7V V _I = GND/V _{DD}			±5	
V _{IK}	Clamp Diode Voltage	V _{DD} = 2.3V, I _{IN} = -18mA		-0.7	- 1.2	V
V _{IN}	DC Input Voltage		-0.3		+3.6	V
V _{IH}	DC Input HIGH ²		1.7			V
V _{IL}	DC Input LOW ³				0.7	V
V _{OH}	Output HIGH Voltage	I _{OH} = -12mA	V _{DD} - 0.4			V
		I _{OH} = -100µA	V _{DD} - 0.1			V
V _{OL}	Output LOW Voltage	I _{OL} = 12mA			0.4	V
		I _{OL} = 100µA			0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. Voltage required to maintain a logic HIGH.
3. Voltage required to maintain a logic LOW.
4. Typical values are at V_{DD} = 2.5V, +25°C ambient.

Power Supply Characteristics

Symbol	Parameter	Test Conditions ¹	Typ	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current	V _{DD} = Max., Reference Clock = LOW Outputs enabled, All outputs unloaded	1	1.5	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V _{DD} = Max., C _L = 0pF	100	150	µA/MHz
I _{TOT}	Total Power V _{DD} Supply Current	V _{DD} = 2.5V., F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF	50	65	mA
		V _{DD} = 2.5V., F _{REFERENCE CLOCK} = 200MHz, C _L = 15pF	75	100	

NOTE:

1. The termination resistors are excluded from these measurements.

Input AC Test Conditions

Symbol	Parameter	Value	Units
V _{IH}	Input HIGH Voltage	V _{DD}	V
V _{IL}	Input LOW Voltage	0	V
V _{TH}	Input Timing Measurement Reference Level ¹	V _{DD} /2	V
t _R , t _F	Input Signal Edge Rate ²	2	V/nS

NOTES:

1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
2. The input signal edge rate of 2V/nS or greater is to be maintained in the 10% to 90% range of the input waveform.

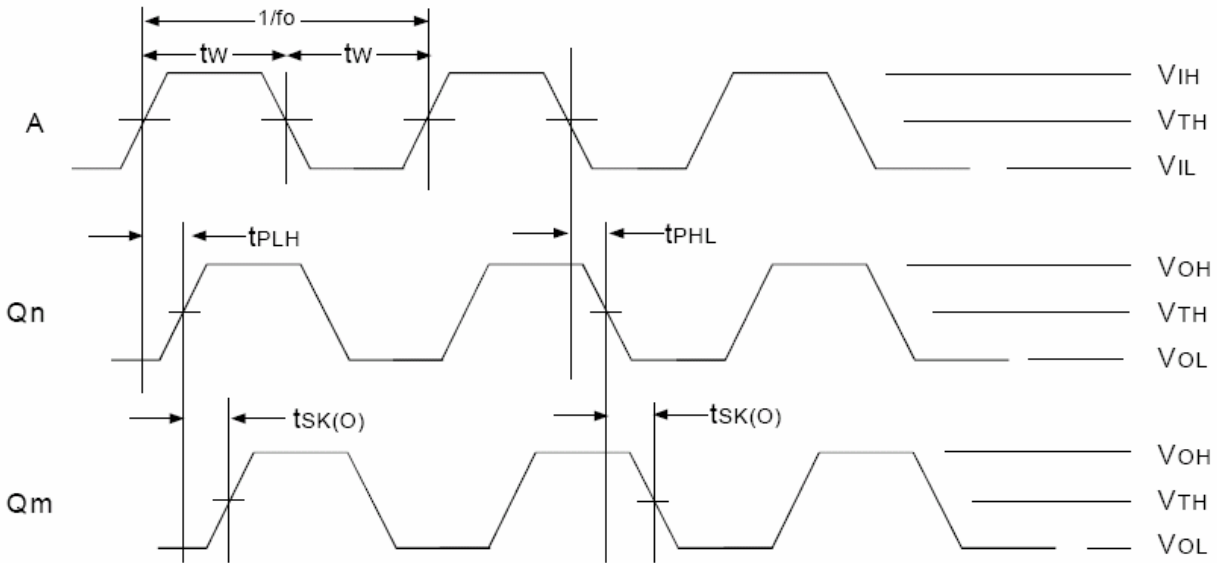
AC Electrical Characteristics Over Operating Range⁴

Symbol	Parameter	Min	Typ	Max	Unit
Skew Parameters					
t _{SK(O)}	Same Device Output Pin-to-Pin Skew ¹			25	pS
t _{SK(P)}	Pulse Skew ²			300	pS
t _{SK(PP)}	Part-to-Part Skew ³			300	pS
Propagation Delay					
t _{PLH} t _{PHL}	Propagation Delay A to Qn			1.8	nS
t _R	Output Rise Time (20% to 80%)	350		850	pS
t _F	Output Fall Time (20% to 80%)	350		850	pS
f _O	Frequency Range			200	MHz
Output Gate Enable/Disable Delay					
t _{PGE}	Output Gate Enable to Qn			3.5	nS
t _{PGD}	Output Gate Enable to Qn Driven to GL Designated Level			3	nS

NOTES:

1. Skew measured between all outputs under identical input and output transitions and load conditions on any one device.
2. Skew measured is the difference between propagation delay times t_{PHL} and t_{PLH} of any output under identical input and output transitions and load conditions on any one device.
3. Skew measured is the magnitude of the difference in propagation times between any outputs of two devices, given identical transitions and load conditions at identical V_{DD} levels and temperature.
4. Guaranteed by design.

AC Timing Waveforms



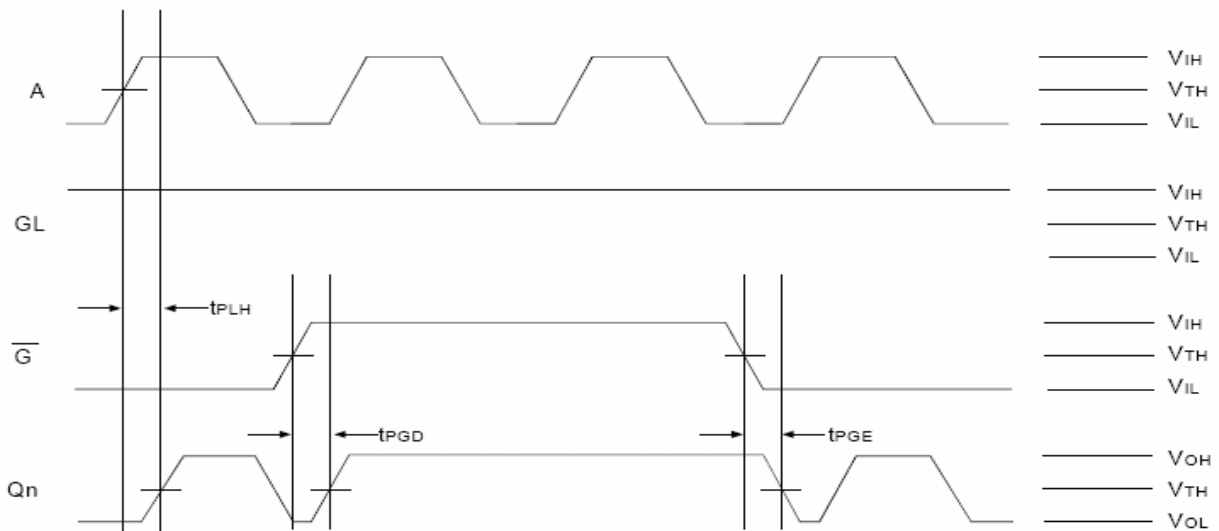
Propagation and Skew Waveforms

NOTE:

Pulse Skew is calculated using the following expression:

$t_{SK(P)} = |t_{PHL} - t_{PLH}|$ where t_{PHL} and t_{PLH} are measured on the controlled edges of any one output from rising and falling edges of a single pulse.

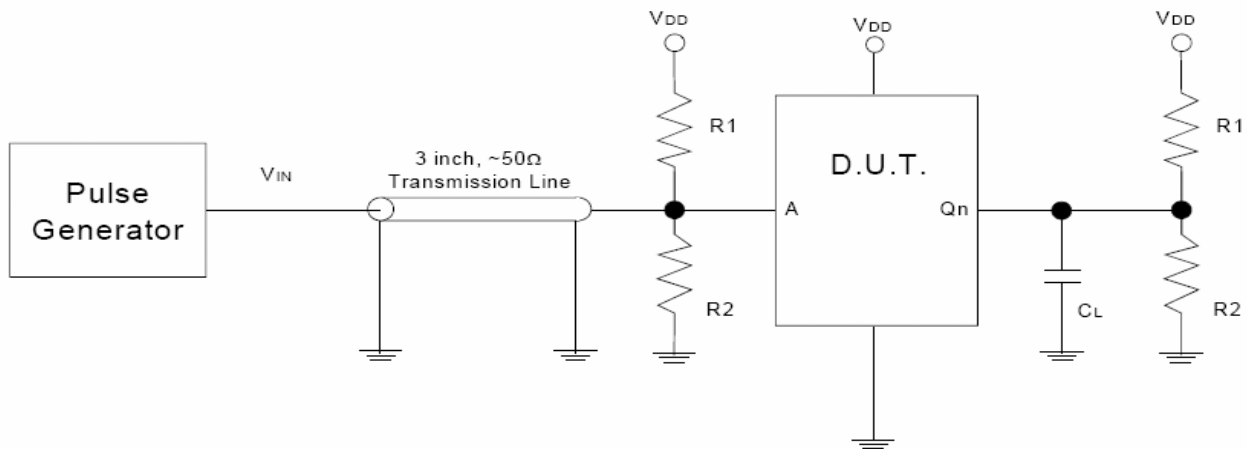
Please note that the t_{PHL} and t_{PLH} shown are not valid measurements for this calculation because they are not taken from the same pulse.



Gate Disable/Enable Showing Runt Pulse Generation

NOTE: As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their G signal to avoid this problem.

Test Circuit and Conditions



Test Circuit for Input/Output

Input/Output Test Conditions

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
V_{TH}	$V_{DD} / 2$	V
R1	100	Ω
R2	100	Ω
C_L	15	pF

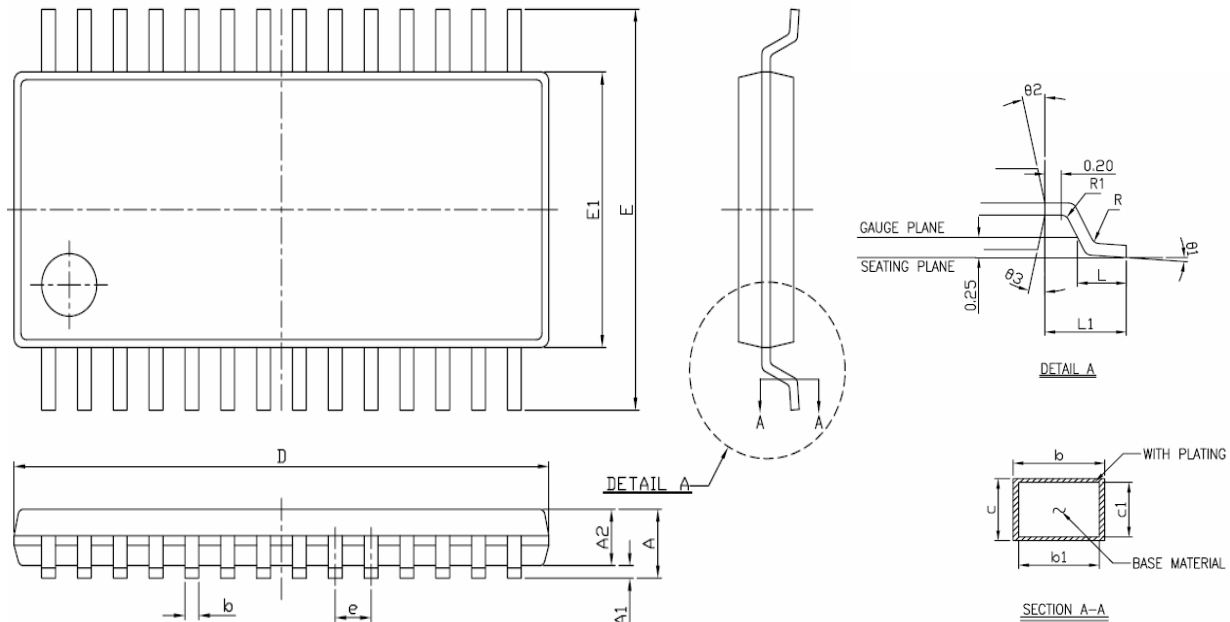
PRELIMINARY

November 2006

rev 0.2

Package Diagram

28L TSSOP (173 mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.043	...	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.031	0.041	0.80	1.05
D	0.3779	0.3858	9.60	9.80
L	0.020	0.030	0.50	0.75
E	0.252 BSC		6.40 BSC	
E1	0.169	0.177	4.30	4.50
R	0.004	0.09
R1	0.004	0.09
b	0.007	0.012	0.19	0.30
b1	0.007	0.010	0.19	0.25
c	0.004	0.008	0.09	0.20
c1	0.004	0.006	0.09	0.16
L1	0.039 REF		1.0 REF	
e	0.026 BSC		0.65 BSC	
theta 1	0°	8°	0°	8°
theta 2	12° REF		12° REF	
theta 3	12° REF		12° REF	

Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS2P5T9050AF-28TT	2P5T9050AF	28 Pin TSSOP, Tube, Pb Free	Commercial
PCS2P5T9050AF-28TR	2P5T9050AF	28 Pin TSSOP, Tape and Reel, Pb Free	Commercial
PCS2I5T9050AF-28TT	2I5T9050AF	28 Pin TSSOP, TUBE, Pb Free	Industrial
PCS2I5T9050AF-28TR	2I5T9050AF	28 Pin TSSOP, Tape and Reel, Pb Free	Industrial
PCS2P5T9050AG-28TT	2P5T9050AG	28 Pin TSSOP, Tube, Green	Commercial
PCS2P5T9050AG-28TR	2P5T9050AG	28 Pin TSSOP, Tape and Reel, Green	Commercial
PCS2I5T9050AG-28TT	2I5T9050AG	28 Pin TSSOP, TUBE, Green	Industrial
PCS2I5T9050AG-28TR	2I5T9050AG	28 Pin TSSOP, Tape and Reel, Green	Industrial

Ordering Information

P C S 2 P 5 T 9 0 5 0 A F - 2 8 T R

OR – TSOT23 -6, T/R TT – TSSOP, TUBE TR – TSSOP, T/R VT – TVSOP, TUBE VR – TVSOP, T/R ST – SOIC, TUBE AR – SSOP, T/R AT – SSOP, TUBE	SR – SOIC, T/R QR – QFN, T/R QT – QFN, TRAY BT – BGA, TRAY BR – BGA, T/R UR – SOT-23, T/R DR – QSOP, T/R DT – QSOP, TUBE
PIN COUNT	
LEAD FREE PART	
F = LEAD FREE AND RoHS COMPLIANT PART G = GREEN PACKAGE, LEAD FREE, and RoHS	
X = Automotive (-40C to +125C) I = Industrial (-40C to +85C) P or n/c = Commercial (0C to +70C)	
1 – reserved 2 – Non PLL based 3 – EMI Reduction 4 – DDR support products 5 – STD Zero Delay Buffer	6 – power management 7 – power management 8 – power management 9 – Hi performance 0 – reserved
PulseCore Semiconductor Mixed Signal Product	

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200
Campbell, CA 95008
Tel: 408-879-9077
Fax: 408-879-9018
www.pulsecoresemi.com

Copyright © PulseCore Semiconductor
All Rights Reserved
Preliminary Information
Part Number: PCS2P5T9050
Document Version: 0.2

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

© Copyright 2006 PulseCore Semiconductor Corporation. All rights reserved. Our logo and name are trademarks or registered trademarks of PulseCore Semiconductor. All other brand and product names may be the trademarks of their respective companies. PulseCore reserves the right to make changes to this document and its products at any time without notice. PulseCore assumes no responsibility for any errors that may appear in this document. The data contained herein represents PulseCore's best data and/or estimates at the time of issuance. PulseCore reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warranty to any user or customer. PulseCore does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of PulseCore products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in PulseCore's Terms and Conditions of Sale (which are available from PulseCore). All sales of PulseCore products are made exclusively according to PulseCore's Terms and Conditions of Sale. The purchase of products from PulseCore does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of PulseCore or third parties. PulseCore does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of PulseCore products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify PulseCore against all claims arising from such use..