# 2.5V Single Data Rate1:5 Clock Buffer Terabuffer

## Features

- Optimized for 2.5V LVTTL
- Guaranteed Low Skew < 25pS (max)
- Very low duty cycle distortion< 300pS (max)
- High speed propagation delay < 1.8nS. (max)
- Up to 200MHz operation
- Very low CMOS power levels
- Hot Insert able and over-voltage tolerant inputs
- 1:5 fan-out buffer
- 2.5V Supply Voltage
- Available in TSSOP Package

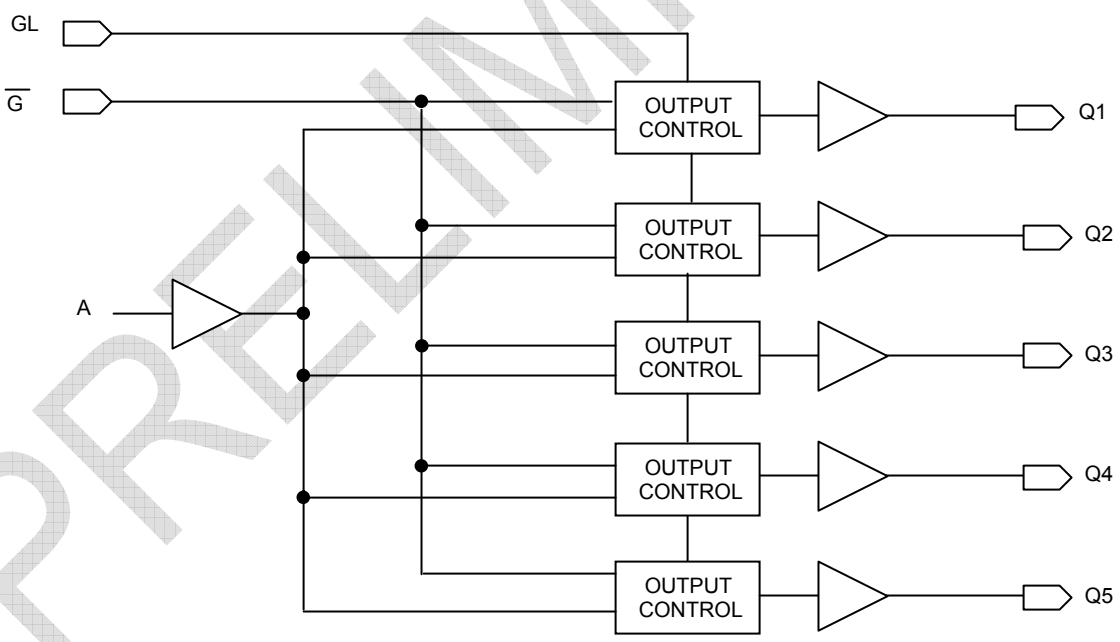
The PCS2P5T9050A 2.5V single data rate (SDR) clock buffer is a single-ended input to five single-ended outputs buffer built on advanced metal CMOS technology. The SDR clock buffer fan-out from a single input to five single-ended outputs reduces the loading on the preceding driver and provides an efficient clock distribution network. Multiple power and grounds reduce noise.

## Applications:

PCS2P5T9050A is targeted towards Clock and signal distribution applications.

## Functional Description

## Block Diagram



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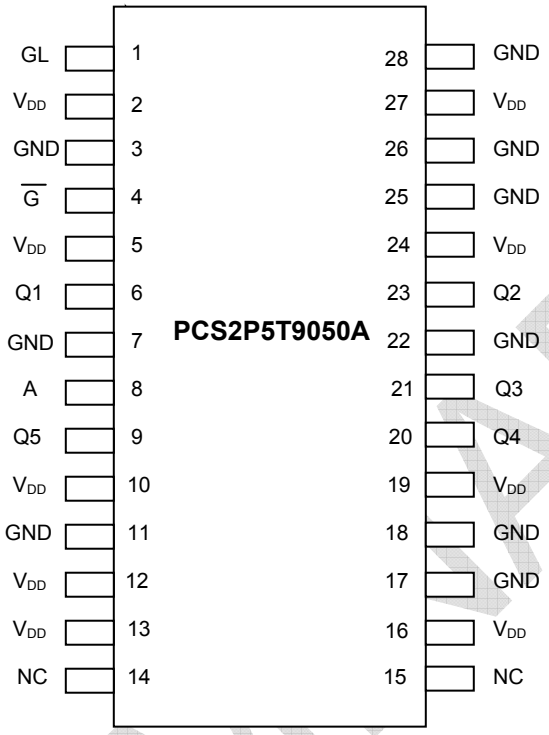
## Pin Configuration- Top View – TSSOP Package




## Pin Description

| Symbol | I/O | Type | Description |
|---|---|---|---|
| A | I | LVTTL | Clock input |
| $\overline{G}$ | I | LVTTL | Gate control for Qn outputs. When $\overline{G}$ is LOW, these outputs are enabled. When $\overline{G}$ is HIGH, these outputs are asynchronously disabled to the level designated by GL[1]. |
| GL | I | LVTTL | Specifies output disable level. If HIGH, the outputs disable HIGH. If LOW, the outputs disable LOW. |
| Qn | O | LVTTL | Clock outputs |
| $V_{DD}$ | | PWR | Power supply for the device core, inputs, and outputs |
| GND | | PWR | Power supply return for power |

**NOTE:**
1. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.

## Absolute Maximum Ratings

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | -0.5 to +3.6 | V |
| $V_I$ | Input Voltage | -0.5 to +3.6 | V |
| $V_O$ | Output Voltage | -0.5 to $V_{DD}$ +0.5 | V |
| $T_{STG}$ | Storage Temperature | -65 to +165 | °C |
| $T_J$ | Junction Temperature | 150 | °C |

Note:
1. These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

## Capacitance[1] ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 6 | | pF |

NOTE:
1. This parameter is measured at characterization but not tested.

## Recommended Operating Range

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | -40 | +25 | +85 | ° C |
| $V_{DD}$ | Internal Power Supply Voltage | 2.3 | 2.5 | 2.7 | V |

## DC Electrical Characteristics Over Operating Range[1]

| Symbol | Parameter | Test Conditions | Min | Typ[4] | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | $V_{DD}$= 2.7V $V_I = V_{DD}$/GND | | | ±5 | µA |
| $I_{IL}$ | Input LOW Current | $V_{DD}$= 2.7V $V_I$ = GND/$V_{DD}$ | | | ±5 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{DD}$= 2.3V, $I_{IN}$= -18mA | | -0.7 | - 1.2 | V |
| $V_{IN}$ | DC Input Voltage | | -0.3 | | +3.6 | V |
| $V_{IH}$ | DC Input HIGH[2] | | 1.7 | | | V |
| $V_{IL}$ | DC Input LOW[3] | | | | 0.7 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$= -12mA | $V_{DD}$- 0.4 | | | V |
| | | $I_{OH}$= -100µA | $V_{DD}$- 0.1 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$= 12mA | | | 0.4 | V |
| | | $I_{OL}$= 100µA | | | 0.1 | V |

NOTES:
1. See RECOMMENDED OPERATING RANGE table.
2. Voltage required to maintain a logic HIGH.
3. Voltage required to maintain a logic LOW.
4. Typical values are at $V_{DD}$ = 2.5V, +25°C ambient.

## Power Supply Characteristics

| Symbol | Parameter | Test Conditions[1] | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDQ}$ | Quiescent $V_{DD}$ Power Supply Current | $V_{DD}$= Max., Reference Clock = LOW<br>Outputs enabled, All outputs unloaded | 1 | 1.5 | mA |
| $I_{DDD}$ | Dynamic $V_{DD}$ Power Supply Current per Output | $V_{DD}$= Max., $C_L$= 0pF | 100 | 150 | µA/MHz |
| $I_{TOT}$ | Total Power $V_{DD}$ Supply Current | $V_{DD}$= 2.5V., $F_{REFERENCE\ CLOCK}$ = 100MHz, $C_L$= 15pF | 50 | 65 | mA |
| | | $V_{DD}$= 2.5V., $F_{REFERENCE\ CLOCK}$ = 200MHz, $C_L$= 15pF | 75 | 100 | |

NOTE:
1. The termination resistors are excluded from these measurements.

### Input AC Test Conditions

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | $V_{DD}$ | V |
| $V_{IL}$ | Input LOW Voltage | 0 | V |
| $V_{TH}$ | Input Timing Measurement Reference Level[1] | $V_{DD}/2$ | V |
| $t_R$, $t_F$ | Input Signal Edge Rate[2] | 2 | V/nS |

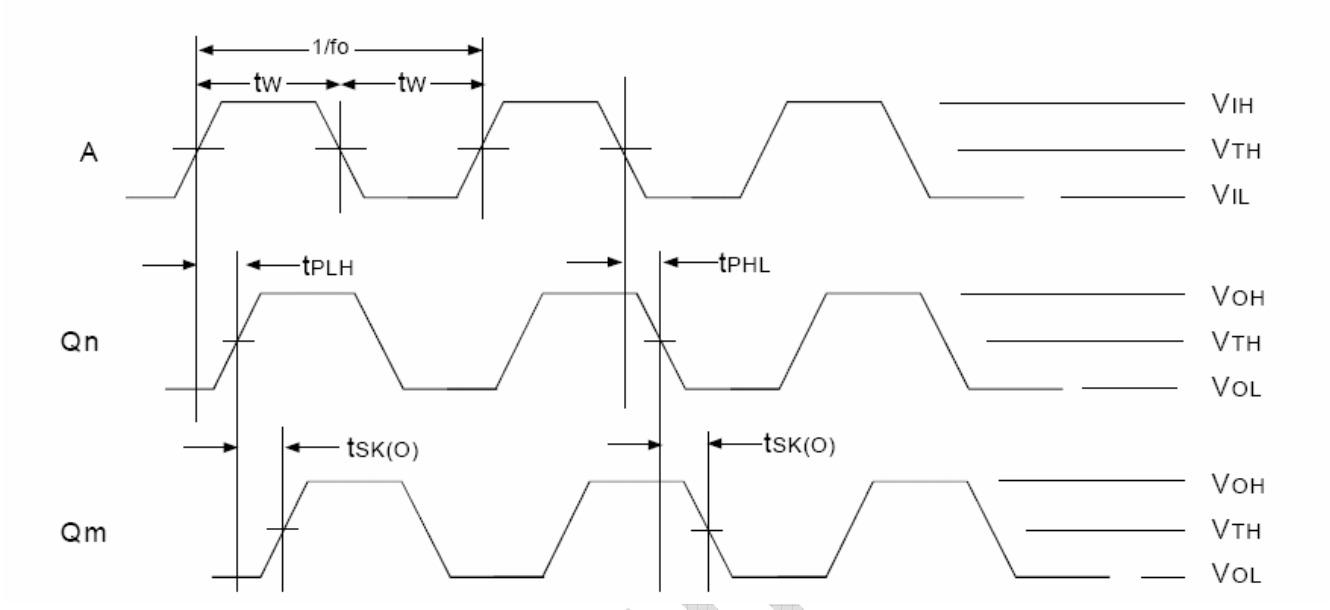
NOTES:
1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
2. The input signal edge rate of 2V/nS or greater is to be maintained in the 10% to 90% range of the input waveform.

### AC Electrical Characteristics Over Operating Range[4]

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Skew Parameters** | | | | | |
| $t_{SK(O)}$ | Same Device Output Pin-to-Pin Skew[1] | | | 25 | pS |
| $t_{SK(P)}$ | Pulse Skew[2] | | | 300 | pS |
| $t_{SK(PP)}$ | Part-to-Part Skew[3] | | | 300 | pS |
| **Propagation Delay** | | | | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay A to Qn | | | 1.8 | nS |
| $t_R$ | Output Rise Time (20% to 80%) | 350 | | 850 | pS |
| $t_F$ | Output Fall Time (20% to 80%) | 350 | | 850 | pS |
| $f_O$ | Frequency Range | | | 200 | MHz |
| **Output Gate Enable/Disable Delay** | | | | | |
| $t_{PGE}$ | Output Gate Enable to Qn | | | 3.5 | nS |
| $t_{PGD}$ | Output Gate Enable to Qn Driven to GL Designated Level | | | 3 | nS |

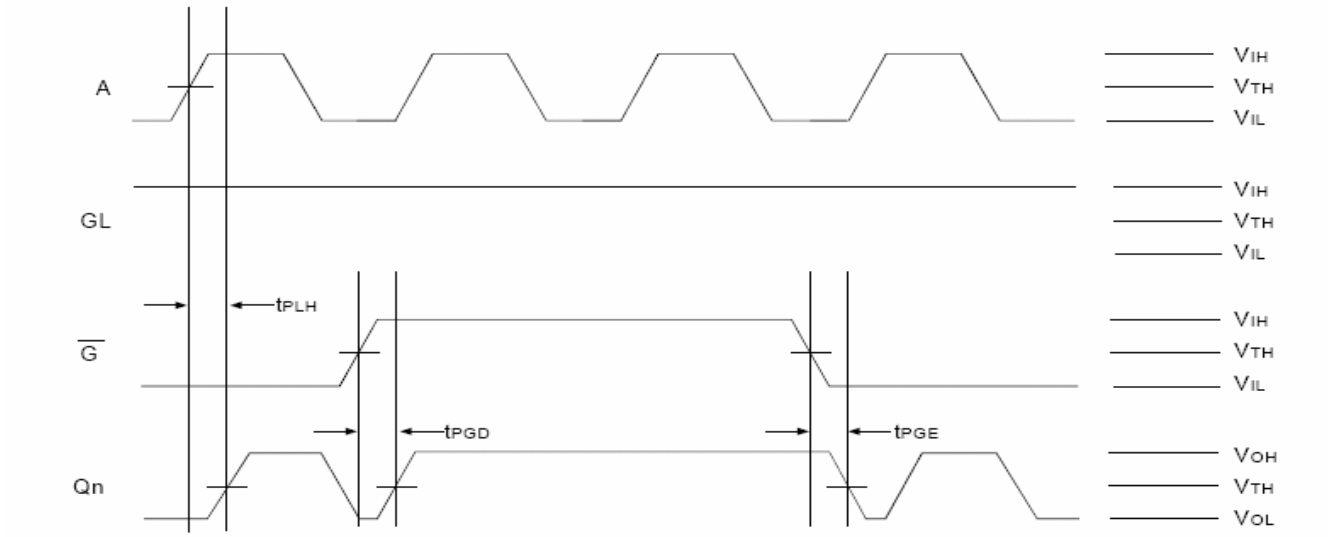
NOTES:
1. Skew measured between all outputs under identical input and output transitions and load conditions on any one device.
2. Skew measured is the difference between propagation delay times $t_{PHL}$ and $t_{PLH}$ of any output under identical input and output transitions and load conditions on any one device.
3. Skew measured is the magnitude of the difference in propagation times between any outputs of two devices, given identical transitions and load conditions at identical $V_{DD}$ levels and temperature.
4. Guaranteed by design.

### AC Timing Waveforms




**Propagation and Skew Waveforms**

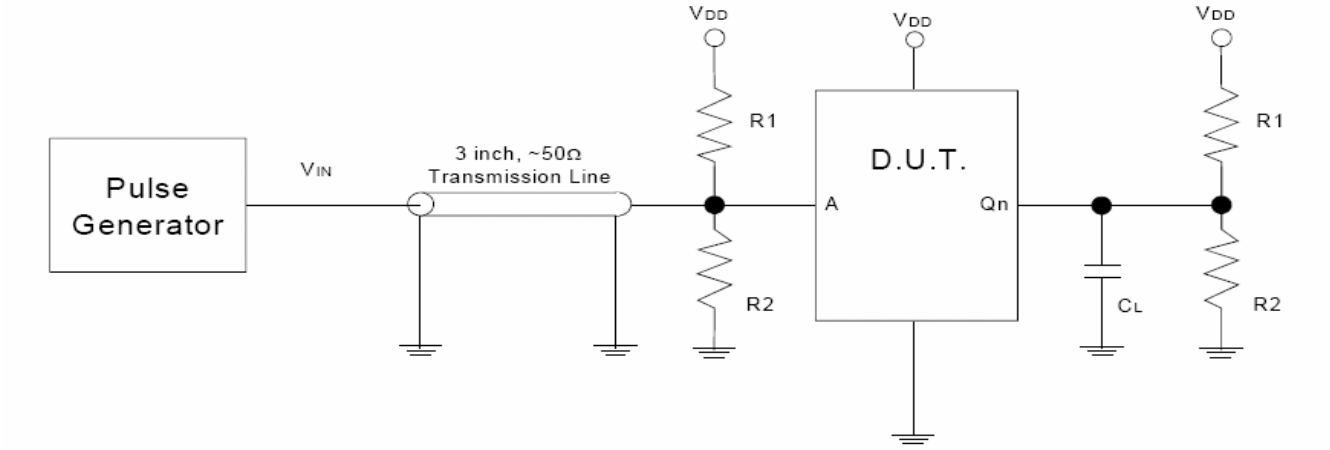
NOTE:
Pulse Skew is calculated using the following expression:
$t_{SK(P)} = | t_{PHL} - t_{PLH} |$ where $t_{PHL}$ and $t_{PLH}$ are measured on the controlled edges of any one output from rising and falling edges of a single pulse.
Please note that the $t_{PHL}$ and $t_{PLH}$ shown are not valid measurements for this calculation because they are not taken from the same pulse.




**Gate Disable/Enable Showing Runt Pulse Generation**

NOTE: As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their $\overline{G}$ signal to avoid this problem.

### Test Circuit and Conditions



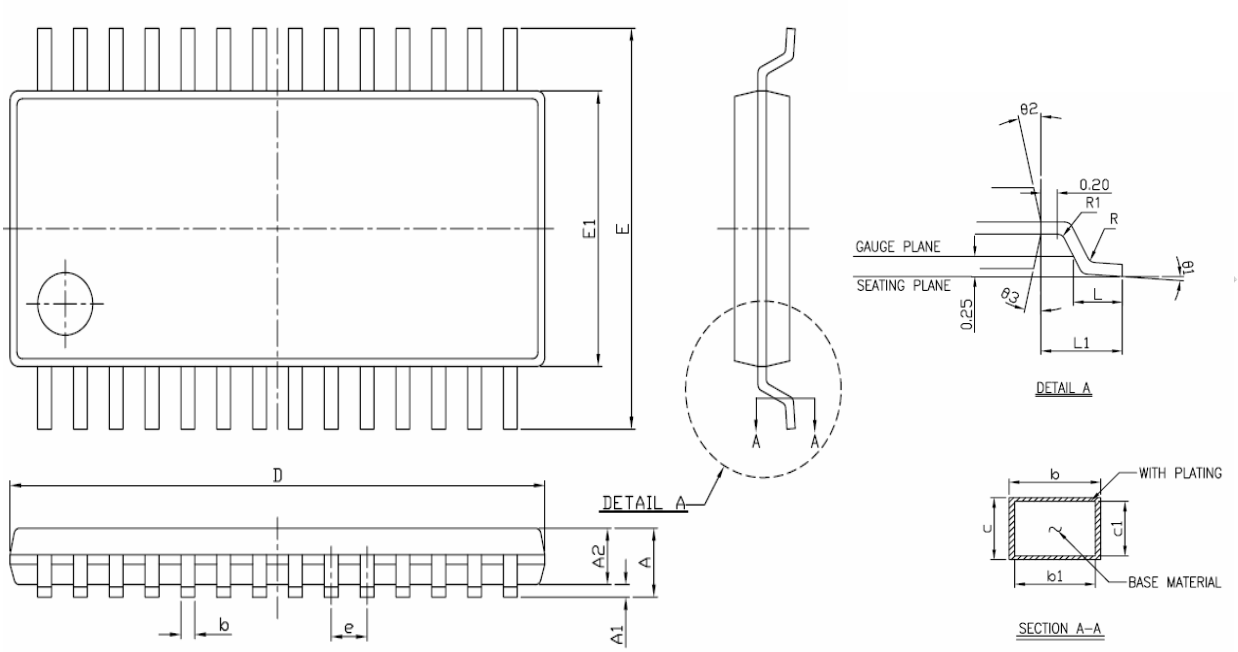

**Test Circuit for Input/Output**

### Input/Output Test Conditions

| Symbol | $V_{DD}$= 2.5V ± 0.2V | Unit |
|---|---|---|
| $V_{TH}$ | $V_{DD}$/ 2 | V |
| R1 | 100 | Ω |
| R2 | 100 | Ω |
| $C_L$ | 15 | pF |

**Package Diagram**

**28L TSSOP (173 mil)**

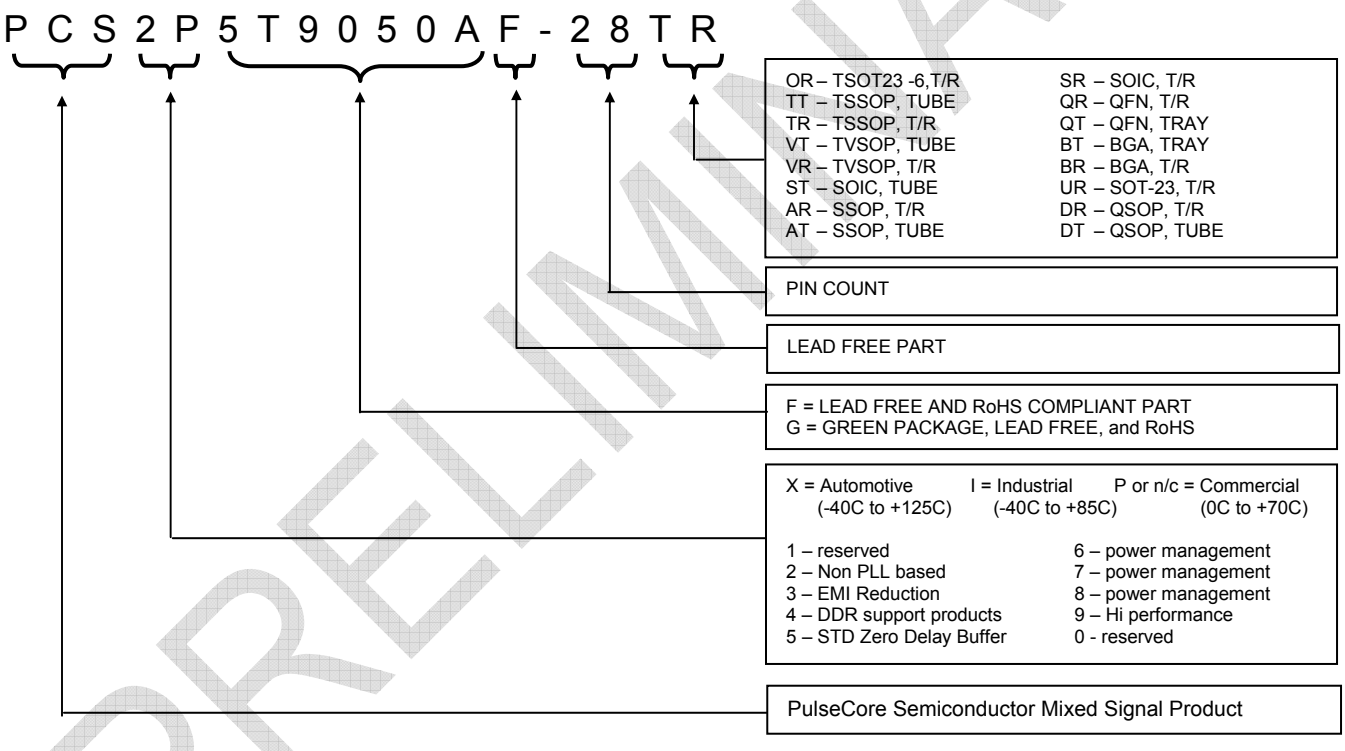



| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | …. | 0.043 | … | 1.2 |
| A1 | 0.0020 | 0.0059 | 0.05 | 0.15 |
| A2 | 0.031 | 0.041 | 0.80 | 1.05 |
| D | 0.3779 | 0.3858 | 9.60 | 9.80 |
| L | 0.020 | 0.030 | 0.50 | 0.75 |
| E | 0.252 BSC | | 6.40 BSC | |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 |
| R | 0.004 | …. | 0.09 | ….. |
| R1 | 0.004 | …. | 0.09 | ….. |
| b | 0.007 | 0.012 | 0.19 | 0.30 |
| b1 | 0.007 | 0.010 | 0.19 | 0.25 |
| c | 0.004 | 0.008 | 0.09 | 0.20 |
| c1 | 0.004 | 0.006 | 0.09 | 0.16 |
| L1 | 0.039 REF | | 1.0 REF | |
| e | 0.026 BSC | | 0.65 BSC | |
| θ1 | 0° | 8° | 0° | 8° |
| θ2 | 12° REF | | 12° REF | |
| θ3 | 12° REF | | 12° REF | |

## Ordering Information

| Part Number | Marking | Package Type | Operating Range |
|---|---|---|---|
| PCS2P5T9050AF-28TT | 2P5T9050AF | 28 Pin TSSOP, Tube, Pb Free | Commercial |
| PCS2P5T9050AF-28TR | 2P5T9050AF | 28 Pin TSSOP, Tape and Reel, Pb Free | Commercial |
| PCS2I5T9050AF-28TT | 2I5T9050AF | 28 Pin TSSOP, TUBE, Pb Free | Industrial |
| PCS2I5T9050AF-28TR | 2I5T9050AF | 28 Pin TSSOP, Tape and Reel, Pb Free | Industrial |
| PCS2P5T9050AG-28TT | 2P5T9050AG | 28 Pin TSSOP, Tube, Green | Commercial |
| PCS2P5T9050AG-28TR | 2P5T9050AG | 28 Pin TSSOP, Tape and Reel, Green | Commercial |
| PCS2I5T9050AG-28TT | 2I5T9050AG | 28 Pin TSSOP, TUBE, Green | Industrial |
| PCS2I5T9050AG-28TR | 2I5T9050AG | 28 Pin TSSOP, Tape and Reel, Green | Industrial |

## Ordering Information



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003