STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	0.3A Low Dropout Voltage Regulator with Shut Down Switch（Adjustable Voltage）
PRODUCT SERIES	**BA3662CP-V5**
FEATURES	Maximum Output Current : 300mA High Input Voltage : 35V, Built in Over Voltage Protection

○ABSOLUTE MAXIMUM RATINGS（Ta=25℃）

Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	-0.3 ～ +35 ※1	V
Output Control Voltage	V_{CTL}	-0.3 ～ Vcc	V
Power Dissipation (TO220CP-V5)	Pd	2000 ※2	mW
Operating Temperature Range	Topr	-40 ～ +125	℃
Storage Temperature Range	Tstg	-55 ～ +150	℃
Maximum Junction Temperature	Tjmax	150	℃
Peak Supply Voltage	Vcc peak	50 ※3	V

※1 Do not however exceed Pd.
※2 Derating in done at 16mW/℃ for operating above Ta≧25℃.（without heat sink）
※3 Bias voltage in 200msec (tr≧1msec).

○OPERATING CONDITIONS（Ta=-40～+125℃, however do not exceed Pd.）

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	4.0	25.0	V
Output Current	Io	－	0.3	A
Output Voltage	Vo	3	15	V

○PROTECTION（Design Guarantee）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Over Voltage Protection	Vcc	26	28	30	V

NOTE : This product is not designed for protection against radioactive rays.

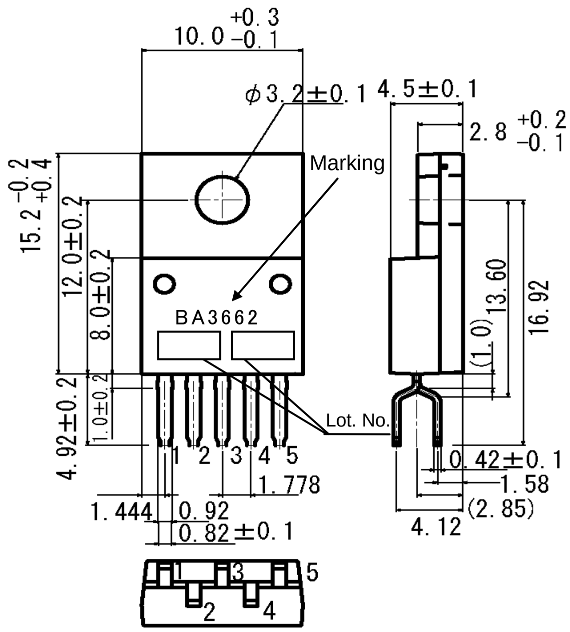
○ELECTRICAL CHARACTERISTIC

(Unless otherwise specified, Ta=25℃、Vcc=10V、V_{CTL}=5V、Io=200mA、Vo=5V Setting)

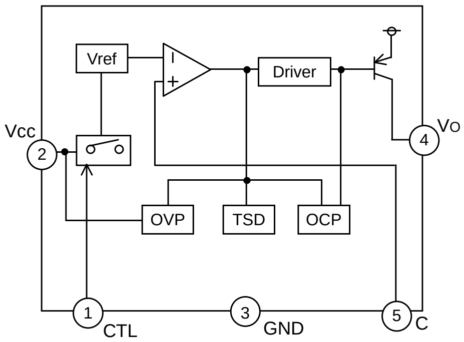
Parameter	Symbol	Limit			Umit	Conditions
		Min.	Typ.	Max.		
Shut Down Current	Isd	―	0	10	μA	V_{CTL}=0V
Bias Current	Ib	―	2.5	5.0	mA	V_{CTL}=2V, Io=0mA
C Terminal Voltage	Vc	1.200	1.225	1.250	V	Io=50mA
Dropout Voltage	⊿Vd	―	0.3	0.5	V	Vcc=Vo×0.95
Peak Output Current	Io	0.3	―	―	A	
Ripple Rejection	R.R.	45	55	―	dB	f=120Hz,ein※1=1Vrms, Io=100mA
Line Regulation	Reg.I	―	20	100	mV	Vcc=6→25V
Load Regulation	Reg.L	―	40	80	mV	Io=5mA→200mA
Temperature Coefficient of Output Current	Tcvo	―	±0.02	―	%/℃	Io=5mA,Tj=0～125℃
Output Short Current	Ios	―	0.1	―	A	Vcc=25V,Vo=0V
ON Mode Voltage	VthH	2.0	―	―	V	ACTIVE MODE, Io=0mA
OFF Mode Voltage	VthL	―	―	0.8	V	OFF MODE, Io=0mA
Input High Current	I_{CTL}	100	200	300	μA	V_{CTL}=5V, Io=0mA

※1 ein : Input Voltage Ripple

○PHYSICAL DIMENSIONS, MARKING



○ BLOCK DIAGRAM



○PIN NO. , PIN NAME

Pin Number	Pin Name
1	CTL
2	Vcc
3	GND
4	VO
5	C

○NOTES FOR USE

1. Absolute maximum range
Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed we cannot be defined the failure mode, such as short mode or open mode.
Therefore physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.

3. GND pin voltage
GND terminal should be connected the lowest voltage, under all conditions. And all terminals except GND should be under GND terminal voltage under all conditions including transient situations.

4. GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid voltage fluctuations in any connected external component GND.

5. Be sure to connect a capacitor with capacitance of at least 22μF, including temperature characteristics and variation, to prevent oscillation between the Vo and GND. Note that if the capacity of the capacitor changes due to factors such as changes in temperature or ESR, oscillation may occur, and the original characteristics of the IC may not be realized. For example, when a ceramic capacitor is employed, oscillation will be generated because the series resistance is too small. Please take countermeasures to prevent this, such as adding a series resistor. Standard electrolytic capacitors are subject to extremely large capacitance and ESR fluctuations due to temperature conditions. Particularly at low temperature, capacity is decreased, while ESR grows larger, conditions which increase the vulnerability to oscillation. Therefore, be certain to check for the presence of oscillation.
Keep capacitor capacitance within a range of 22μF～1000μF. It is also recommended that a 0.33μF bypass capacitor be connected as close to the input pin-GND as location possible. However, in situations such as rapid fluctuation of the input voltage or the load, please check the operation in real application to determine proper capacitance.

6. Mounting Failures
Mounting failure, such as misdirection or mismount, may cause a malfunction in the device.

7. Malfunction may be happened when the device is used in the strong electromagnetic field.

8. Precautions for board inspection
Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the test operation. To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

9. Power dissipation
If IC is used on condition that the power loss is over the power dissipation, the reliability will become worse by heat up. The power dissipation that is described to the absolute maximum rating in this specification is a value when the heat sink is not populated. In this case it exceed the power dissipation, please consider using the heat sink,etc.
Also, be sure to use this IC within a power dissipation range allowing enough of margin.

10. Thermal design
Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.

11. Over current protection circuit （OCP）
The built-in over current protection circuit is designed to respond to the output current and prevent destruction of the IC from load short circuits; however, it is only effective in protecting the IC from destruction in sudden over current accidents. The protection circuit is not to be used continuously, or for transitions. In executing thermal design, bear in mind that over current protection has negative characteristic according with the temperature.

12. Thermal shutdown circuit （TSD）
A built-in internal shutdown circuit is provided to protect the IC from heat destruction. Operation has to be done within the allowable loss range, but in continuous use beyond the range, chip temperature Tj will increase to the threshold, activating the TSD circuit and turning the output power Tr OFF. Once the chip temperature Tj returns to the normal range, the circuit is automatically restored. Note that the TSD circuit is designed to operate over the maximum absolute rating. Therefore, make absolutely certain not to use the TSD function in set design.

13. Internal circuits or elements may be damaged when Vcc and pin voltage are reversed. For example, Vcc short circuit to GND while a external capacitor is charged. Output pin capacitor is recommended no larger than 1000μF. In addition, inserting a Vcc series countercurrent prevention diode, or a bypass diode between the various pins and the vcc, is recommended.

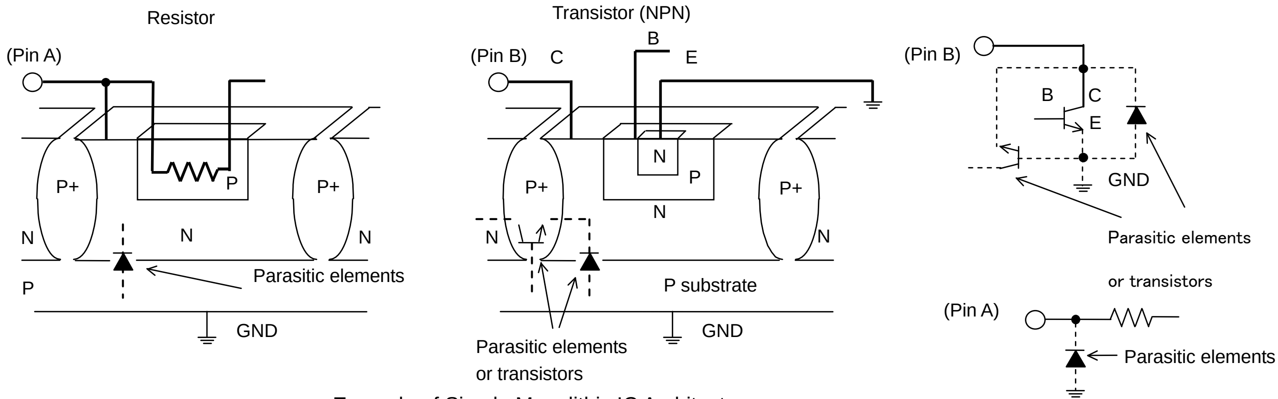
14. Positive voltage surges on Vcc pin
A power zener diode should be inserted between Vcc and GND for protection against voltage surges of more than 50V on the Vcc pin.

15. Negative voltage surges on Vcc pin
A schottky barrier diode should be inserted between Vcc and GND for protection against voltages lower than GND on the Vcc pin.

16. We recommend to put Diode for protection purpose in case of output pin connected with large load of impedance or reserve current occurred at initial and output off.

17. Regarding input pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):
- ●When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- ●When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of Simple Monolithic IC Architecture

Notes

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