

AOD4187
P-Channel Enhancement Mode Field Effect Transistor
General Description

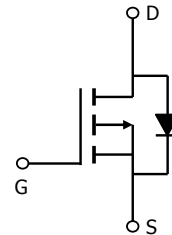
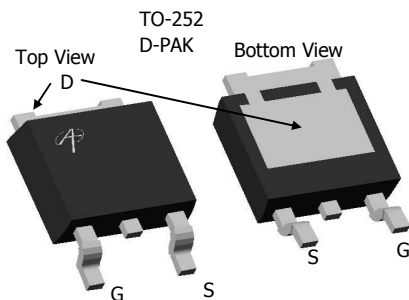
The AOD4187 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications

- RoHS Compliant
- Halogen Free*

Features

V_{DS} (V) = -40V
 I_D = -45A ($V_{GS} = -10V$)
 $R_{DS(ON)} < 17m\Omega$ ($V_{GS} = -10V$)
 $R_{DS(ON)} < 23m\Omega$ ($V_{GS} = -4.5V$)

100% UIS Tested!
100% Rg Tested!


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	-45
		$T_C=100^\circ\text{C}$	-30
Pulsed Drain Current ^C	I_{DM}	-100	A
Continuous Drain Current	I_{DSM}	$T_C=25^\circ\text{C}$	-9
		$T_C=100^\circ\text{C}$	-7
Avalanche Current ^C	I_{AR}	-36	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	65	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	60
		$T_C=100^\circ\text{C}$	30
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	2.5
		$T_A=70^\circ\text{C}$	1.6
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	41	50
Maximum Junction-to-Case	$R_{\theta JC}$	2	2.5	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-40\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.7	-1.9	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-100			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-12\text{A}$ $T_J=125^\circ\text{C}$ $V_{GS}=-4.5\text{V}$, $I_D=-8\text{A}$		14 21 18	17 26 23	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-12\text{A}$		40		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current				-50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-20\text{V}$, $f=1\text{MHz}$	1960	2350	2850	pF
C_{oss}	Output Capacitance		185	240	320	pF
C_{rss}	Reverse Transfer Capacitance		130	185	260	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	2	5.5	11	Ω
SWITCHING PARAMETERS						
$Q_{g(-10V)}$	Total Gate Charge	$V_{GS}=-10\text{V}$, $V_{DS}=-20\text{V}$, $I_D=-12\text{A}$	35	42	50	nC
$Q_{g(-4.5V)}$	Total Gate Charge		16	20	25	nC
Q_{gs}	Gate Source Charge		5.5	6.6	8	nC
Q_{gd}	Gate Drain Charge		7	9.7	14	nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-20\text{V}$, $R_L=1.6\Omega$, $R_{GEN}=3\Omega$		9.6		ns
t_r	Turn-On Rise Time			29		ns
$t_{D(off)}$	Turn-Off DelayTime			56		ns
t_f	Turn-Off Fall Time			19.2		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-12\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$	14	17	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-12\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$	40	49	60	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev 1: Oct-2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

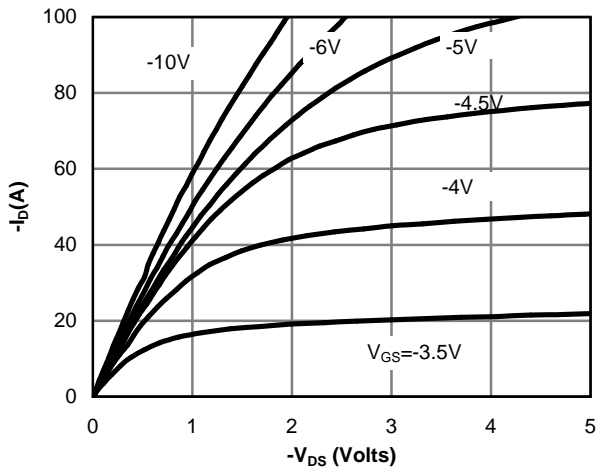


Figure 1: On-Region Characteristics

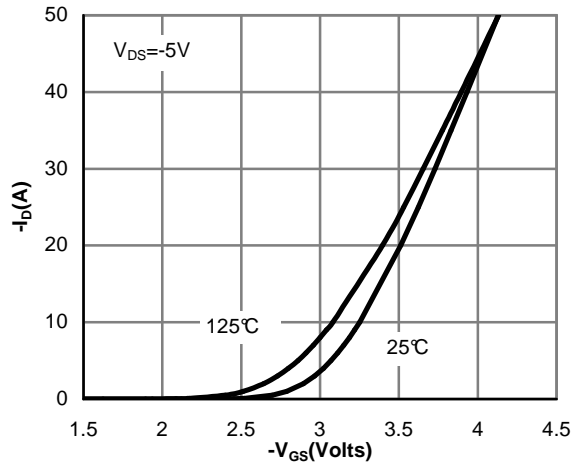


Figure 2: Transfer Characteristics

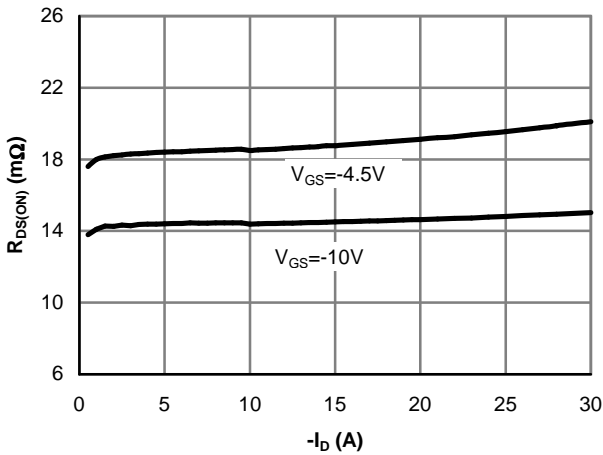


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

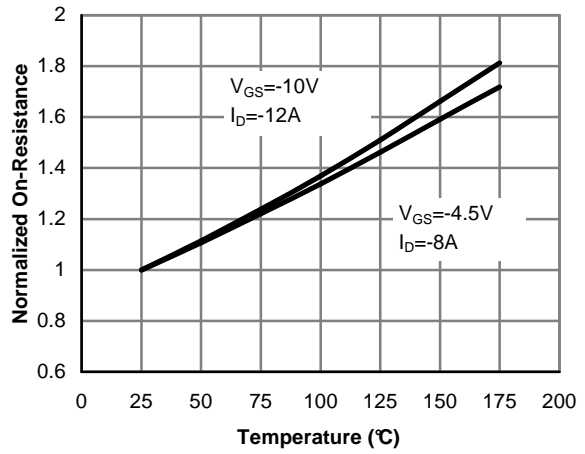


Figure 4: On-Resistance vs. Junction Temperature

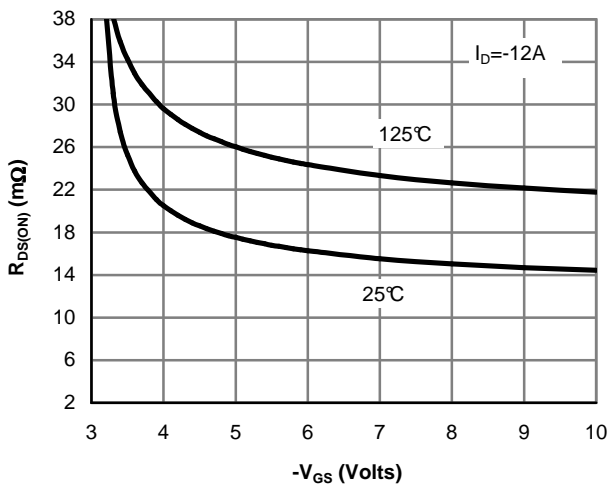


Figure 5: On-Resistance vs. Gate-Source Voltage

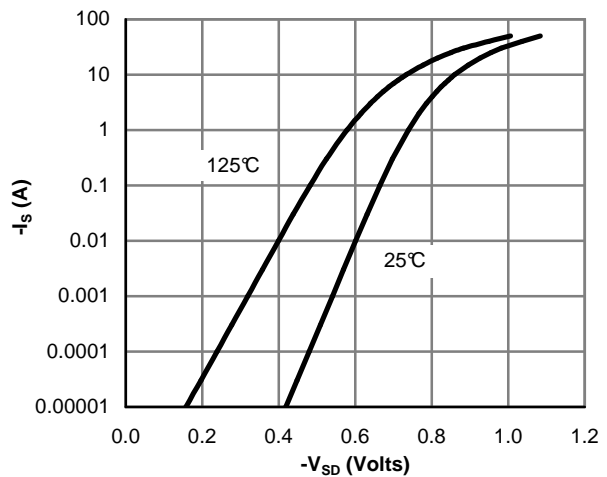


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

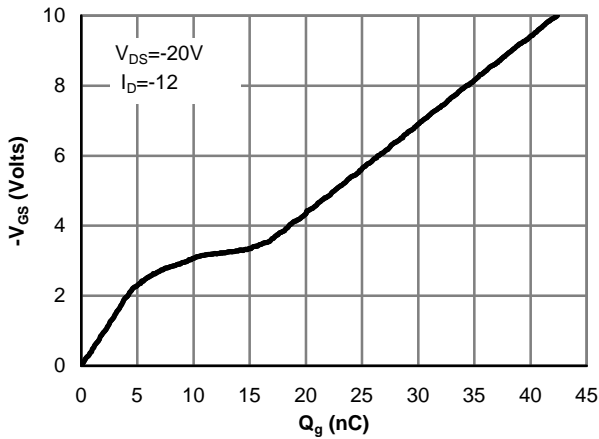


Figure 7: Gate-Charge Characteristics

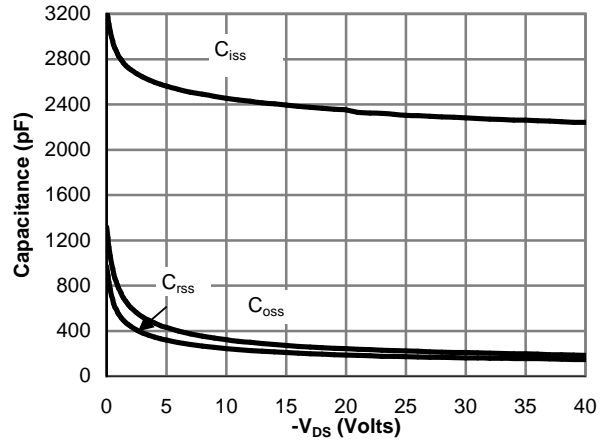


Figure 8: Capacitance Characteristics

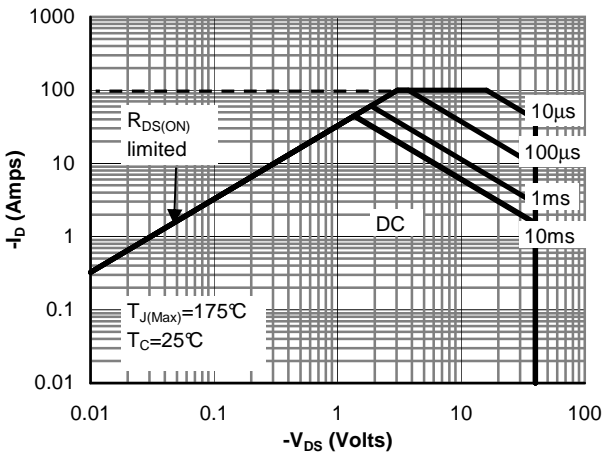


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

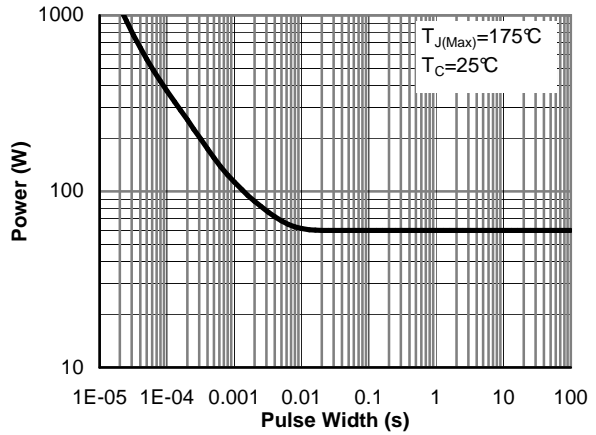


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

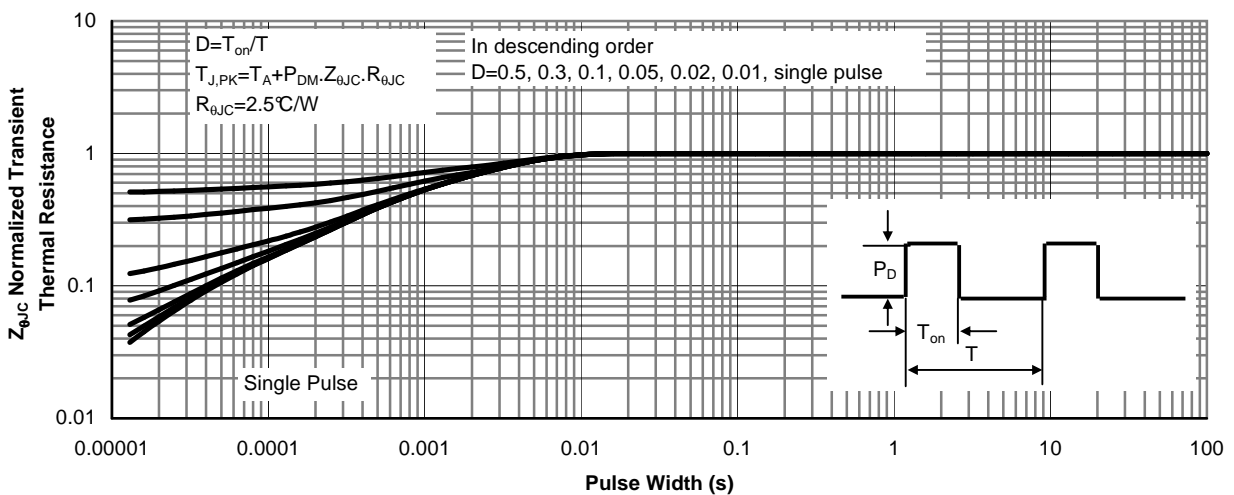


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

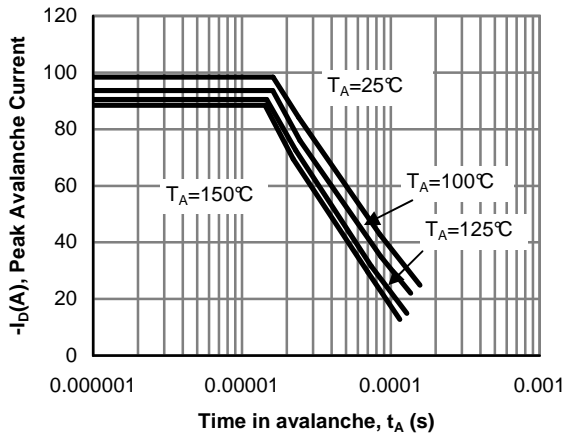


Figure 12: Single Pulse Avalanche capability

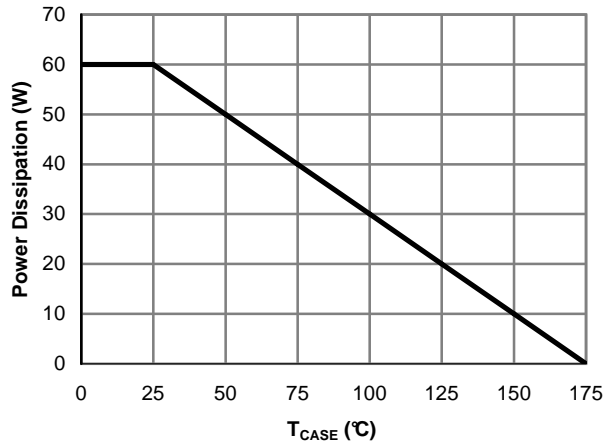


Figure 13: Power De-rating (Note F)

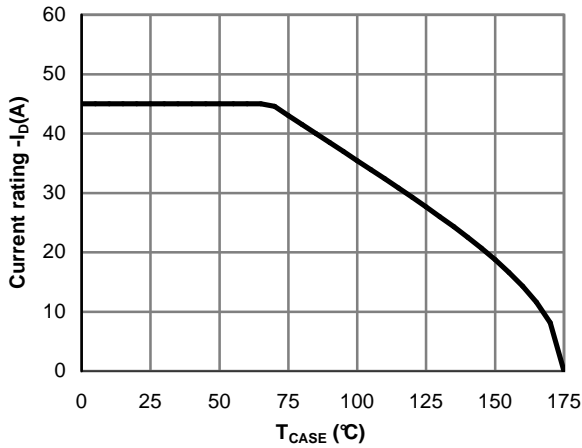


Figure 14: Current De-rating (Note F)

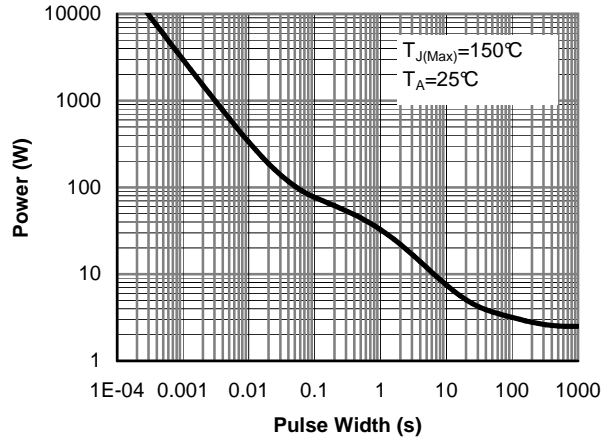


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

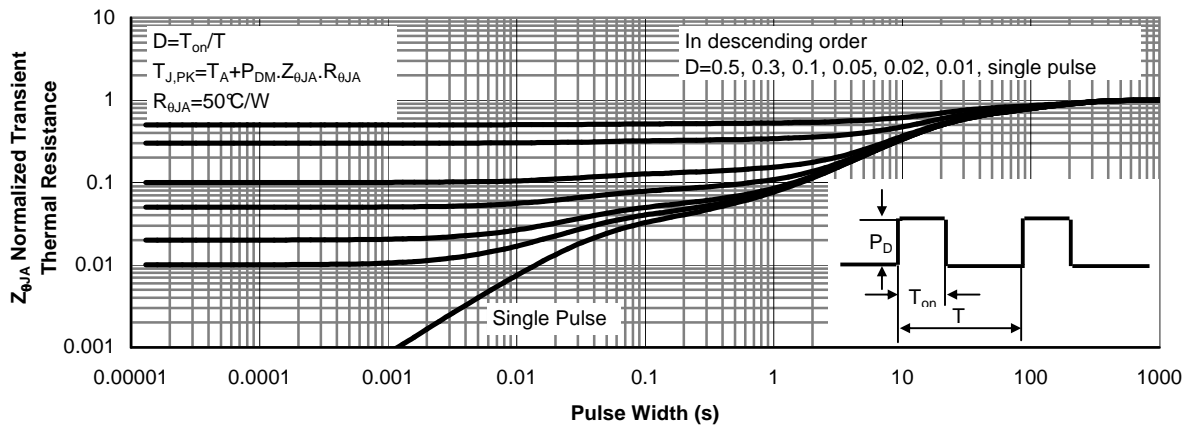
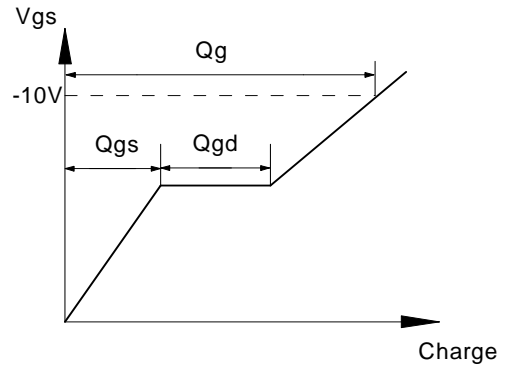
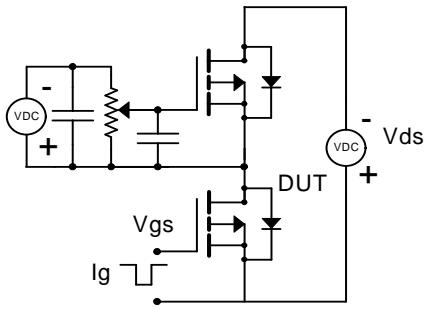
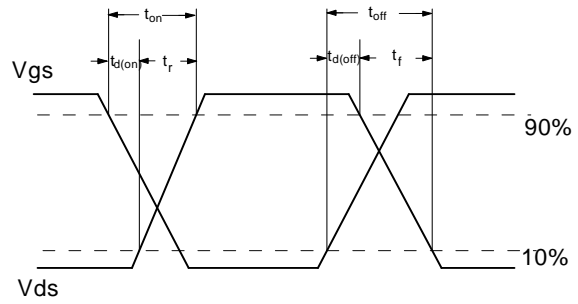
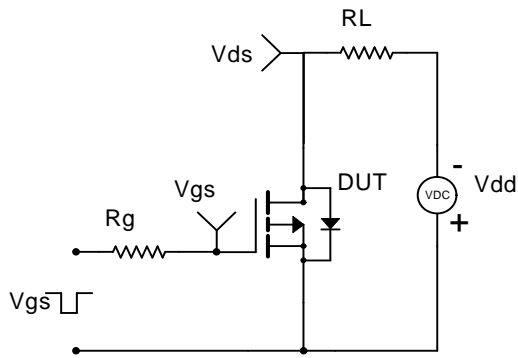


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

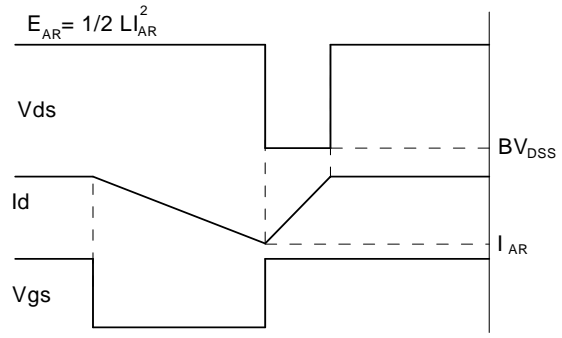
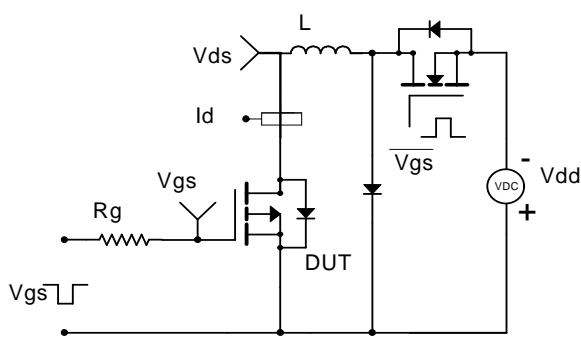
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

