Structure Silicon monolithic integrated circuit

Product Color TV signal encoder

Type **BH7240AKV**

Features Digital RGB signals (8-bit parallel) are converted into video signals.
It corresponds to both the systems of NTSC and PAL format.

○ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	AVCC1, AVCC2,DVDD	7.0	V
Power dissipation	Pd	900 *1	mW
Storage temperature range	Tstg	-55 ～ +125	℃

*1 A measured value at mounting on 50×50×1.6mm glass epoxy substrate.
In the case of exceeding Ta=25℃, 9.0mW should be reduced per 1℃.

* The radiation-resistance design is not carried out.

* Operation is not guaranteed.

○ Operating Conditions (Ta=-20～+70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	AVCC1, AVCC2,DVDD	4.5	-	5.5	V
Input "H" voltage (SYNCIN,NT/PAL)	VIH	2.2	-	5.0 *2	V
Input "L" voltage (SYNCIN,NT/PAL)	VIL	0.0	-	0.8 *2	V
Input level (SCIN)	Vsci	0.4	-	5.0	Vpp
Input "H" voltage 2 (VCLK,RDATA,GDATA,BDATA)	VIH2	2.2	-	5.0 *2	V
Input "L" voltage 2 (VCLK,RDATA,GDATA,BDATA)	VIL2	0	-	0.8 *2	V

*2 AVCC1=AVCC2=DVDD=5.0V

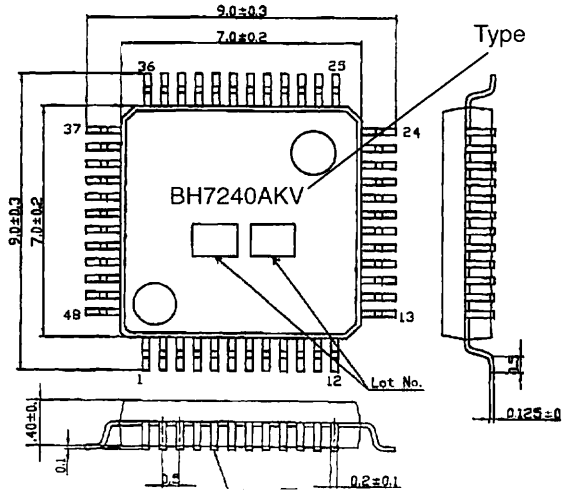
○ Electrical Characteristics (Ta=25℃, AVCC1=AVCC2=DVDD=5.0V unless otherwise noted.)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Consumption current	Icc	-	85	105	mA	RGB DATA=00h input
Luminance level (Vout,Yout)						
White level	Vlwhite	0.59	0.70	0.81	Vpp	RGB DATA=FFh input
Red level	Vlred	0.18	0.21	0.24	Vpp	R DATA=FFh input
Green level	Vlgreen	0.35	0.41	0.47	Vpp	G DATA=FFh input
Blue level	Vlblue	0.07	0.08	0.09	Vpp	B DATA=FFh input
Sync level	Vsync	0.27	0.30	0.33	Vpp	
Sync/White level ratio	Rs/w	0.37	0.43	0.49		
Chroma level (Vout,Cout)						
Red/Burst level ratio	Vcr/Vbur	2.69	3.16	3.63	-	R DATA=FFh input *3
Green/Burst level ratio	Vcg/Vbur	2.51	2.95	3.39	-	G DATA=FFh input *3
Blue/Burst level ratio	Vcb/Vbur	1.91	2.24	2.57	-	B DATA=FFh input *3
Burst level	Vbur	0.25	0.29	0.33	Vpp	*4
Red phase	θ red	94	104	114	deg	R DATA=FFh input *3
Green phase	θ green	231	241	251	deg	G DATA=FFh input *3
Blue phase	θ blue	337	347	357	deg	B DATA=FFh input *3
RGB level (Rout,Gout,Bout)						
Red level	Vrout	0.56	0.70	0.81	Vpp	R DATA=FFh input
Green level	Vgout	0.59	0.70	0.81	Vpp	G DATA=FFh input
Blue level	Vbout	0.59	0.70	0.81	Vpp	B DATA=FFh input
Others						
RGB DATA conversion frequency	Fda	-	-	20	MHz	
RGB DATA Set-up time	Tset	20	-	-	nsec	
RGB DATA hold time	Thold	20	-	-	nsec	
SYNCIN、NT/PAL Input current High	IH	-	-	300	μA	Terminal is applied to 5V.
SYNCIN、NT/PAL Input current Low	IL	-200	-	-	μA	Terminal is applied to 0V.

*3 This specification is design target.

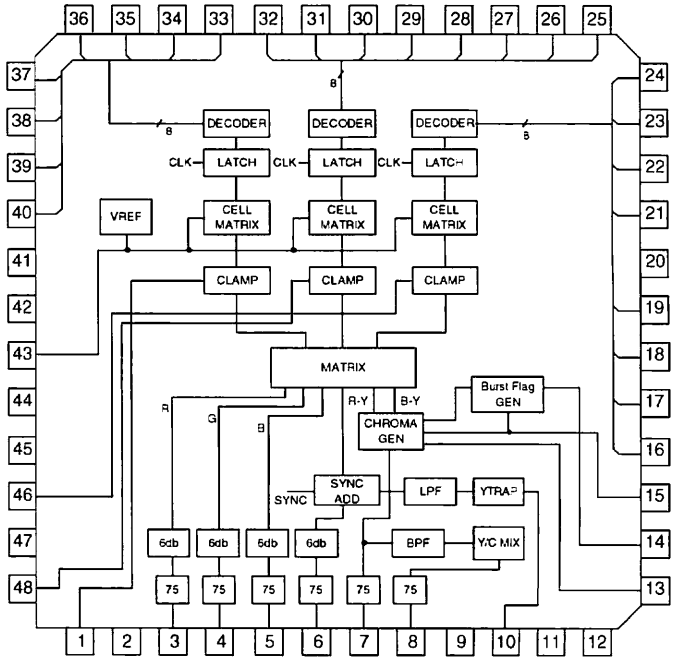
*4 This specification is measured with 3.58MHz BPF.

○ Package outline



VQFP48 (Unit : mm)

○Block diagram



○ Terminal functions

Terminal No.	Terminal name	Descriptions of terminals	Terminal No.	Terminal name	Descriptions of terminals
1	BCLAMP	Analog Blue signal clamp terminal.	25	GDATA7	Green data input terminal (bit 7)
2	AGND2	Ground terminal for 75Ω driver.	26	GDATA6	Green data input terminal (bit 6)
3	ROUT	Analog Red signal output terminal.	27	GDATA5	Green data input terminal (bit 5)
4	GOUT	Analog Green signal output terminal.	28	GDATA4	Green data input terminal (bit 4)
5	BOUT	Analog Blue signal output terminal.	29	GDATA3	Green data input terminal (bit 3)
6	YOUT	Luminance signal output terminal.	30	GDATA2	Green data input terminal (bit 2)
7	COUT	Chrominance signal output terminal.	31	GDATA1	Green data input terminal (bit 1)
8	VOUT	Composite video signal output terminal.	32	GDATA0	Green data input terminal (bit 0)
9	AVCC2	Power supply terminal for 75Ω driver.	33	BDATA7	Blue data input terminal (bit 7)
10	YTRAP	Luminance trap filter terminal.	34	BDATA6	Blue data input terminal (bit 6)
11	N.C.	No Connection	35	BDATA5	Blue data input terminal (bit 5)
12	N.C.	No Connection	36	BDATA4	Blue data input terminal (bit 4)
13	NT/PAL	Input terminal for the selection of TV form	37	BDATA3	Blue data input terminal (bit 3)
14	SYNCIN	Composite sync input terminal.	38	BDATA2	Blue data input terminal (bit 2)
15	SCIN	Color subcarrier input terminal.	39	BDATA1	Blue data input terminal (bit 1)
16	RDATA7	Red data input terminal (bit 7)	40	BDATA0	Blue data input terminal (bit 0)
17	RDATA6	Red data input terminal (bit 6)	41	VCLK	DAC clock input.
18	RDATA5	Red data input terminal (bit 5)	42	DGND	Ground terminal for digital circuits.
19	RDATA4	Red data input terminal (bit 4)	43	VREFOUT	RGBDAC reference voltage output terminal.
20	DVDD	Power supply terminal for digital circuits.	44	N.C.	No Connection
21	RDATA3	Red data input terminal (bit 3)	45	AGND1	Ground terminal for analog circuit except 75Ω driver.
22	RDATA2	Red data input terminal (bit 2)	46	RCLAMP	Analog Red signal clamp terminal.
23	RDATA1	Red data input terminal (bit 1)	47	AVCC1	Power supply terminal for analog circuit except 75Ω driver.
24	RDATA0	Red data input terminal (bit 0)	48	GCLAMP	Analog Green signal clamp terminal.

○ Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as power-supply voltage, operating temperature range, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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