Large Current External FET Controller Type Switching Regulators

# Step-down,High-frequency Switching Regulator (Controller type)

**BD63536FJ**

No.09028EAT09

## ●Description

The BD63536FJ is a gate direct drive switching regulator operational at a power supply voltage from 3V. This regulator uses a compact package SOP-J8 and operates as a switching regulator for the voltage control type of step-down DC/DC converter. The regulator features reliable design with ±1% reference voltage accuracy, built-in current limit function (±4%), and a variety of built-in protection circuits.

## ●Features

1) Gate direct drive available (External Pch FET, Vcc-5.4V)
2) Built-in current limit function (150mV±4%)
3) Built-in gate-off function
4) Error amplifier reference voltage (1.25V±1%)
5) Built-in soft start
6) 2.5V regulator output
7) External oscillation frequency variable
8) Built-in thermal shutdown circuit

## ●Applications

Laser beam printers, MFPs, PPCs, etc.

## ●Absolute maximum ratings (Ta=25°C)

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | -0.2 to 32.0 | V |
| Current detection pin | $V_{CS}$ | -0.2 to 32.0 | V |
| $V_{CC}$-$V_{CS}$ potential difference | $V_{CC}$-$V_{CS}$ | -0.2 to 5.0 | V |
| Output current (DC) | $I_{OUT}$ | 30 *1 | mA |
| Output current (peak) | $I_{OUTPEAK}$ | 200 *2 | mA |
| Power dissipation 1 | Pd1 | 563 *3 | mW |
| Power dissipation 2 | Pd2 | 675 *4 | mW |
| Operating temperature range | $T_{opr}$ | -25 to 85 | °C |
| Storage temperature range | $T_{stg}$ | -55 to 150 | °C |
| Junction temperature | $T_{jmax}$ | 150 | °C |

*1 Should not exceed Pd value.

*2 Should not exceed Pd value when Pulse width tw≤100μs and Duty≤50%.


*3 Ratings for the IC alone. To use the IC at temperatures over Ta=25°C, derate power rating by 4.5mW/°C.

*4 Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm. To use the IC at temperatures over Ta=25°C, derate power rating by 5.4mW/°C.

## ●Operating conditions (Ta=–25 to +85°C)

| Item | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Power supply voltage | $V_{CC}$ | 3 | 24 | 30 | V |
| Oscillation frequency | $F_{OSC}$ | - | - | 300 | kHz |

●**Electrical characteristics (Unless otherwise specified, Ta=25°C, $V_{CC}$ =24V)**

| Item | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **General** | | | | | | |
| Circuit current | $I_{CC}$ | - | 2 | 4 | mA | $V_{OSC}$=0V |
| **Current limit block** | | | | | | |
| Switching voltage | $V_{CL}$ | $V_{CC}$-0.156 | $V_{CC}$-0.150 | $V_{CC}$-0.144 | V | $V_{CS}$: sweep down |
| Output OFF switching voltage | $V_{OOFF}$ | $V_{CC}$-1.3 | $V_{CC}$-1.0 | $V_{CC}$-0.7 | V | $V_{CS}$: sweep down |
| CS input bias current | $I_{CS}$ | - | 0.3 | 1.0 | μA | $V_{CS}$=$V_{CC}$ |
| **Output block** | | | | | | |
| GATE H voltage | $V_{ONH}$ | $V_{CC}$-0.10 | $V_{CC}$-0.05 | - | V | $I_{GATE}$=-10mA |
| GATE L voltage | $V_{ONL}$ | $V_{CC}$-6.20 | $V_{CC}$-5.40 | $V_{CC}$-4.60 | V | $I_{GATE}$=10mA |
| **Reference voltage block** | | | | | | |
| VREF output voltage | $V_{REF}$ | 2.375 | 2.500 | 2.625 | V | $I_{VREF}$=-0.1mA |
| **Low input malfunction prevention circuit block** | | | | | | |
| Threshold voltage | $V_{UVLO}$ | 2.3 | 2.5 | 2.7 | V | $V_{CC}$: sweep up |
| Hysteresis voltage | $\Delta V_{UVLO}$ | 0.05 | 0.15 | 0.25 | V | |
| **Triangular waveform oscillator block** | | | | | | |
| Oscillation H voltage | $V_{OSH}$ | 1.26 | 1.40 | 1.54 | V | $V_{OSC}$: sweep up |
| Oscillation L voltage | $V_{OSL}$ | 0.9 | 1.0 | 1.1 | V | $V_{OSC}$: sweep down |
| **Error amplifier block** | | | | | | |
| Input bias current | $I_{IN-}$ | -0.3 | -0.1 | - | μA | IN-=0V |
| Reference voltage | $V_{IN-}$ | 1.237 | 1.250 | 1.263 | V | FB=$V_{IN-}$ |
| Feedback H voltage | $V_{FBH}$ | 1.6 | 1.9 | - | V | $I_{FB}$=-100μA |
| Feedback L voltage | $V_{FBL}$ | - | 0.6 | 0.9 | V | $I_{FB}$=100μA |

●**Reference Characteristics (Unless otherwise specified, Ta=25°C, $V_{CC}$ =3V)**

| Item | Symbol | Reference value | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Output block** | | | | | | |
| GATE H voltage | $V_{ONH}$ | $V_{CC}$-0.02 | $V_{CC}$-0.01 | - | V | $I_{GATE}$=-1mA |
| GATE L voltage | $V_{ONL}$ | - | 0.075 | 0.150 | V | $I_{GATE}$=1mA |

○"–" sign for current value represents the direction in which the current flows out from the IC.

●**Reference characteristics data (Unless otherwise specified, Ta=25°C, $V_{CC}$ =24V)**

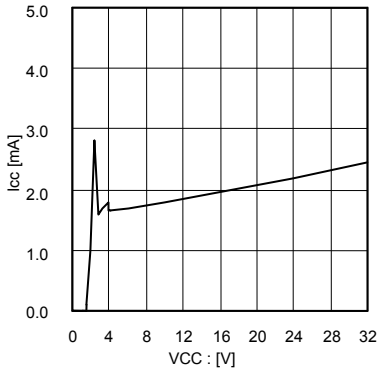



Fig.1 Circuit current

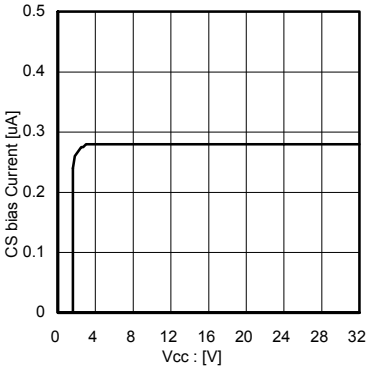



Fig.2 CS current

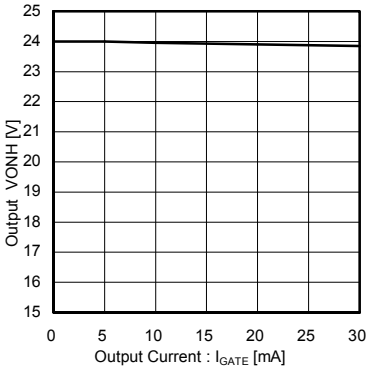



Fig.3 H voltage (Output block)

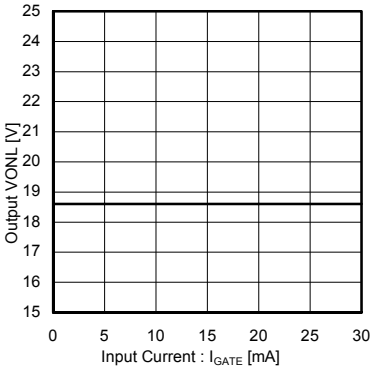



Fig.4 L voltage (Output block)

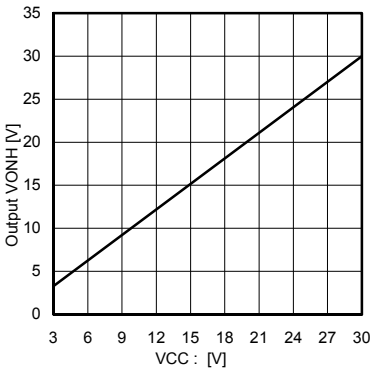



Fig.5 H voltage (Output block)

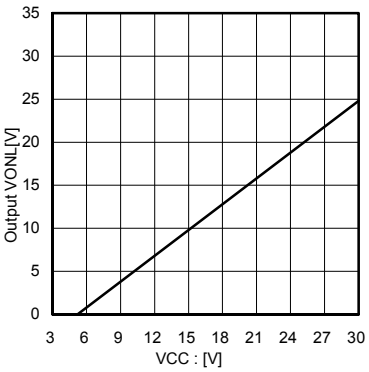



Fig.6 L voltage (Output block)

**●Reference characteristics data (Unless otherwise specified, Ta=25°C, VCC =24V)**

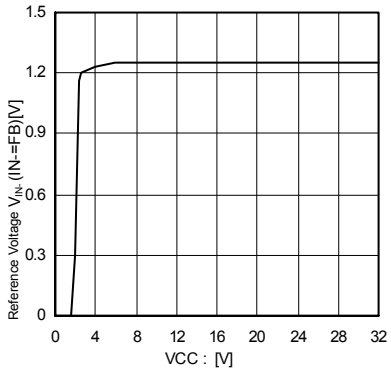



Fig.7 Reference Voltage (Error amplifier block)

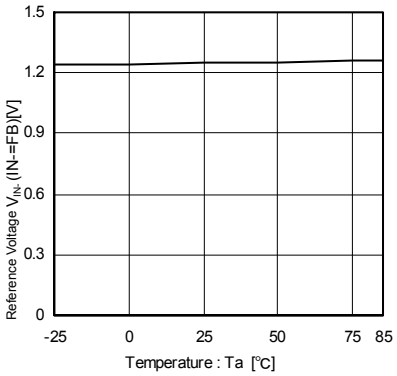



Fig.8 Reference Voltage (Error amplifier block)

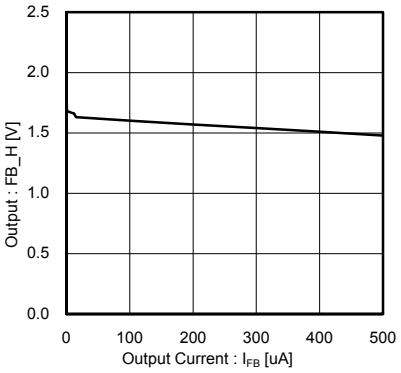



Fig.9 FB_H voltage

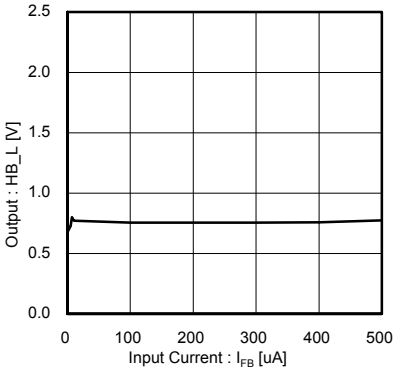



Fig.10 FB_L voltage

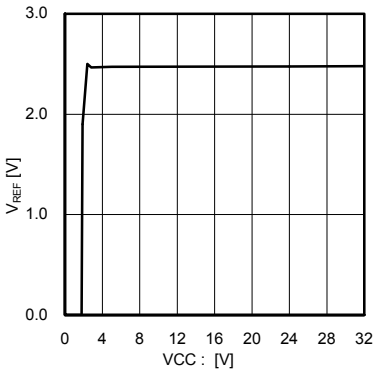



Fig.11 Reference Voltage (Reference voltage block)

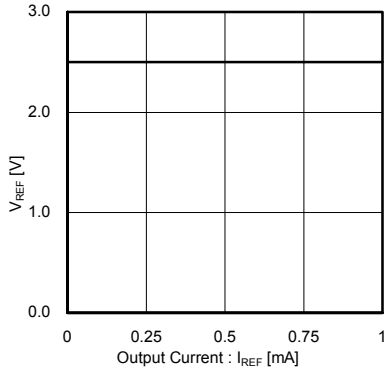



Fig.12 Reference Voltage (Reference voltage block)

**●Pin functions / Block diagram / Application circuit diagram / I/O equivalent circuit diagram**

| PIN NO. | Pin Name | Function |
|---|---|---|
| 1 | OSC | PWM frequency setting |
| 2 | VREF | 2.5V regulator output |
| 3 | FB | Error amplifier output |
| 4 | IN- | Error amplifier input |
| 5 | GATE | Gate output |
| 6 | CS | Current limit input |
| 7 | Vcc | Power supply |
| 8 | GND | Ground |

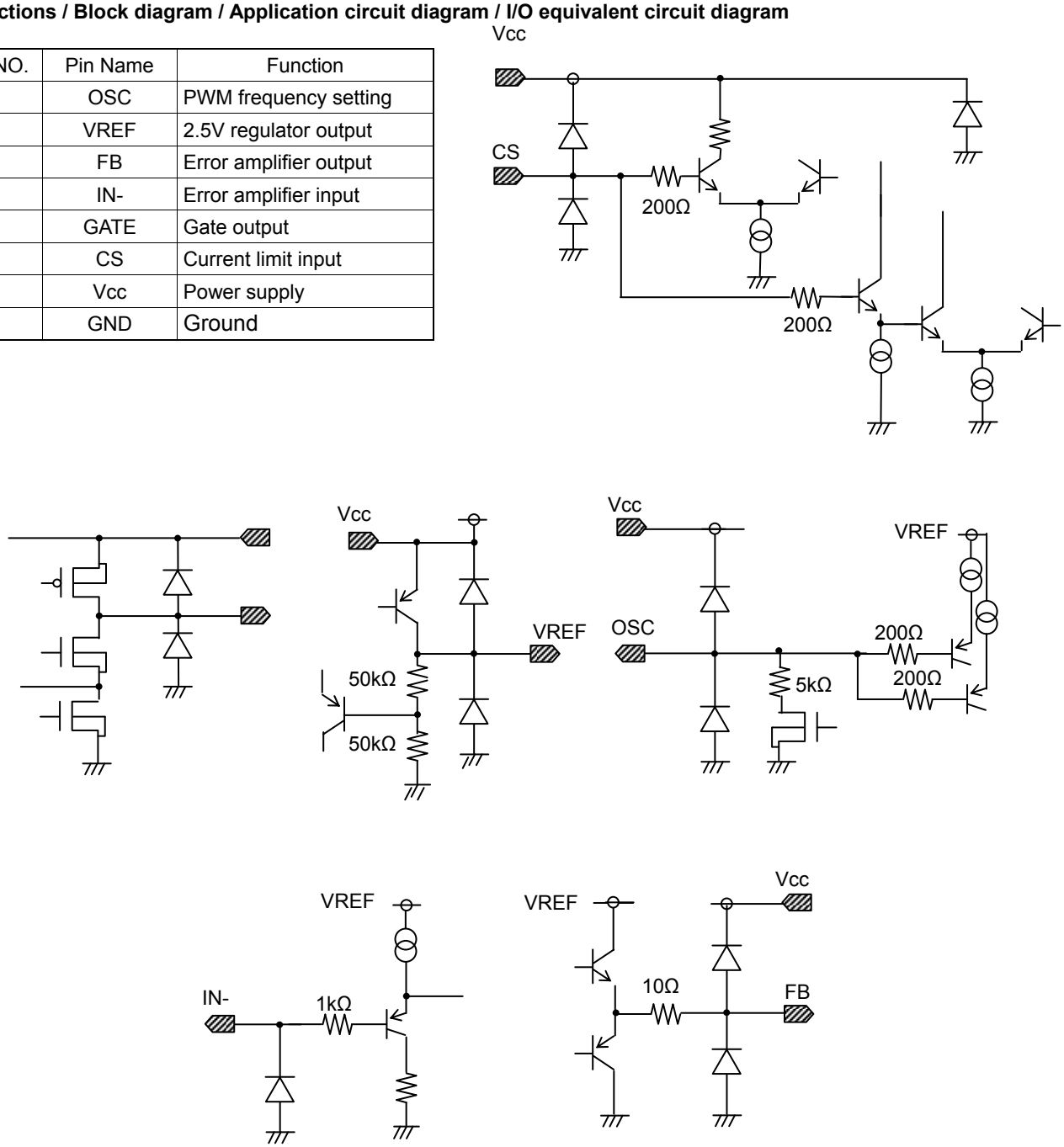



Fig.13 I/O equivalent circuit diagram

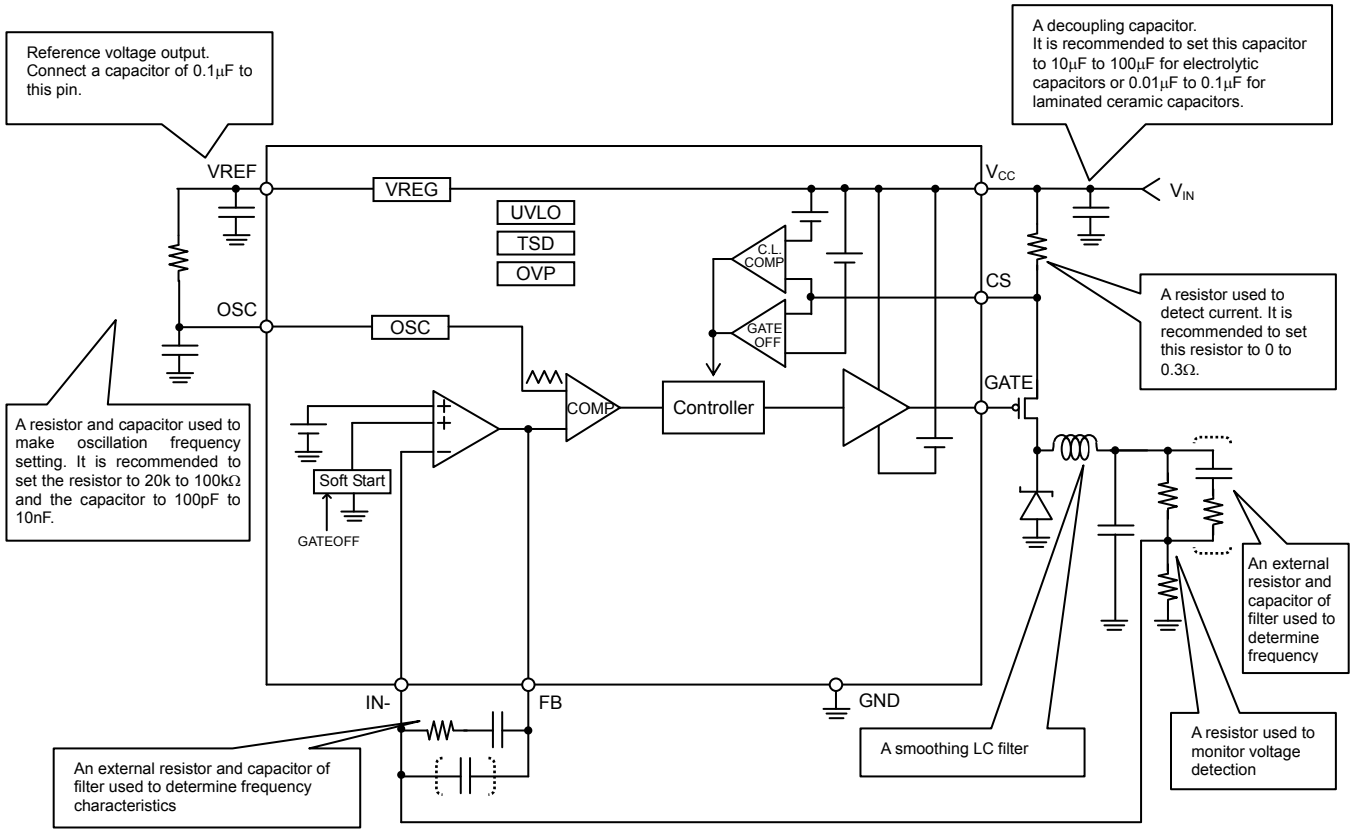



Fig.14 Typical block diagram / application circuit

## ●Description of pins and functions

○$V_{CC}$: Power supply pin

To apply large drive currents, provide thick and short low impedance wiring, and make current adjustment with careful attention paid to PWM switching noise so that $V_{CC}$ voltage will be stable. It is also possible to arrange laminated ceramic capacitors of approximately 0.01μ to 0.1μF in parallel with the aim of reducing power supply impedance in a broad frequency band. Take extra care for $V_{CC}$ voltage so that it will not exceed its rating even for a moment. The $V_{CC}$ pin has a built-in clamp element for electrostatic breakdown protection. If a sudden pulse signal or voltage such as a surge exceeding the absolute maximum rating is applied, this clamp element may be activated to lead to breakdown. To avoid this, NEVER exceed the absolute maximum rating. It is also effective to mount a zener diode having a rating approximate to the absolute maximum rating. In addition, note that since a diode for electrostatic breakdown protection is inserted between the $V_{CC}$ pin and the GND pin, if an inverse voltage is applied to the $V_{CC}$ pin and the GND pin, the IC may lead to breakdown.

○GND: Ground pin

In order to reduce noises due to switching current and stabilize the internal reference voltage of IC, minimize wiring impedance from this pin and maintain the potential at the minimum level in any operating state. In addition, design patterns so that the pin has no common impedance to other GND patterns.

○VREF: 2.5V regulator output pin

The VREF pin is a pin used to output internal reference voltage 2.5V (typ.) generated from power supply voltage input to the $V_{CC}$ pin. In order to stabilize power supply, be sure to connect a 0.1μF capacitor. This pin is also used as a bias power supply. For this application, set a load current to approximately 1mA or less. In addition, note that grounding this pin may pass a large current through the IC, causing it to break down.

○FB: Error amplifier output pin

The FB pin is an output pin of the feedback error amplifier.

○IN-: Error amplifier input pin

The IN- pin is an input pin of the feedback error amplifier.

○GATE: External FET drive pin

This GATE pin is a pin used to drive the external FET gate. Since output H voltage is "$V_{CC}$ voltage − 0.05V (typ)" and output L voltage is "$V_{CC}$ voltage − 5.4V (typ)", the pin is able to directly drive the external FET gate. Provide thick and short low impedance wiring from this pin. The GATE pin has a built-in clamp element for electrostatic breakdown protection. If a sudden pulse signal or voltage such as a surge exceeding the absolute maximum rating is applied, this clamp element may be activated to lead to breakdown. To avoid this, NEVER exceed the absolute maximum rating. It is also possible to make switching rate adjustment by mounting a resistor between the GATE pin and the external FET. In addition, note that since the GATE pin is designed to connect the internal regulator to CMOS output, if voltages between the $V_{CC}$ pin and the GATE pin causes a significant difference by grounding or else, the IC may lead to breakdown.

○OSC: PWM oscillation frequency setting capacitance connection pin

The OSC pin is a pin used to produce a triangular waveform for output PWM oscillation frequency and connect an external resistor and capacitor. By connecting the external resistor and capacitor to this pin, perform charge and discharge. Since H level for a triangular waveform is 1.4V (typ) and L level is 1.0V (typ), a triangular waveform having an amplitude of ΔOSC=0.4V (typ) is produced. The resistor determines a charge current, and the current is discharged inside the IC through resistance of 5kΩ (typ). However, at high frequencies in excess of several hundred kHz, ΔOSC amplitude may exceed 0.4V (typ) due to delay in the internal circuit. To operate the IC at high frequencies, pay careful attention to the frequencies. The following section shows a characteristics table of capacitance when the external resistor is set to 30kΩ. For example, when the capacitor is set to 1000pF, frequency "f" will come to 91 [kHz].

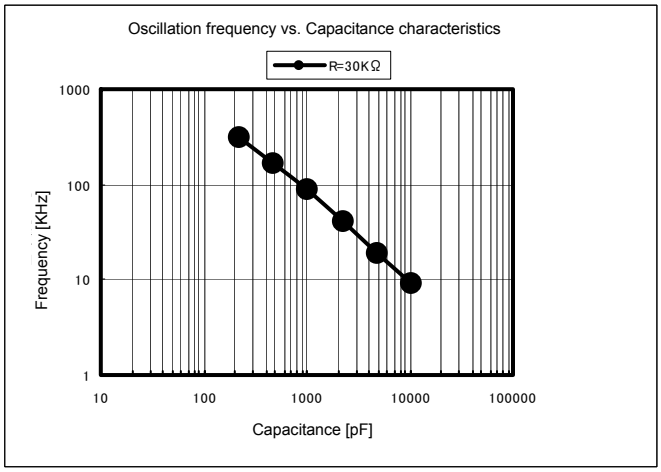



Fig.15 Typical oscillation frequency characteristics

A calculation formula used to make oscillation frequency setting is shown below.

$$f = \frac{1}{C(0.31R + 1980) + 2e - 7}$$

Note that the formula shown above is a reference formula for calculations in the setting range of 470p to 2200pF for the capacitor and 30k to 100kΩ for the resistor. On application boards, oscillation frequencies may be influenced by wiring capacitance or the capacity of an oscilloscope used to monitor the frequencies and thereby calculated values may become different from actual values. Consequently, make it principle to use this formula as a guide for making oscillation frequency setting.

○CS: Current detection comparator input pin

The CS pin is an input pin of overcurrent detection circuit comparator. This IC has a built-in overcurent detection circuit (current limit function) used to turn OFF output current if an abnormal overcurrent such as short-circuited output current flows through the IC. This circuit monitors the currents of external FET such as current-sense resistor to input them to the CS pin. When a voltage input to the CS pin reaches "$V_{CC}$ voltage − 0.15V (typ)", the current limit function will be activated. And when it reaches the current limit voltage, the CS pin will turn OFF output current according to the set resistance and current values. Subsequently, the pin will be automatically reset when the OSC pin reaches its peak voltage. As just described, the CS pin is of the automatic resetting type. The CS pin is reset at the peak voltage of the OSC pin and, when the voltage reaches the set current limit voltage, reset at the same peak voltage again. Then, the CS pin repeats such resetting cycle. Since superimposing noises onto this pin may cause malfunctions, masking time of approximately 300ns has been internally set. In addition, it is possible to prevent noises form jumping in the CS pin by adding a capacitor to this pin. Since delay time of approximately 700ns including the said masking time of approximately 300ns is provided after the current limit is input until it reaches the GATE pin, if the IC is controlled at a duty cycle of 700ns or less, the current limit function will not be activated. Normally, no current setting seems to be made to the extent that the CS pin reaches the current limit voltage in the period of approximately 700ns. However, pay utmost attention to the current setting because it also depends on the external FET. If the overcurrent detection circuit is not used, short-circuit the CS pin to the $V_{CC}$ pin. If a current exceeds the absolute maximum rating of the CS pin, the IC may break down. To avoid this, pay utmost attention to the current.

A current for the current limit function is set to "0.15V ÷ Resistance". For example, when resistance is 75mΩ, the set current for the current limit function will come to "2A".

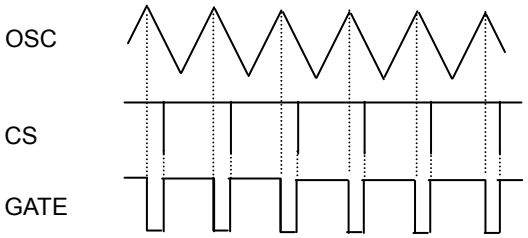



Fig.16 Current limit operation

If a voltage to be input to the CS pin falls below "$V_{CC}$ voltage − 1V (typ)", the gate-off function will be activated to turn OFF output current. When the CS pin exceeds a voltage of "$V_{CC}$ voltage − 1V (typ)", the output current will be reset by the soft start function.

○SOFT START

This IC has a built-in soft start function. This function is used to generate a clock in sync with oscillation inside the IC and operate the internal 6bitDAC with this clock. Soft start time depends on the oscillation frequency. Taking a frequency 8 times as high as the oscillation frequency as a reference clock, raise the output voltage at a rate of 40mV/count. The output voltage will exceed approximately 1.25V at 32 counts. For example, when oscillation frequency $f_{OSC}$ is set to 100 kHz, a period of time required to raise the voltage from 0V to 1.25V will come to approximately 2.56ms from "10μs × 8 × 32 counts".

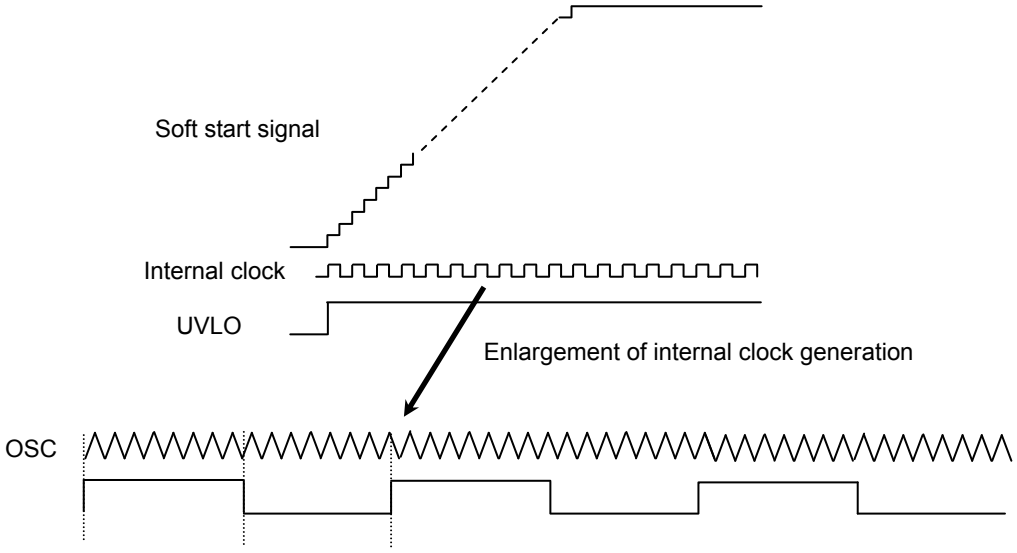



Fig.17 Soft start operation

## ●Protection circuits

### ○Thermal shutdown (TSD) circuit

This IC has a built-in thermal shutdown (TSD) circuit as overheat protection. When the IC chip temperature exceeds 175°C (typ), GATE output will be turned OFF. When the temperature falls below 155°C (typ), the IC will return to the normal operation. In this case, the normal operation starts up in the soft start sequence. However, if external heat is continually applied to the IC even when the TSD circuit is in operation, the IC may cause thermal runaway, resulting in breakdown.

### ○Overcurrent protection circuit (Current limit function)

This IC has a built-in overcurrent protection circuit. This circuit is a circuit absolutely intended to protect the IC from breakdown due to overcurrent in abnormal states such as output short circuit, not intended to protect or guarantee sets with the overcurrent protection circuit incorporated. Consequently, do not design the protection of sets making use of the function of this circuit. For practical use, take physical safety measures such as use of fuses.

### ○Undervoltage lockout (UVLO) function

This IC has a built-in undervoltage lockout circuit to prevent malfunctions such as IC output at low power supply voltages. If power supply voltage falls below the operating voltage range, this UVLO function will be activated. However, if a voltage applied to the $V_{CC}$ pin reaches 2.35V (typ), the UVLO function will turn OFF the Gate output once. The switching voltage is provided with hysteresis of approximately 0.15V (typ) in order to prevent malfunctions such as noises. If the UVLO function is cleared, the IC will start up in the soft start sequence.

### ○Overvoltage protection (OVP) function

This IC has a built-in overvoltage protection function as a protection circuit for a rise in power supply voltage. If power supply voltage exceeds the absolute maximum rating, this OVP function will be activated. However, if a voltage applied to the $V_{CC}$ pin exceeds 33.5V (typ), the OVP function will turn OFF the Gate output once. The switching voltage is provided with hysteresis of approximately 1V (typ) in order to prevent malfunctions such as noises. If the OVP function is reset, the IC will start up in the soft start sequence.

**●Switching regulator control**

Fig. 18 shows the basic configuration of a switching regulator application. The error amplifier determines an output duty cycle so that a voltage used to monitor output voltage will become equal to the internal reference voltage. The output driver switches frequency at the said duty cycle, smoothes the switching voltage through the LC filter, and outputs Vout. This IC has an internal reference voltage of 1.25V (typ) and a recommended output voltage range of 3.3V to 5V. Note that if the output voltage is set to below 3.3V, for example to 1.25V, the output switching duty cycle may become narrow to disable current limit setting, depending on oscillation frequency to be used.

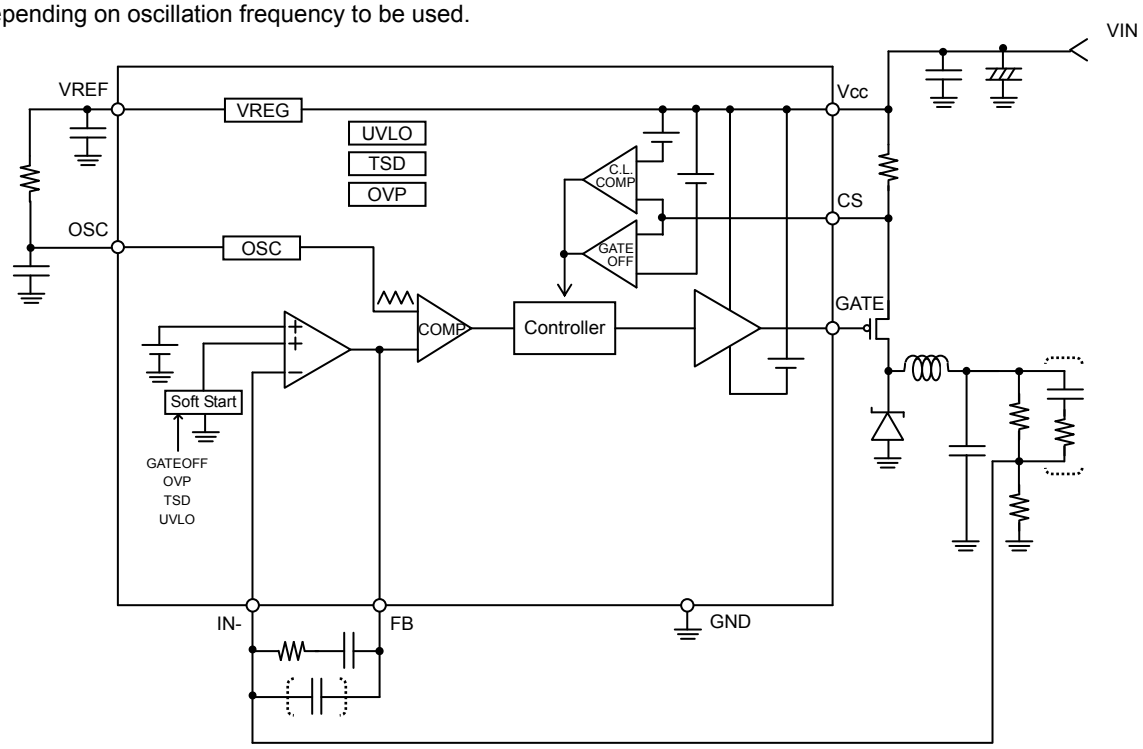
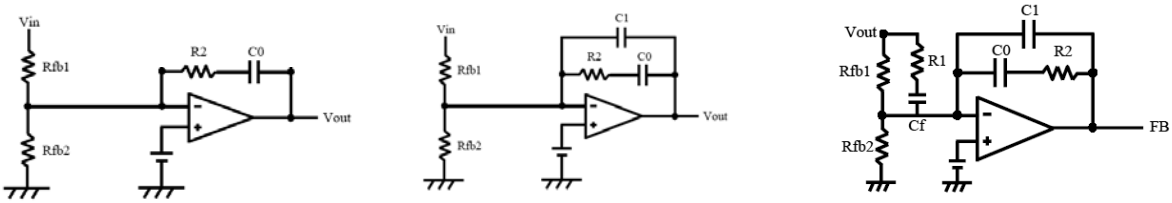



Fig.18 Switching regulator block diagram

**<Typical filter circuit>**

When considering a filter circuit used to determine phase characteristics with the application of this IC, the three patterns shown in Fig. 19 below are available as a popular way to arrange the filter circuits. The selective use of these circuits is determined by the relationship between the PWM frequency to be used and the second pole of LC filter, the zero point at ESR of output capacitor, and ripple elimination rate at the PWM switching frequency to be used.




(a) Filter example 1 (b) Filter example 2 (c) Filter example 3

Fig.19 Examples of filter circuits used to determine phase characteristics

The circuit (a) is the simplest pattern and available for use if the output capacitor has high ESR.
The circuit (b) is a pattern designed by adding a capacitor to the pattern of (a) and available for use if the output capacitor has high ESR and the voltage ripple elimination rate at the PMW frequency needs to be increased from that of the pattern of (a).
The circuit (c) is a pattern designed by adding two zero-points and thereby available for use even if the output capacitor has small ESR.

Selectively use the circuits according to the requirement specifications and situations for inductors, capacitors, and PWM frequency using the patterns shown above.

**<Typical application design>**

The following section shows a typical application design.

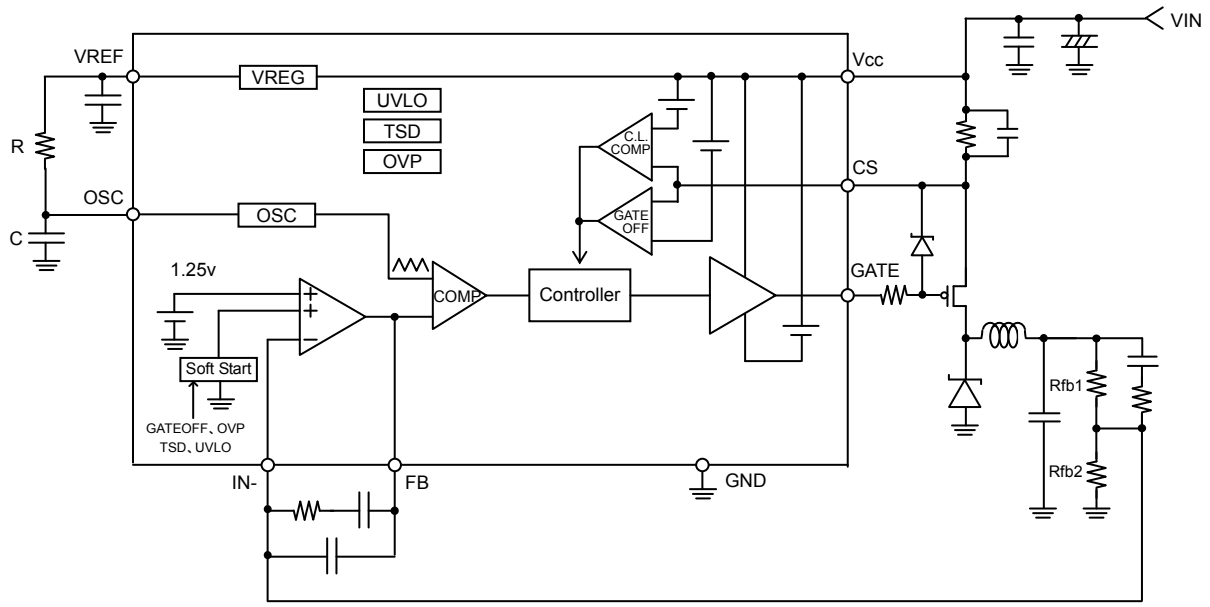



Fig.20 Typical application design

**<Example of simple design>**

The following section shows a design example of constants targeting the applications listed below.
Power supply voltage=24V, Output voltage=3.3V, Coil=47μF, Output capacitor=2200μF, Resr=0.015Ω, PWM frequency=80 kHz, and Load resistance=10Ω

**1. Determination of values of output voltage detecting resistance**

The internal reference voltage is 1.25V and the maximum IN-bias current is 2μA. Consequently, to output Vout of 3.3V, select resistance values enough to keep from the influence of this bias current, that is, Rfb1=33kΩ and Rfb2=20kΩ. In this case, the ratio of Rfb1 to Rfb2 cannot be changed, but the number of digits of resistance values can be changed.

**2. Setting of R (resistance) and C (capacitance) used to make PWM frequency setting**

When setting C to 1000pF and R to 39kΩ, the PWM frequency will come to approximately 80 kHz.

**3. Determination of L (inductance) and C (capacitance) in accordance with characteristic requirements**

This design example is based on L=47μF, C=2200μF, and Resr=0.015Ω.

**<Reference>**

Determine a value for the coil to the extent that the system does not enter intermittent mode until it reaches the minimum value of the preset output current. In this case, however, careful attention should be paid not to cause the coil to become saturated when the maximum current flows.

Reference formula: $L=(Vi-Vo)VoT/\Delta ILVi$ [H], where $\Delta IL$ = Ripple current of coil, T = 1/Switching frequency

Determine a value for the output capacitor from ESR and output ripple voltage. It is recommended to use a capacity taking into account enough margin to a value meeting the specification.

Reference formula: $\Delta Vout \approx \Delta IL \times Resr$, where Resr = Equivalent series resistance of capacitor

**4. Selection of filter circuit**

For the selection of a filter type, PWM frequency, second pole of LC: "fωp", and zero point at ESR: "fzesr" are important. This design example is based on the following:

$$f\omega p = \frac{1}{2\pi\sqrt{LC(1+\frac{\mathrm{Re}\,sr}{R0})}} = \frac{1}{2\pi\sqrt{47u\times 2200u(1+\frac{0.015}{10})}} = 495Hz$$

$$fz = \frac{1}{2\pi\ C\mathrm{Re}\,sr} = \frac{1}{2\pi\times 2200u\times 0.015} = 4.823kHz$$

For this design, PWM frequency is 80 kHz. When looking at unity gain frequency in a total loop with consideration given to ripple elimination at this frequency, the unity gain frequency should be set in the range of 1/5 to 1/10 of the PWM frequency, i.e., 8 kHz to 16 kHz. This frequency comes to 10 or more times as high as that for fωp, however the return of zero point at ESR cannot be expected particularly in the range of 8 kHz to 16 kHz because fz is set to 4.823 kHz. As a result, design the filter circuit based on the Example (c) shown on the previous page.

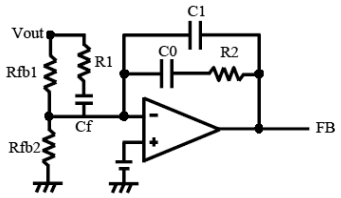



Fig.21 Example (c) of filter circuit used to determine phase characteristics

**5. Determination of filter constant**

Look at the design example based on (c). Making an approximate calculation by taking "∞" as the open loop gain of the amplifier in this circuit will come to the following formula.

$$G(j\omega) = \frac{Vout}{Vin} = -\frac{1}{j\omega\bullet(C0+C1)Rfb1}\bullet\frac{(1+j\omega C0R2)(1+j\omega Cf(Rfb1+R1))}{[1+j\omega(C0//C1)R2]\bullet(1+j\omega R1Cf)}$$

| | |
|---|---|
| **DC gain** | $\mathrm{Gain} = \frac{1}{(C0+C1)Rfb1}$ |
| **Zero point** | $fz1 = \frac{1}{2\pi(R1+Rfb1)Cf}$ $\quad fz\,2 = \frac{1}{2\,\pi\,R\,2\,C\,0}$ |
| **Cutoff frequency** | $fp\,1 = \frac{1}{2\,\pi\,R\,1Cf}$ $\quad fp2 = \frac{1}{2\pi R2(C0//C1)}$ |

The transfer functions of this circuit are shown above. Two zero points can be set. Look at the filter constant using this circuit as shown below. Approximating phase characteristics in the whole loop with the use of this circuit will come to the following formula.

Phase = Second pole of LC filter + Zero point of LC filter + First pole of error amplifier
+ Second pole + −90° (1/s) of error amplifier + First zero-point of error amplifier
+ Second zero-point

Make calculations by converting these items into a formula and supposing that unity gain frequency is 8 kHz and phase margin is 51°. Since directly calculating constants results in values in too small digits, the values need to be rounded off. Then, the constants come to Rfb1=33kΩ, Rfb2=20kΩ, R1=10kΩ, R2=120kΩ, C0=220pF, C1=51pF, and Cf=1nF. In this case, when looking at the LC filter on the ideal basis of only the second pole + zero point, the unity gain frequency will be calculated to 10 kHz and the phase margin to approximately 54°. Actually, the inductance and capacitance of printed circuit board will be added, and thereby errors will be caused in calculation results depending on the printed circuit board used. Consequently, it is considered acceptable to make fine adjustment of resistance and the capacitance of capacitor with FRA according to the calculation results and then determine the constants.

## ●Notes for Use

(1) Absolute maximum ratings

An excess in the absolute ratings such as applied voltage, operating temperature range, etc. can break down devices, thus making it impossible to identify a destruction state such as short or open circuit mode. If any special mode to exceed the absolute maximum ratings is expected, consider adding circuit protection devices such as fuses.

(2) Reverse connection of power supply connector

Making a reverse connection of the power supply connector can cause the IC to break down.

(3) Power supply line

If current regenerated by back electromotive force flows back, consider adding protection devices such as insertion of a capacitor between the power supply and ground as a path of regenerative current and thoroughly check capacitance for any problems with characteristics such as lack of capacitance of electrolytic capacitors caused at low temperatures, and then determine the power supply line.

(4) GND potential

The potential of the GND pin should be maintained at the minimum level in any operating state.

(5) Transient changes

In this IC, the GATE pin L voltage is set to "$V_{CC}$ voltage − 5.4V (typ)" with the internal regulator of the IC. If output makes a sudden change due to high switching speed, the voltage can cause transient deviation in excess of "$V_{CC}$ voltage − 6.2V (max)". To avoid this and also protect between the gate and the source of external MOS-FET, it is recommended to insert and clamp a proper zener diode between the GATE pin and the power supply pin.

(6) Thermal design

Provide thermal design having a sufficient margin in consideration of power dissipation (Pd) in the practical operating conditions. Use the thermal design providing as wide radiation pattern as possible in thorough consideration of practical operating conditions.

(7) Inter-pin shorts and mounting errors

To mount the IC on printed circuit boards, pay utmost care to the direction and the displacement of the IC. The IC may get damaged if there is any mounting error or if a short circuit is established due to foreign matter entered between pins. In addition, thoroughly note that this IC may also get damaged if the VREF pin or GATE pin reaches low potential or is grounded.

(8) Operation in strong magnetic field

This IC is not designed for operation in the presence of strong magnetic field. To use the IC in a strong magnetic field, ensure that such use causes the IC not to malfunction.

(9) Thermal-protection circuit (TSD circuit)

This IC has a built-in thermal-protection circuit (TSD circuit). If chip temperature rises beyond $T_{jmax}$=150°C, the GATE pin will output high voltage and turn OFF the external output transistor. The thermal-protection circuit (TSD circuit) is a circuit absolutely intended to protect the IC from thermal runaway under abnormal conditions beyond $T_{jmax}$=150°C, not intended to protect or guarantee sets. Consequently, do not design the protection of sets making use of the function of this circuit

| TSD ON temperature [°C] (typ.) | Hysteresis temperature [°C] (typ.) |
|---|---|
| 175 | 25 |

(10) Testing on application board

When testing the IC on an application board with a capacitor connected to the pin, the IC can be subjected to stress. In this case, be sure to discharge the capacitor after each process. For static electricity protection, ground the IC during the assembly process, and further pay utmost attention to the transport and storage of the IC. In addition, to connect the IC to a jig up to the testing process, be sure to turn OFF prior to connection, and disconnect the IC only after turning OFF the power supply.

(12) IC pin input

This monolithic IC contains P + Isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersections of these P layers and the N layers of other elements, thus making up different types of parasitic elements.

For example, if a resistor and a transistor is connected with pins respectively as shown in Fig. 22,

○When GND>(Pin A) for the resistor, or when GND>(Pin B) for the transistor (NPN),
P-N junctions operate as a parasitic diode.

○When GND>(Pin B) for the transistor (NPN),
the parasitic NPN transistor operates by the N layer of other element adjacent to the parasitic diode aforementioned.

Due to the structure of the IC, parasitic elements are inevitably formed depending on the relationships of potential. The operation of parasitic elements can result in interferences in circuit operation, leading to malfunctions and eventually breakdown of the IC. Consequently, pay utmost attention not to use the IC for any applications by which the parasitic elements are operated, such as applying a voltage lower than that of GND (P substrate) to the input pin.

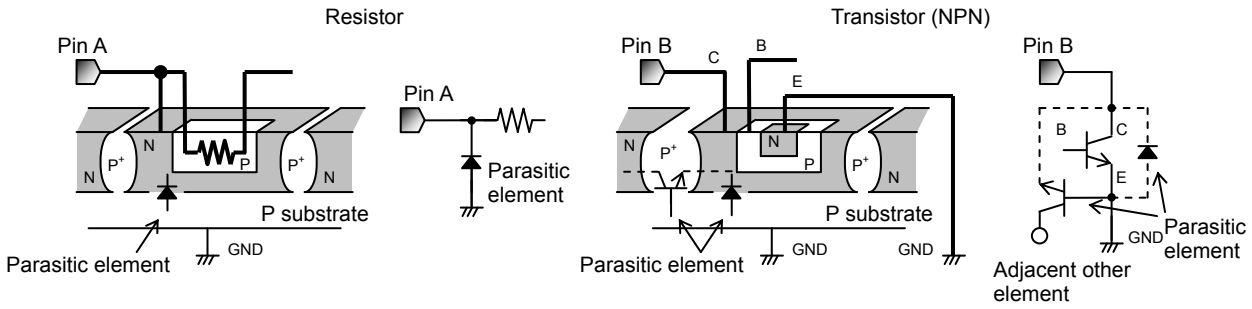



Fig.22 Pattern diagram of parasitic elements

(13) Wiring patterns

Give thorough consideration to power supply and ground wirings, for example, reduce the common impedance and minimize ripple.

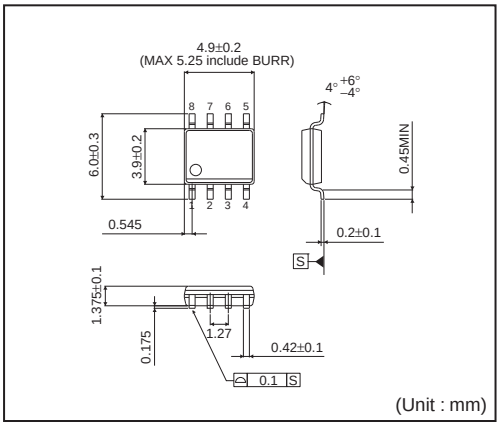
If there are large-current ground and small-signal ground, it is recommended to isolate the large-current ground pattern from the small-signal ground pattern and ground these patterns to a single reference point on the set so that fluctuations in voltage due to the resistance of pattern wiring and large current will not result in fluctuations in the voltage of the small-signal ground. In addition, pay careful attention to the ground wiring patterns of external parts so that no fluctuations in voltage will be caused.

## ●Ordering part number

| B | D | 6 | 3 | 5 | 3 | 6 | F | J | - | E | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|

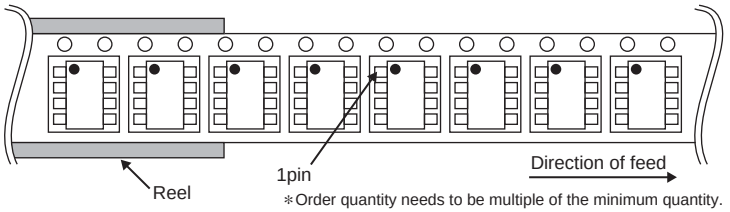
| Part No. | Part No. | Package<br>FJ: SOP-J8 | Packaging and forming specification<br>E2: Embossed tape and reel |
|---|---|---|---|

**SOP-J8**




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.

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