XC6121/XC6122 XC6123/XC6124 Series

Voltage Detector with Watchdog Function and ON/OFF Control (V_{DF}=1.6V~5.0V)

■GENERAL DESCRIPTION

The XC6121/XC6122/XC6123/XC6124 series are groups of high-precision, low current consumption voltage detectors with watchdog functions incorporating CMOS process technology. The series consist of a reference voltage source, delay circuit, comparator, and output driver. With the built-in delay circuit, the XC6121/XC6122/XC6123/XC6124 series' ICs do not require any external components to output signals with release delay time. The output type is VDFL low when detected. With the XC6121/XC6122/XC6123/XC6124 series' ICs, the EN/ENB pin can control ON and OFF of the watchdog functions. By setting the EN/ENB pin to low or high level, the watchdog function can be OFF while the voltage detector remains operation. Since the EN/ENB pin of the XC6122 and XC6124 series is internally pulled up to the VIN pin or pulled down to the V_{SS} pin, the ICs can be used with the EN/ENB pin left open, when the watchdog functions is used. The detect voltages are internally fixed 1.6V ~ 5.0V in increments of 0.1V, using laser trimming technology. Six watchdog timeout period settings are available in a range from 50ms to 1.6s. Five release delay time settings are available in a range from 3.13ms to 400ms.

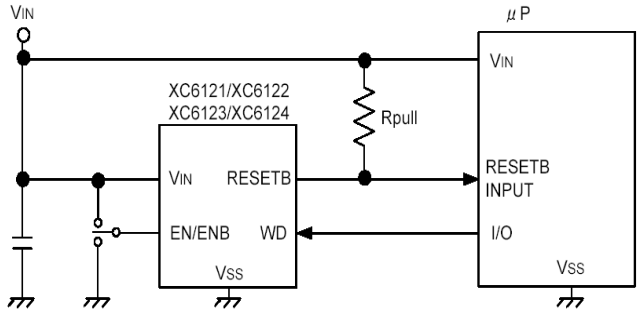
■APPLICATIONS

- Microprocessor watchdog monitoring and reset circuits
- Memory battery backup circuits
- System power-on reset circuits
- Power failure detection

■FEATURES

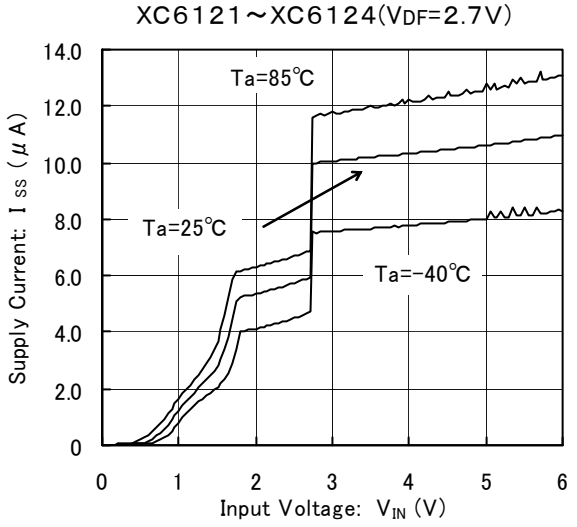
Detect Voltage Range	: 1.6V ~ 5.0V, ±2% (0.1V increments)
Hysteresis Width	: VDFL x 5% (TYP.)
Operating Voltage Range	: 1.0V ~ 6.0V
Detect Voltage Temperature Characteristics	: ±100ppm/°C (TYP.)
Output Configuration	: N-channel open drain
Watchdog Pin	: Watchdog input If watchdog input maintains 'H' or 'L' within the watchdog timeout period, a reset signal is output from the RESETB pin.
EN/ENB Pin	: When the EN/ENB pin voltage is set to low or high level, the watchdog function is forced off.
Release Delay Time	: 400ms, 200ms, 100ms, 50ms, 3.13ms (TYP.)
Watchdog Timeout Period	: 1.6s, 800ms, 400ms, 200ms, 100ms, 50ms (TYP.)
Package	: SOT-25, USP-6C
Environmentally Friendly	: EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

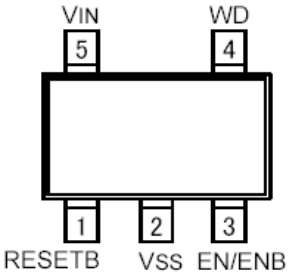


■TYPICAL PERFORMANCE CHARACTERISTICS

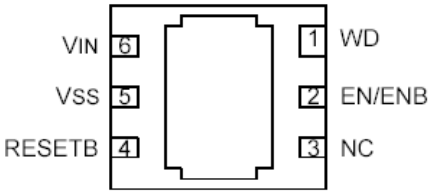
●Supply Current vs. Input Voltage



■PIN CONFIGURATION



SOT-25
(TOP VIEW)



USP-6C
(BOTTOM VIEW)

* The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the VSS (No. 5) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-25	USP-6C		
1	4	RESETB	Reset Output
2	5	VSS	Ground
3	2	EN/ENB	Watchdog ON/OFF Control
4	1	WD	Watchdog
5	6	VIN	Power Input
-	3	NC	No Connection

■PRODUCT CLASSIFICATION

●Selection Guide

SERIES	RESET OUTPUT		HYSTERESIS	EN/ENB PIN FUNCTION
	V_{DFL} (RESETB)	V_{DFH} (RESET)		(EN/ENB INPUT LOGIC*, PULL-UP OR DOWN RESISTOR)
XC6121	N-channel open drain	-	Available: V_{DFL} x 5% (TYP.)	EN with No Pull-Up Resistor
XC6122	N-channel open drain	-		EN with Pull-Up Resistor
XC6123	N-channel open drain	-		ENB with No Pull-Down Resistor
XC6124	N-channel open drain	-		ENB with Pull-Down Resistor

* EN input logic: The watchdog function turns on when the EN pin becomes high level.

* ENB input logic: The watchdog function turns on when the ENB pin becomes low level.

●Ordering Information

XC6121①②③④⑤⑥-⑦(*1): N-channel Open Drain Output (RESETB), EN Pin: No Pull-Up Resistor
XC6122①②③④⑤⑥-⑦(*1): N-channel Open Drain Output (RESETB), EN Pin: Pull-Up Resistor
XC6123①②③④⑤⑥-⑦(*1): N-channel Open Drain Output (RESETB), ENB Pin: No Pull-Down Resistor
XC6124①②③④⑤⑥-⑦(*1): N-channel Open Drain Output (RESETB), ENB Pin: Pull-Down Resistor

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Release Delay Time	A	3.13ms (TYP.)
		C	50ms (TYP.)
		D	100ms (TYP.)
		E	200ms (TYP.)
		F	400ms (TYP.)
②	Watchdog Timeout Period	2	50ms (TYP.)
		3	100ms (TYP.)
		4	200ms (TYP.)
		5	400ms (TYP.)
		6	1.6s (TYP.)
		7	800ms (TYP.)
③④	Detect Voltage	16 ~ 50	Detect voltage ex.) 4.5V: ③⇒4, ④⇒5
⑤⑥-⑦	Packages Taping Type (*2)	MR	SOT-25
		MR-G	SOT-25
		ER	USP-6C
		ER-G	USP-6C

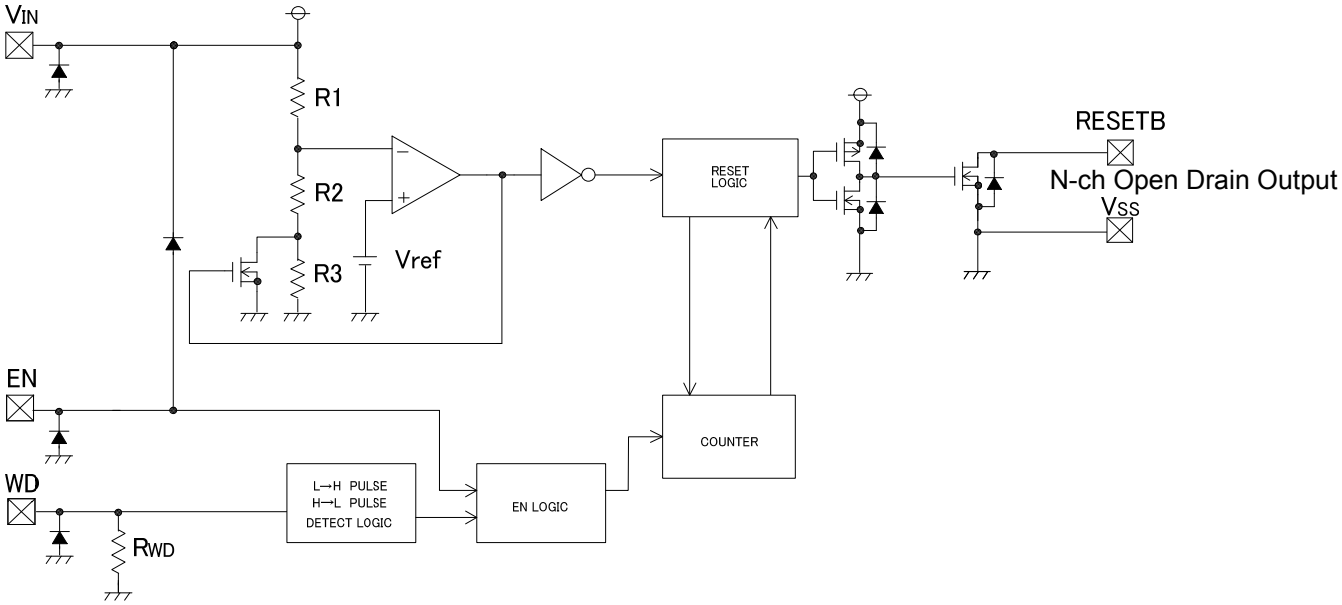
* Please set the release delay time shorter than or equal to the watchdog timeout period.

ex.) XC6121D327MR or XC6121D627MR

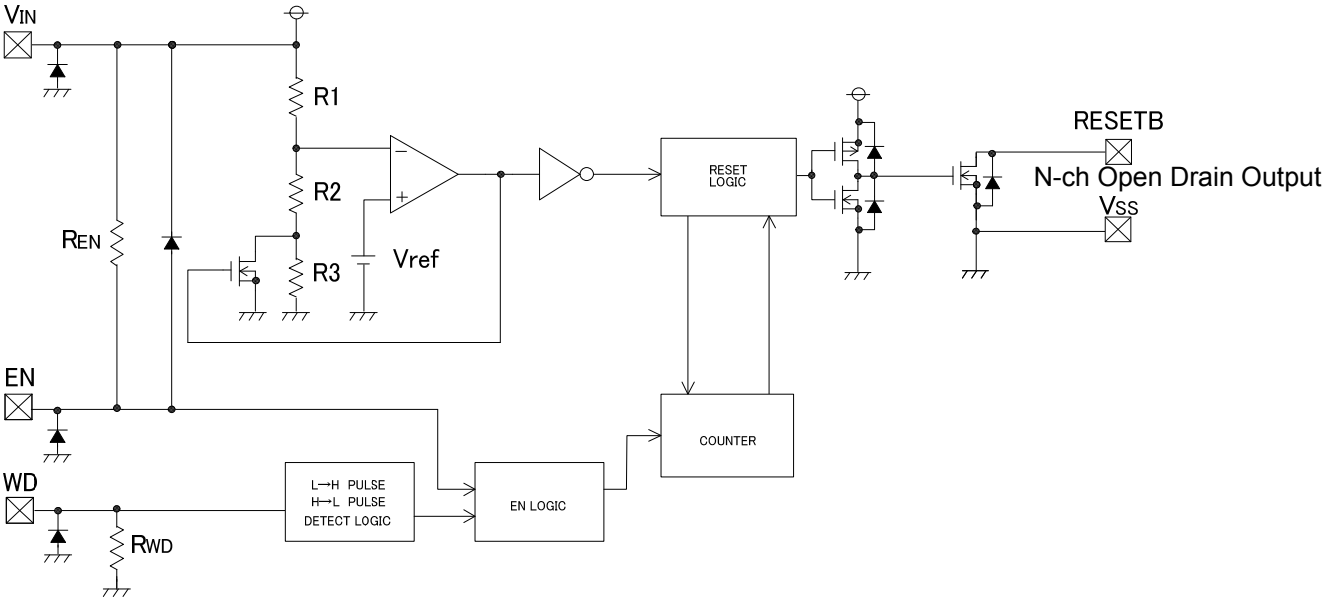
(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.
(*2) The device orientation is fixed in its embossed tape pocket. For reverse orientation, please contact your local Torex sales office or representative. (Standard orientation: ⑤R-⑦, Reverse orientation: ⑤L-⑦)

■BLOCK DIAGRAMS

●XC6121 Series

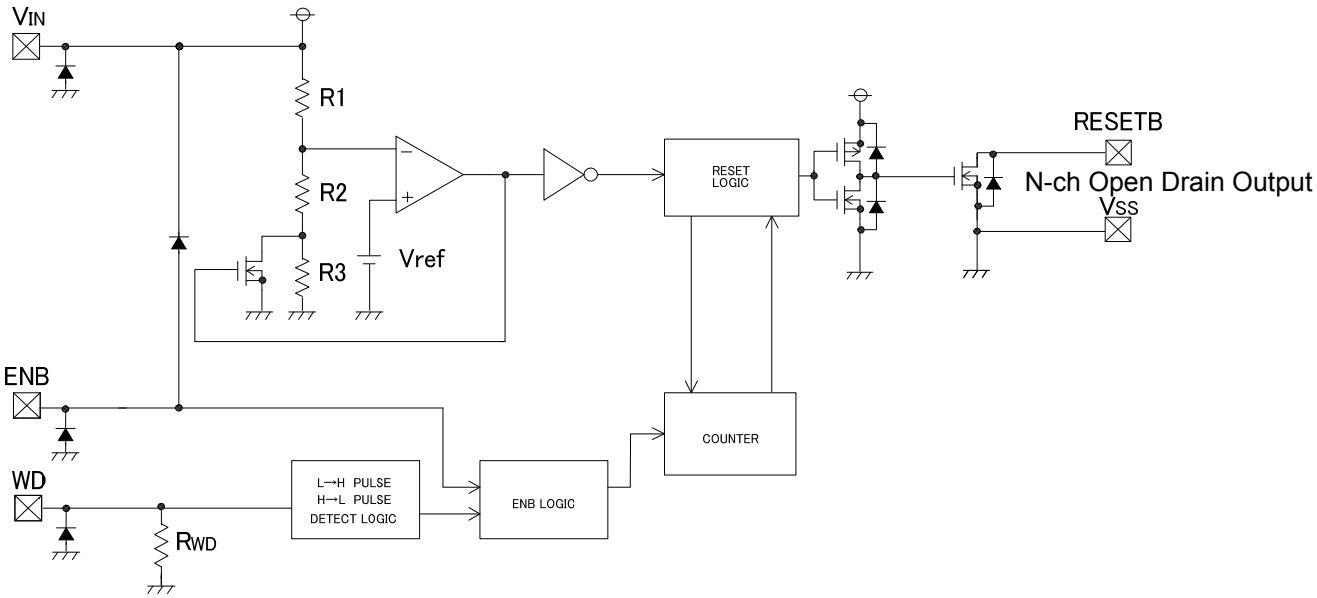


●XC6122 Series

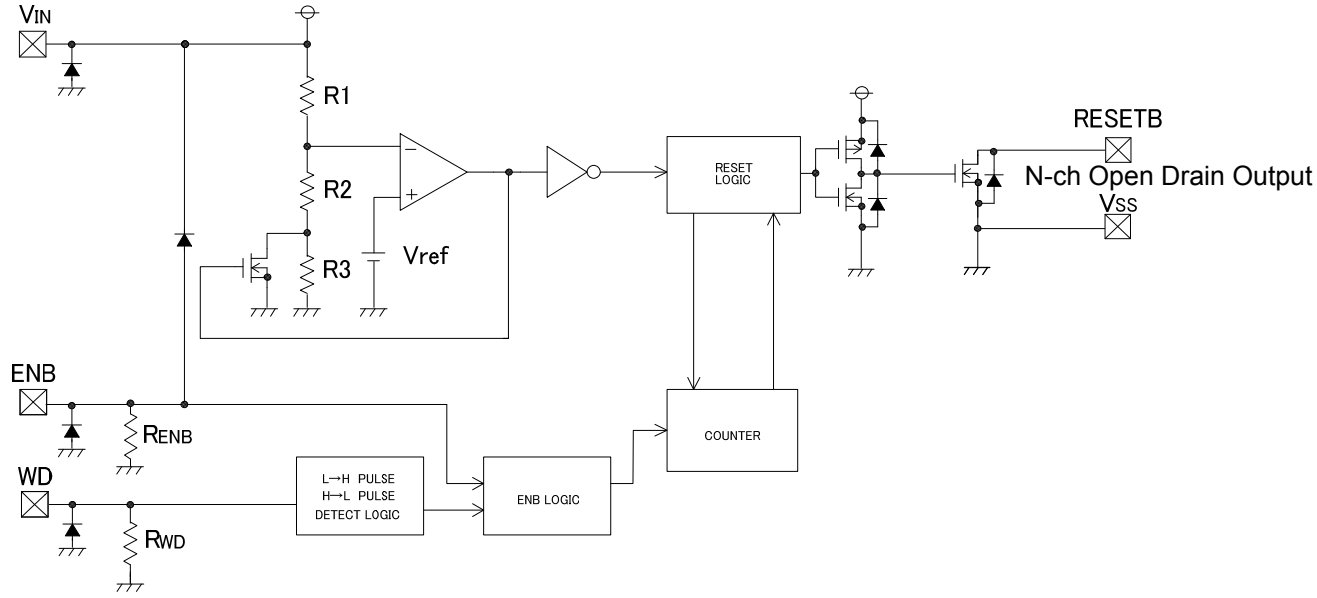


■BLOCK DIAGRAMS (Continued)

●XC6123 Series



●XC6124 Series



■ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	V_{SS} -0.3 ~ 7.0	V
		EN/ENB	V_{SS}-0.3～V_{IN}+0.3≦7.0	V
		WD	V_{SS} -0.3 ~ 7.0	V
Output Current		I_{OUT}	20	mA
Output Voltage		RESETB	V_{SS} -0.3 ~ 7.0	V
Power Dissipation	SOT-25	Pd	250	mW
	USP-6C		100	
Operational Temperature Range		Topr	-40 ~ +85	°C
Storage Temperature Range		Tstg	-55 ~ +125	°C

■ELECTRICAL CHARACTERISTICS

Ta = 25 °C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Detect Voltage	V_{DFL}	EN=V_{SS},ENB=V_{IN}	$V_{DFL(T)}$ × 0.98	$V_{DFL(T)}$	$V_{DFL(T)}$ × 1.02	V	①
Hysteresis Width	V_{HYS}		V_{DFL} × 0.02	V_{DFL} × 0.05	V_{DFL} × 0.08	V	①
Supply Current (*1)	I_{SS}	the WD Pin: OPEN, V_{IN}=$V_{DFL(T)}$×0.9V	-	5	11	⌠A	②
		the WD Pin: OPEN, V_{IN}=$V_{DFL(T)}$×1.1V	-	10	16		
		the WD Pin: OPEN, V_{IN}=6.0V	-	12	18		
Operating Voltage	V_{IN}		1.0	-	6.0	V	①
Output Current	I_{RBOUT}	N-ch. V_{DS} = 0.5V, V_{IN}=1.0V	0.15	0.5	-	mA	③
		N-ch. V_{DS} = 0.5V, V_{IN}=2.0V ($V_{DFL(T)}$> 2.0V)	2.0	2.5	-		
		N-ch. V_{DS} = 0.5V, V_{IN}=3.0V ($V_{DFL(T)}$ >3.0V)	3.0	3.5	-		
		N-ch. V_{DS} = 0.5V, V_{IN}=4.0V ($V_{DFL(T)}$ >4.0V)	3.5	4.0	-		
Temperature Characteristics	△V_{DFL} / △Topr・V_{DFL}	-40°C ≦ Topr ≦ 85 °C	-	±100	-	ppm/ °C	①
Release Delay Time (V_{DFL}≦1.8V)	t_{DR}	Time until V_{IN} is increased from 1.0V to 2.0V and attains to the release time level, and the Reset output pin releases.	2.00	3.13	5.00	ms	④
			37	50	63		
			75	100	125		
			150	200	250		
			300	400	500		
Release Delay Time (V_{DFL}≧1.9V)	t_{DR}	Time until V_{IN} is increased from 1.0V to (V_{DFL} x 1.1V) and attains to the release time level, and the Reset output pin releases.	2.00	3.13	5.00	ms	④
			37	50	63		
			75	100	125		
			150	200	250		
			300	400	500		
Detect Delay Time	t_{DF}	Time until V_{IN} is decreased from 6.0V to 1.0V and attains to the detect voltage level, and the Reset output pin detects while the WD pin left open.	-	5.5	33	⌠s	④
V_{DFL} Leak Current	I_{LEAK}	V_{IN}=6.0V, RESETB=6.0V	-	0.01	0.1	⌠A	③
Watchdog Timeout Period (V_{DFL}≦1.8V)	t_{WD}	Time until V_{IN} increases form 1.0V to 2.0V and the Reset output pin is released to go into the detection state. (WD=V_{SS})	37	50	63	ms	⑤
			75	100	125		
			150	200	250		
			300	400	500		
			600	800	1000		
			1200	1600	2000		
Watchdog Timeout Period (V_{DFL}≧1.9V)	t_{WD}	Time until V_{IN} increases from 1.0V to (V_{DFL}x1.1V) and the Reset output pin is released to go into the detection state. (WD=V_{SS})	37	50	63	ms	⑤
			75	100	125		
			150	200	250		
			300	400	500		
			600	800	1000		
			1200	1600	2000		

■ELECTRICAL CHARACTERISTICS (Continued)

Ta = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Watchdog Minimum Pulse Width	T_{WDIN}	V_{IN}=6.0V, Apply pulse from 6.0V to 0V to the WD pin.	300	-	-	ns	⑥
Watchdog High Level Voltage	V_{WDH}	V_{IN}=V_{DFL} x 1.1V ~ 6.0V	V_{IN} x 0.7	-	6	V	⑥
Watchdog Low Level Voltage	V_{WDL}	V_{IN}=V_{DFL} x 1.1V ~ 6.0V	0	-	V_{IN} x 0.3	V	⑥
Watchdog Pull-down Resistance	R_{WD}	V_{WD}=6V, R_{WD}=V_{WD}/I_{WD}	300	600	1000	kΩ	⑦
EN/ENB High Level Voltage	V_{ENH}/V_{ENBH}	V_{IN}=V_{DFL} x 1.1V ~ 6.0V	1.3	-	V_{IN}	V	⑧
EN/ENB Low Level Voltage	V_{ENL}/V_{ENBL}	V_{IN}=V_{DFL} x 1.1V ~ 6.0V	0	-	0.35	V	⑧
EN Pull-up Resistance (*2)	R_{EN}	V_{IN}=6.0V, EN=0V, R_{EN}=V_{IN} / I_{EN}	1.0	1.6	2.4	MΩ	⑨
ENB Pull-down Resistance (*3)	R_{ENB}	V_{IN}=6.0V, ENB=6V, R_{ENB}=V_{IN} / I_{ENB}					

NOTE:
*: In case where no EN/ENB pin's condition written in the test condition field, EN=V_{IN} and ENB=V_{SS}.
**: $V_{DFL(T)}$=Setting detect voltage value
*1: The condition when the watchdog pin is ON.
The EN/ENB pin is CMOS input. For the XC6122 (pull-up resistor) and XC6124 (pull-down resistor), supply current increases in the following values when the watchdog function is OFF.
XC6122 Series：（V_{IN}-V_{EHL}）/1.6MΩ（TYP）
XC6124 Series：V_{EHBH}/1.6MΩ（TYP）
*2: For the XC6122 series only.
*3: For the XC6124 series only.

■OPERATIONAL EXPLANATION

The XC6121/6122/6123/6124 series compare, using the error amplifier, the voltage of the internal voltage reference source with the voltage divided by R1, R2 and R3 connected to the V_{IN} pin. The resulting output signal from the error amplifier activates the watchdog logic, delay circuit and the output driver. When the V_{IN} pin voltage gradually falls and finally reaches the detect voltage, the RESETB pin output goes from high to low in the case of the V_{DFL} type ICs.

<RESETB / RESET Pin Output Signal>
* V_{DFL} (RESETB) type - output signal: Low when detected.
The RESETB pin output goes from high to low whenever the V_{IN} pin voltage falls below the detect voltage. The RESETB pin remains low for the release delay time (t_{DR}) after the V_{IN} pin voltage reaches the release voltage. If neither rising nor falling signals are applied to the WD pin within the watchdog timeout period, the RESETB pin output remains low for the release delay time (t_{DR}), and thereafter the RESET pin outputs high level signal.

<Hysteresis>
When the internal comparator output is high, the NMOS transistor connected in parallel to R3 is turned ON, activating the hysteresis circuit. The difference between the release and detect voltages represents the hysteresis width, as shown by the following calculations:

V_{DFL} *(detect voltage) = (R1+R2+R3) x Vref / (R2+R3)*
V_{DR} *(release voltage) = (R1+R2) x Vref / (R2)*
V_{HYS} *(hysteresis width) =* V_{DR}*-*V_{DFL} *(V)*
$V_{DR} > V_{DFL}$
* Please refer to the block diagrams for R1, R2, R3 and Vref.
* Hysteresis width is selectable from V_{DFL} x 0.05V (TYP.).

<Watchdog (WD) Pin>
The series use a watchdog timer to detect malfunction or “runaway” of the microprocessor. If neither rising nor falling signals are applied from the microprocessor within the watchdog timeout period, the RESETB pin output maintains the detection state for the release delay time (t_{DR}), and thereafter the RESETB pin outputs low to high signal. The watchdog pin is pulled down to the V_{SS} internally. When the watchdog pin is not connected, A reset signal comes out after the watchdog timeout period. Six watchdog timeout period settings (t_{WD}) are available in 1.6s, 800ms, 400ms, 200ms, 100ms, and 50ms.

<EN Pin>
In case where the watchdog function is not used, When the EN pin input driven to low level, only the watchdog function is forced off while the detect voltage circuit remains operation. For using the watchdog function, the EN pin should be used in high level. Even after the input voltage and the EN pin voltage are driven back high, the RESETB pin output maintains the detection state for the release delay time (T_{DR}). (Refer to the TIMING CHART 1-①.) The watchdog function recovers immediately when the input voltage becomes higher than the release voltage and the EN pin voltage driven from low to high level. (Refer to the TIMING CHART 1-②.) A diode, which is an input protection element, is connected between the EN pin and V_{IN} pin. Therefore, if the EN pin is applied voltage that exceeds V_{IN}, the current will flow to V_{IN} through the diode. For avoiding any damage to the IC, please use this IC within the stated maximum ratings (V_{SS} -0.3 ~ V_{IN} +0.3) on the EN pin.

<ENB Pin>
In case where the watchdog function is not used, when the ENB pin input driven to high level, only the watchdog function is forced off while the detect voltage circuit remains operation. For using the watchdog function, the ENB pin should be used in low level. Even after the input voltage and the ENB pin voltage are driven back low, the RESETB pin output maintains the detection state for the release delay time (t_{DR}). (Refer to the TIMING CHART 2-①.) The watchdog function recovers immediately when the input voltage becomes higher than the release voltage and the ENB pin voltage driven from high to low level. (Refer to the TIMING CHART 2-②.) A diode, which is an input protection element, is connected between the ENB pin and V_{IN} pin. Therefore, if the ENB pin is applied voltage that exceeds V_{IN}, the current will flow to V_{IN} through the diode. For avoiding any damage to the IC, please use this IC within the stated maximum ratings (V_{SS} -0.3 ~ V_{IN} +0.3) on the ENB pin.

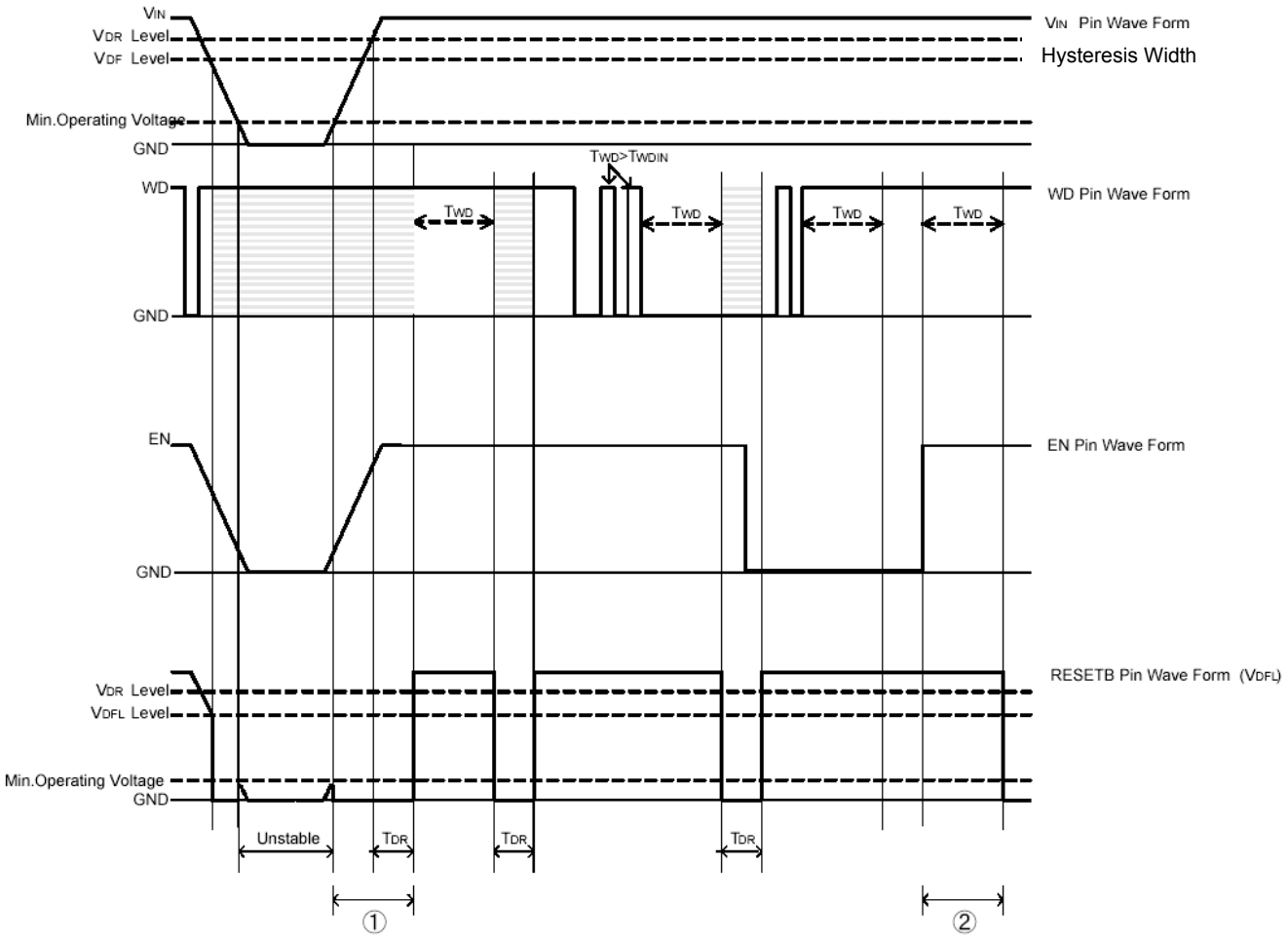
<Release Delay Time>
Release delay time (t_{DR}) is the time that elapses from when the V_{IN} pin reaches the release voltage, or when the watchdog timeout period expires with no rising signal applied to the WD pin, until the RESETB pin output is released from the detection state. Five release delay time (t_{DR}) watchdog timeout period settings are available in 400ms, 200ms, 100ms, 50ms, and 3.13ms.

<Detect Delay Time>
Detect Delay Time (t_{DF}) is the time that elapses from when the V_{IN} pin voltage falls to the detect voltage until the RESETB pin output goes into the detection state.

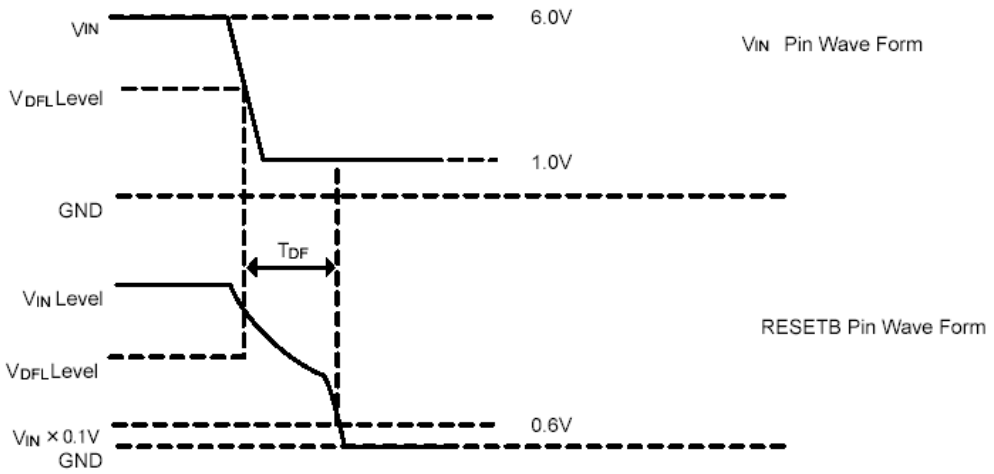
■TIMING CHARTS

1. XC6121/XC6122 Series (EN products)

●N-ch Open Drain Output (Rpull=100kΩ)



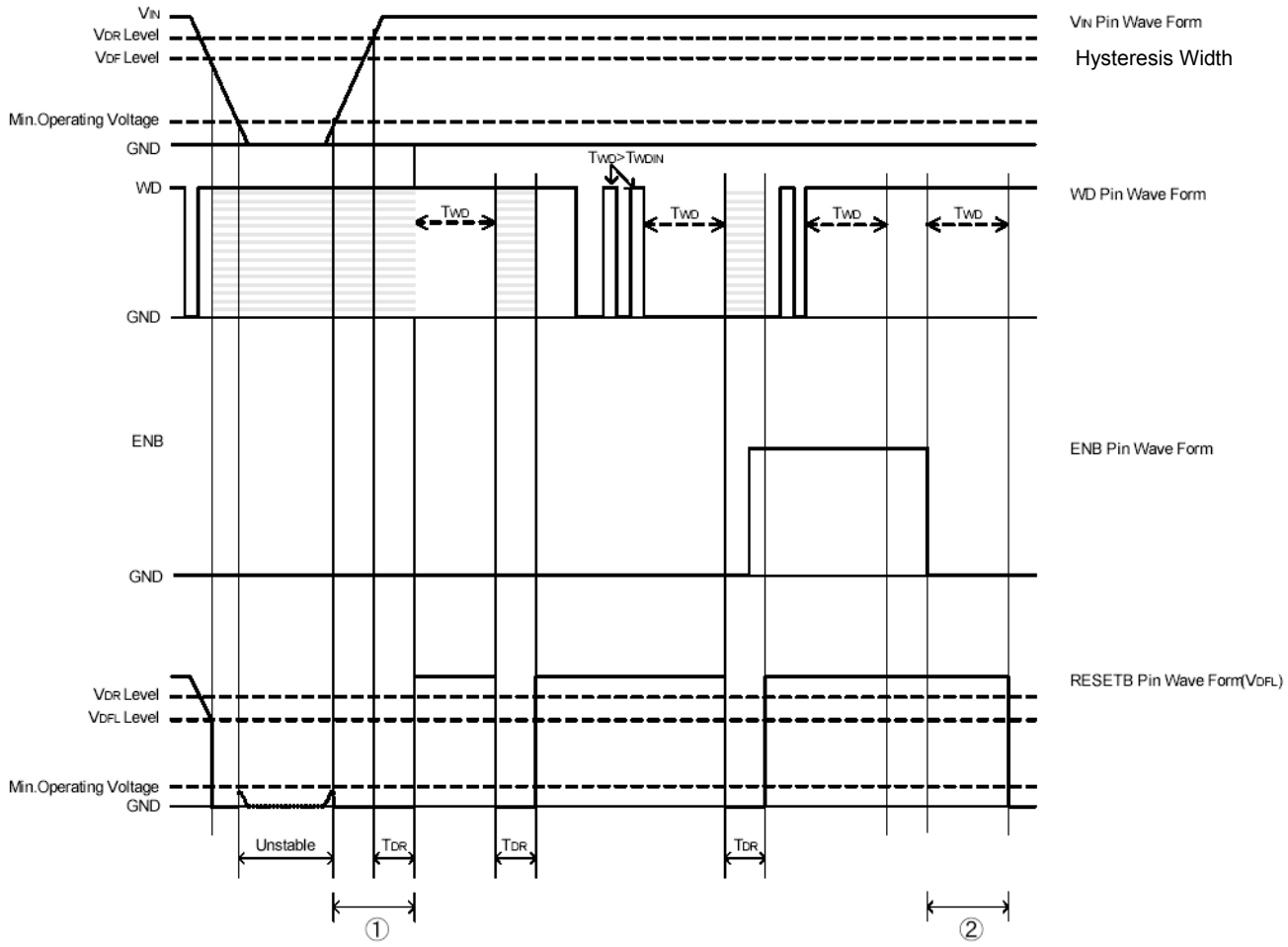
●tDF (N-ch Open Drain Output, Rpull=100kΩ)



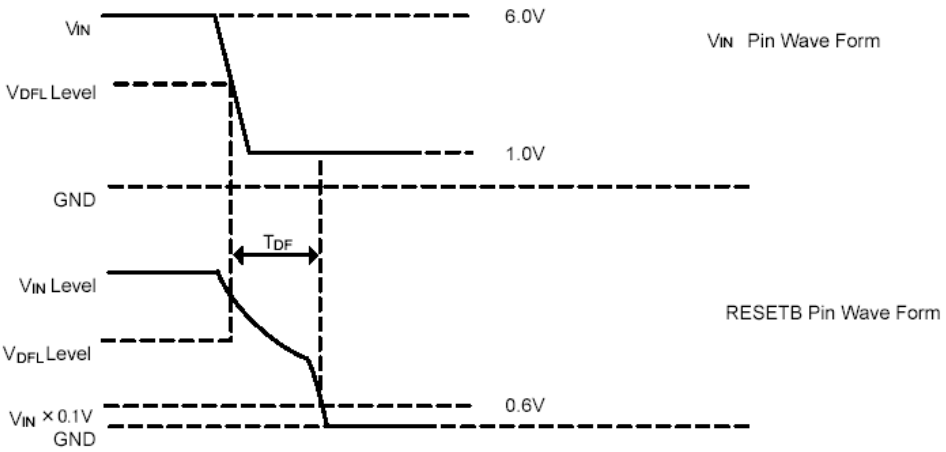
■TIMING CHARTS (Continued)

2. XC6123/XC6124 Series (ENB products)

●N-ch Open Drain Output (Rpull=100kΩ)



●tDF (N-ch Open Drain Output, Rpull=100kΩ)



■NOTES ON USE

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.

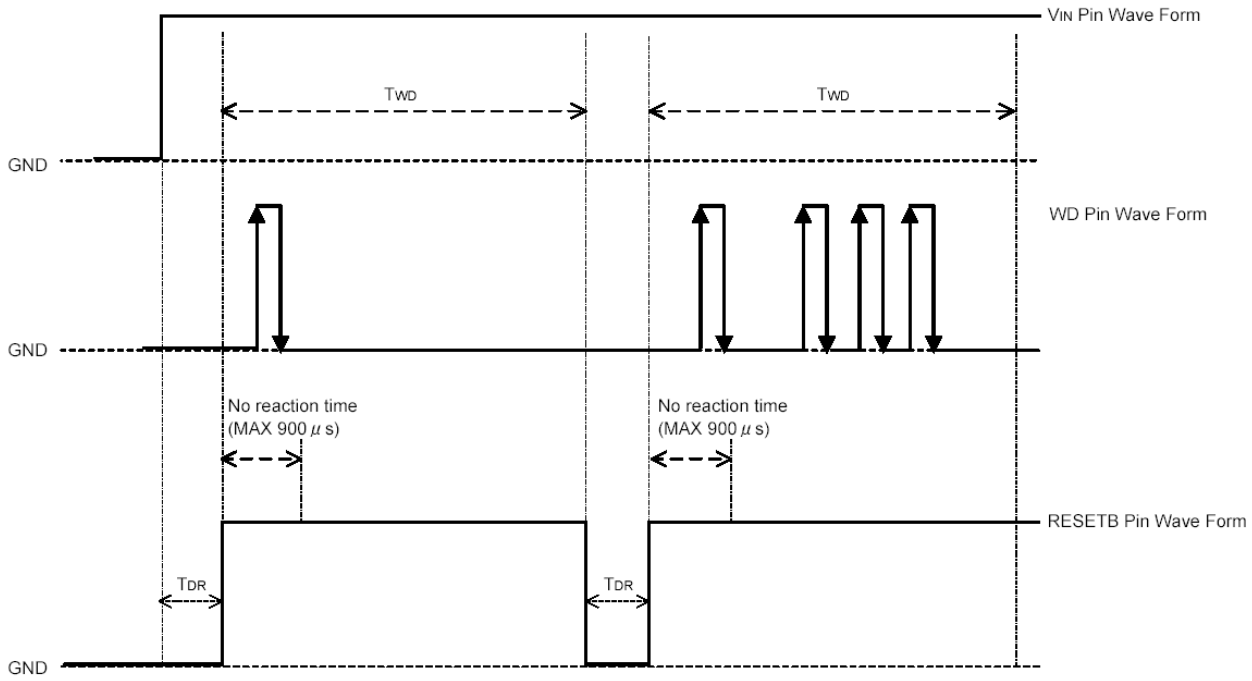
2. When a resistor is connected between the VIN pin and the input, the VIN voltage drops while the IC is operating and a malfunction may occur as a result of the IC's through current.

3. In order to stabilize the IC's operations, please ensure that the VIN pin's input frequency's rise and fall times are more than 1 μ s/V.

4. Noise at the power supply may cause a malfunction of the watchdog operation or the voltage detector. In such case, please strength the line between VIN and the GND pin and connect about 0.22μF of a capacitor between the VIN pin and the GND pin.

5. Protecting against a malfunction while the watchdog time out period, an ignoring time (no reaction time) occurs to the rise and fall times. Referring to the figure below, the ignoring time (no reaction time) lasts for 900μs at maximum.

6. The EN pin of the XC6121 series is not internally pulled up. When using the watchdog function, please drive the EN pin in high level. The EN pin of the XC6122 series is internally pulled up. The watchdog function can be used even the EN pin left open. The ENB pin of the XC6123 series is not internally pulled down. When using the watchdog function, please drive the ENB pin in low level. The ENB pin of the XC6124 series is internally pulled up. The watchdog function can be used even the ENB pin left open.



■PIN LOGIC CONDITIONS

PIN NAME	LOGIC	CONDITIONS	PIN NAME	LOGIC	CONDITIONS
V_{IN}	H	$V_{IN} \geqq V_{DFL}+V_{HYS}$	WD	H	The state maintaining $WD \geqq V_{WDH}$ for more than T_{WD}
	L	$V_{IN} \leqq V_{DFL}$		L	The state maintaining $WD \leqq V_{WDL}$ for more than T_{WD}
EN/ENB	H	EN/ENB≧1.30V		L→H	$V_{WDL} \rightarrow V_{WDH}$, 300ns≦$T_{WDIN}$≦$T_{WD}$
	L	EN/ENB≦0.35V		H→L	$V_{WDH} \rightarrow V_{WDL}$, 300ns≦$T_{WDIN}$≦$T_{WD}$

NOTE:
V_{DFL}: Detect Voltage
V_{HYS}: Hysteresis Range
V_{WDH}: WD High Level Voltage
V_{WDL}: WD Low Level Voltage
T_{WDIN}: WD Pulse Width
T_{WD}: WD Timeout Period
For the details of each parameter, please see the electrical characteristics.

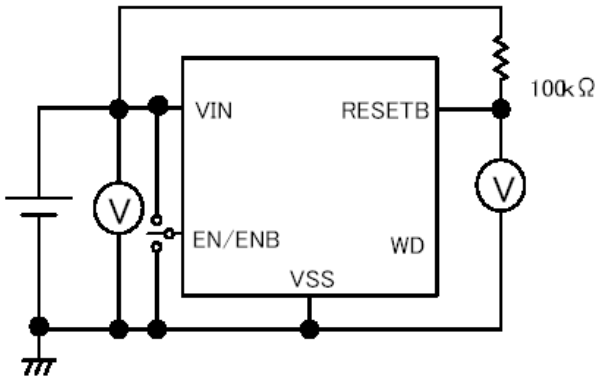
■FUNCTION CHART

V_{IN}	XC6121/XC6122	XC6123/XC6124	WD	RESETB (*2)
	EN	ENB		
H	H	L	H	Repeating detect and release (H→L→H)
			L	
			OPEN	
			L⇔H	H
H	L	H	*1	H
L		L		L

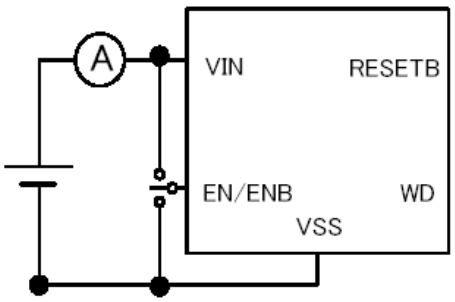
NOTE:
*1: Including all logics of the WD (WD=H, L, OPEN, H→L, L→H).
*2: When the RESETB is High, the circuit is in the release state.
When the RESETB is Low, the circuit is in the detection state.
*3: V_{IN}=L and EN/ENB=H can not be combined because the rated input voltage of the EN/ENB pin is Vss-0.3V to V_{IN}+0.3V.
*4: The RESETB pin becomes indefinite operation while 0.35V<EN/ENB<1.3V.
*5: The EN pin of the XC6121 series is not internally pulled up. When using the watchdog function, please drive the EN pin in high level. The EN pin of the XC6122 series is internally pulled up. The watchdog function can be used even the EN pin left open. The ENB pin of the XC6123 series is not internally pulled down. When using the watchdog function, please drive the ENB pin in low level. The ENB pin of the XC6124 series is internally pulled up. The watchdog function can be used even the ENB pin left open.

■TEST CIRCUITS

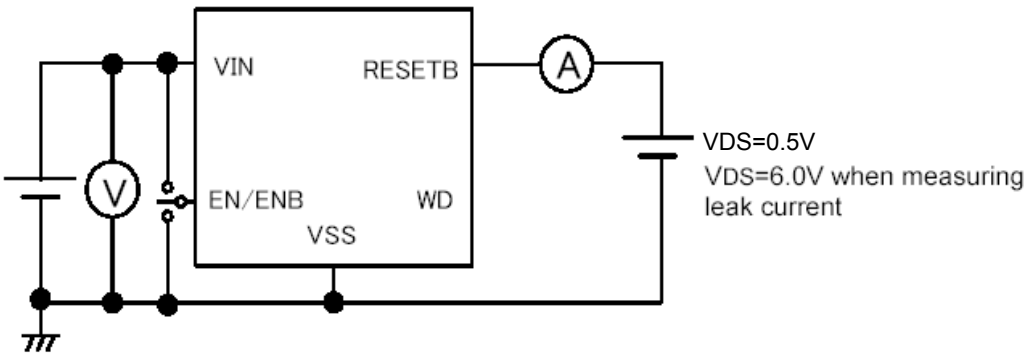
Circuit ①



Circuit ②

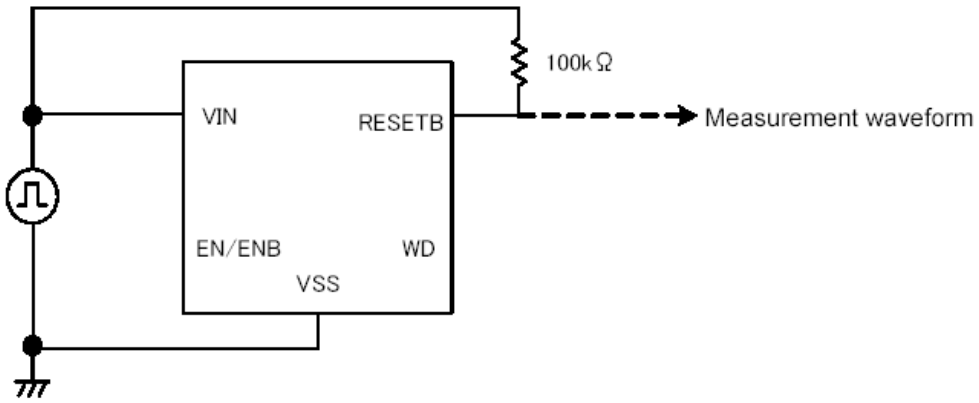


Circuit ③

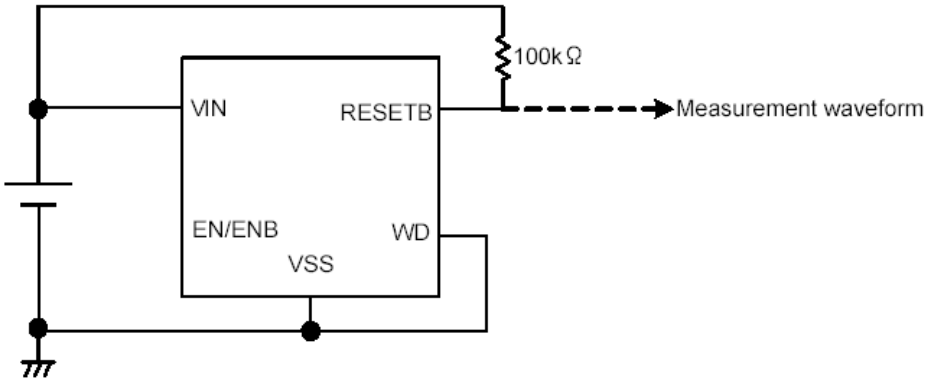


■TEST CIRCUITS (Continued)

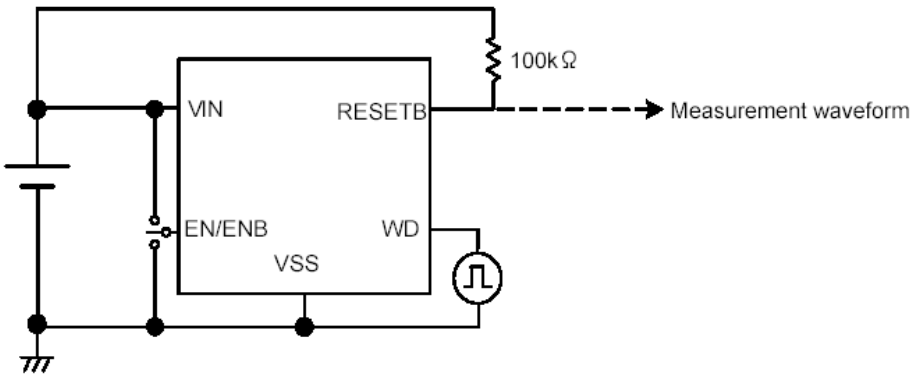
Circuit ④

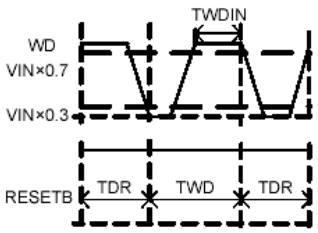


Circuit ⑤



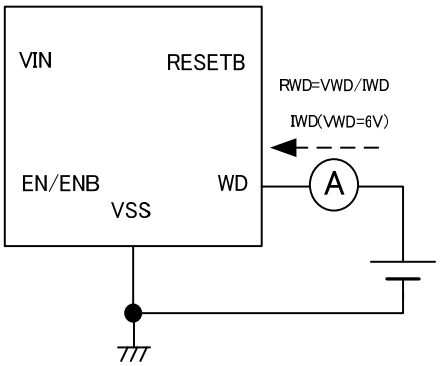
Circuit ⑥



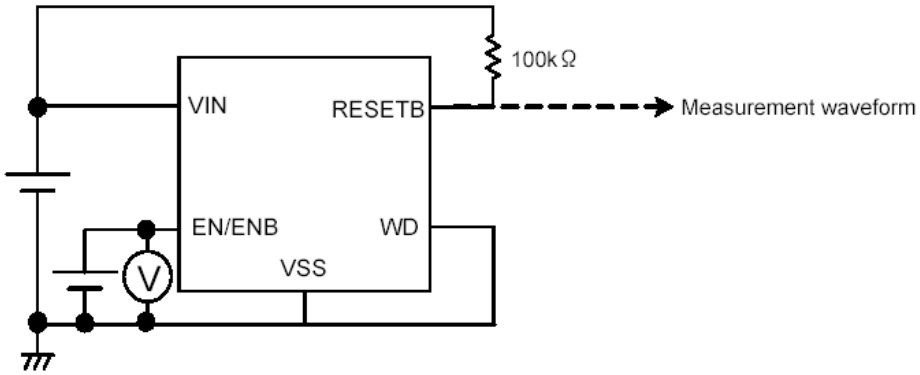


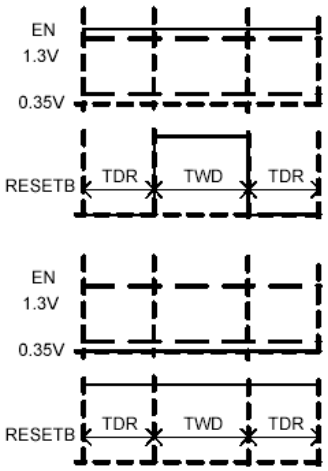
■TEST CIRCUITS (Continued)

Circuit ⑦



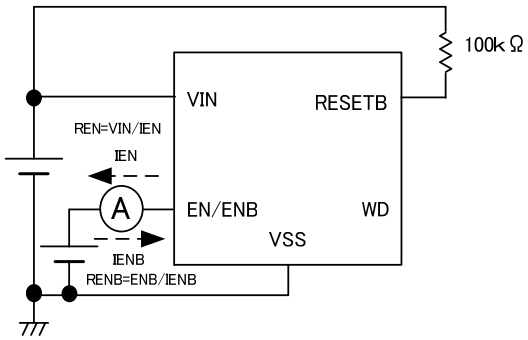
Circuit ⑧





Note:
The above reference is about the EN logic operation.

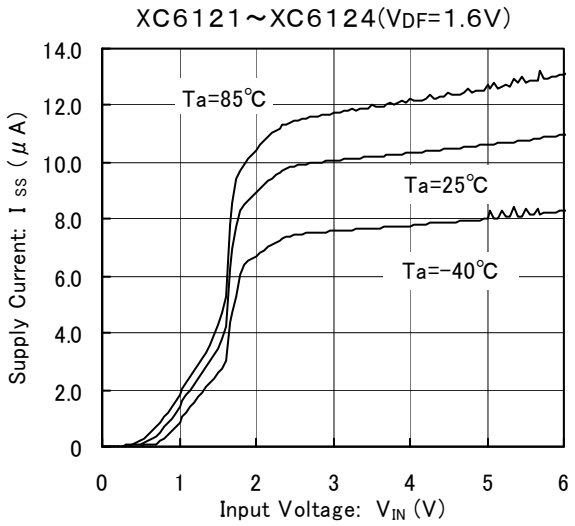
Circuit ⑨

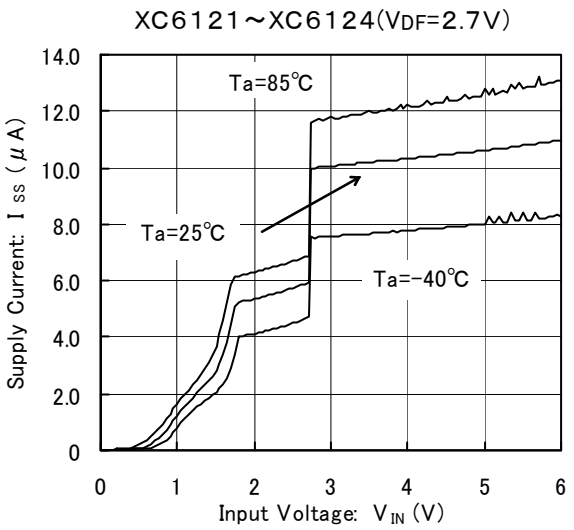


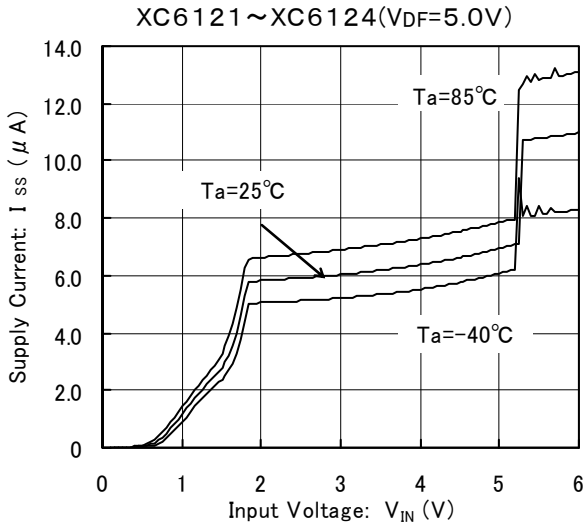
Note:
XC6122 series has EN pin,
XC6124 Series has ENB pin.

■TYPICAL PERFORMANCE CHARACTERISTICS

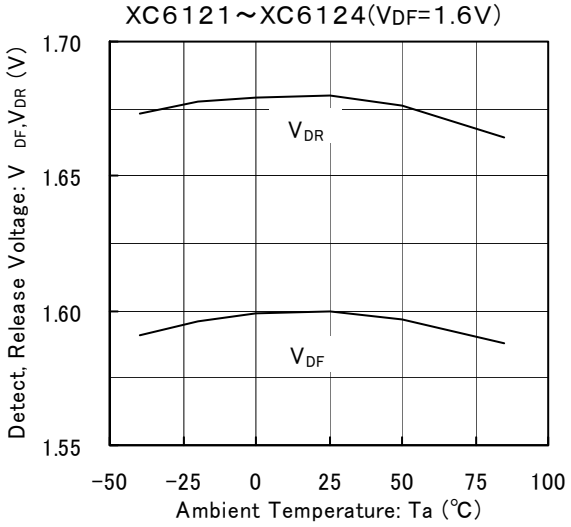
(1.) Supply Current vs. Input Voltage

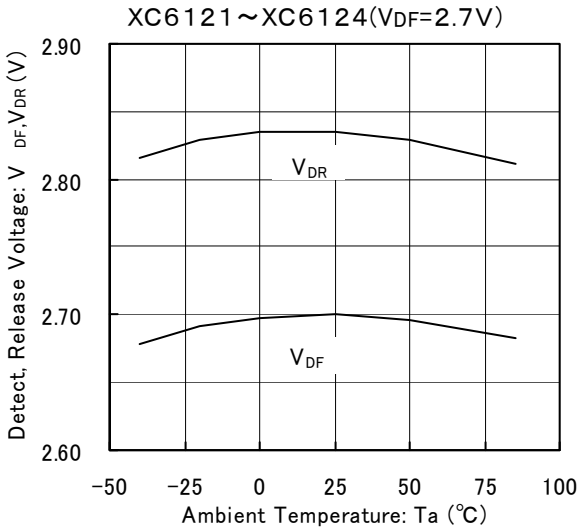






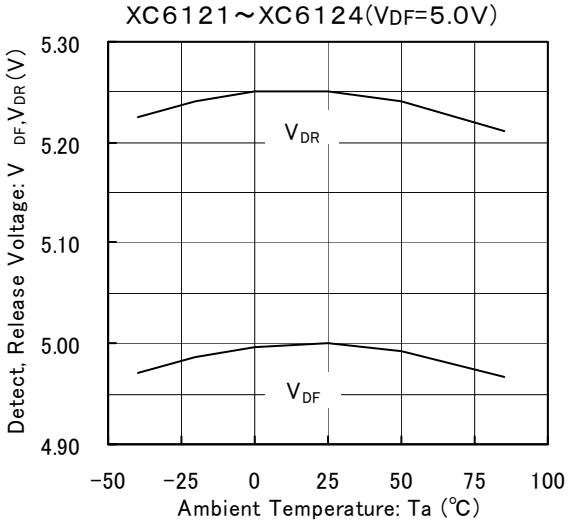
(2.) Detect, Release Voltage vs. Ambient Temperature



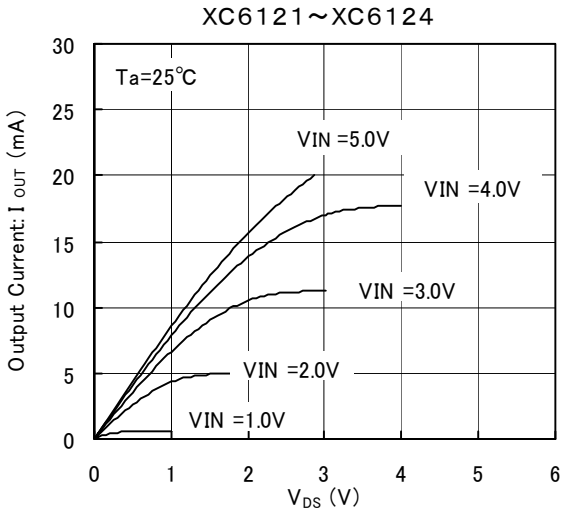


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

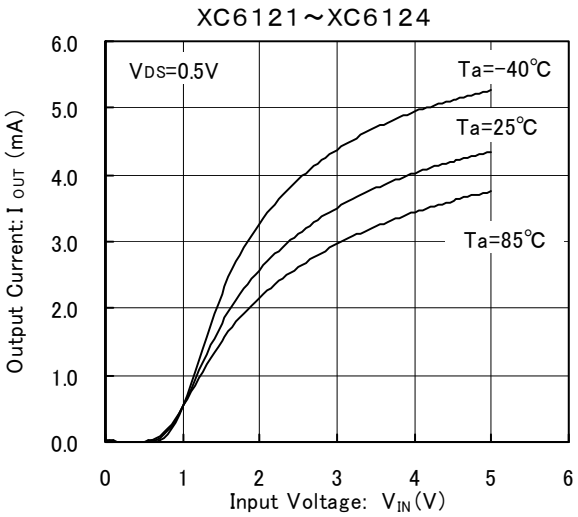
（2.）Detect, Release Voltage vs. Ambient Temperature (Continued)



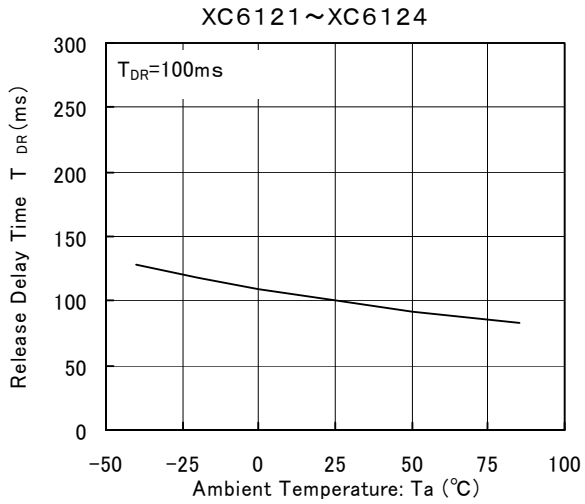
（3.）Nch Driver Output Current vs. VDS

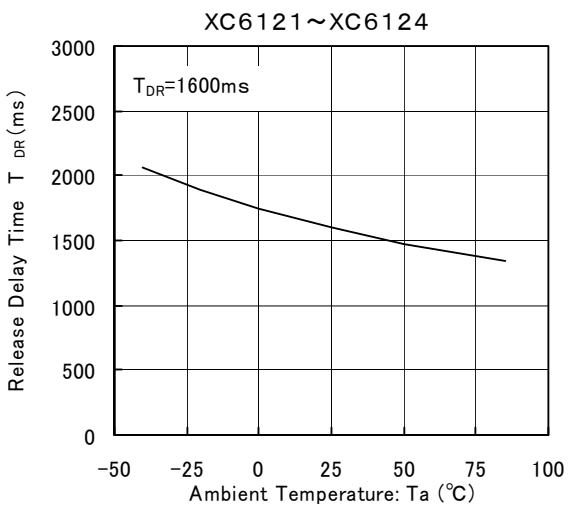


（4.）Driver Output Current vs. Input Voltage



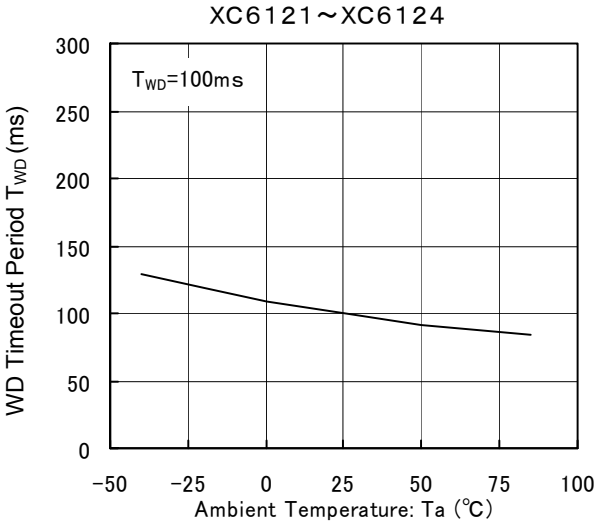
（5.）Release Delay Time vs. Ambient Temperature

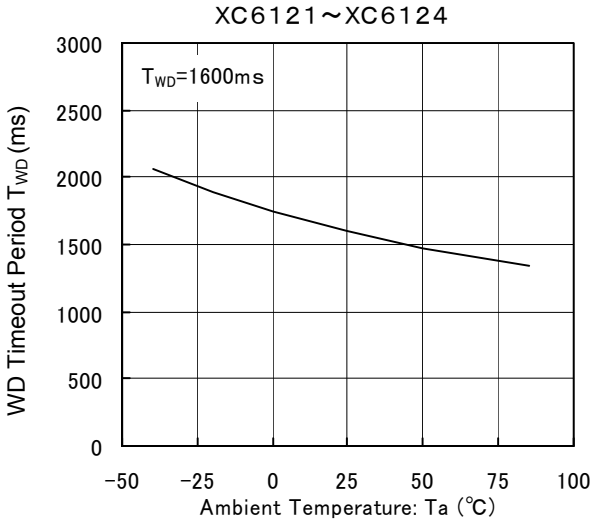




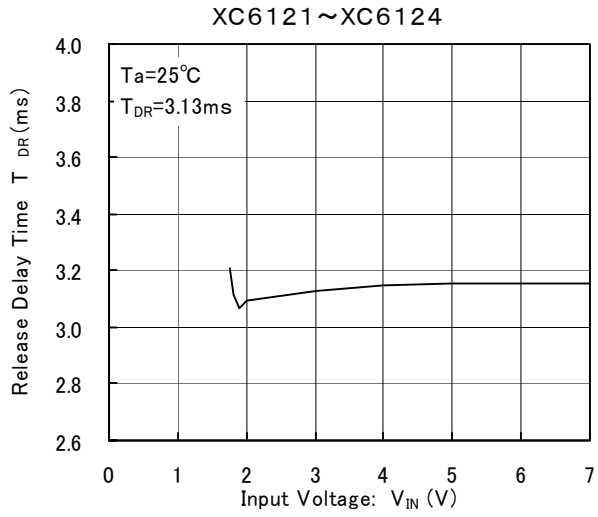
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(6.) Watchdog Timeout Period vs. Ambient Temperature

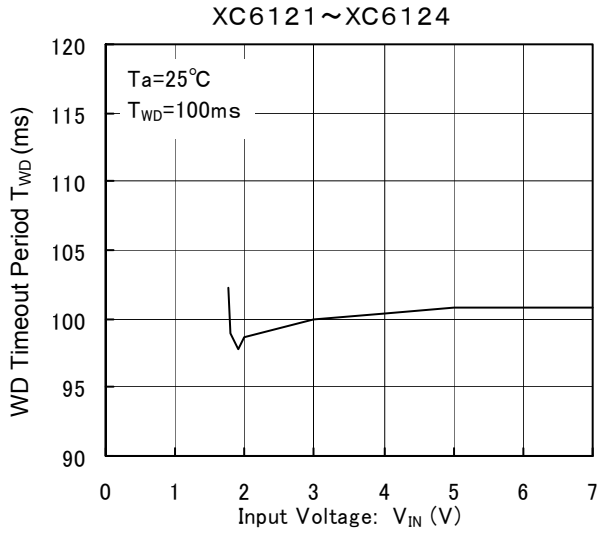




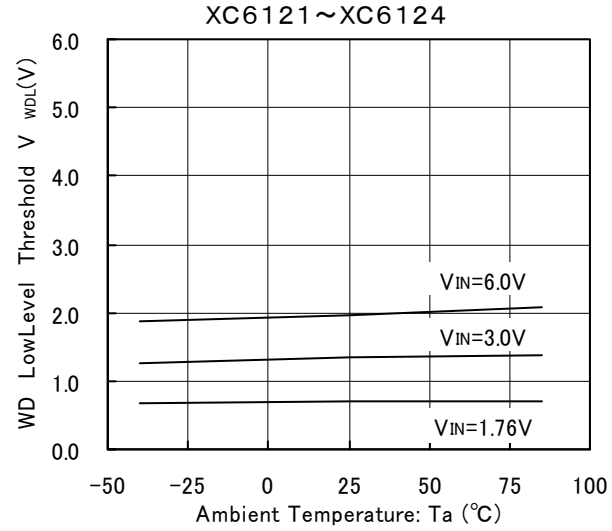
(7.) Release Delay Time vs. Input Voltage



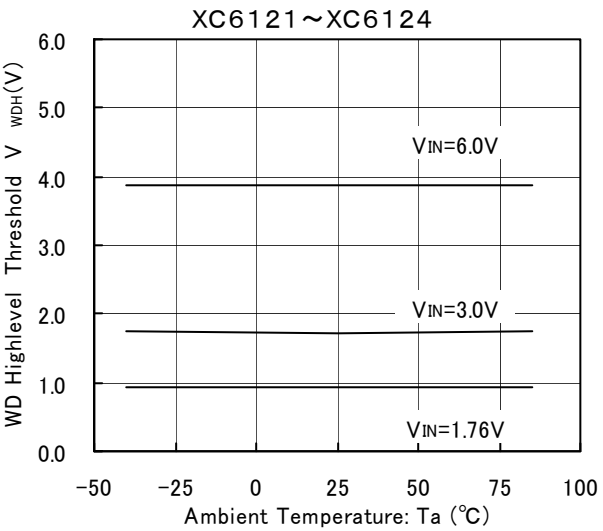
(8.) Watchdog Timeout Period vs. Input Voltage



(9.) Watchdog Low Level Threshould vs. Ambient Temperature

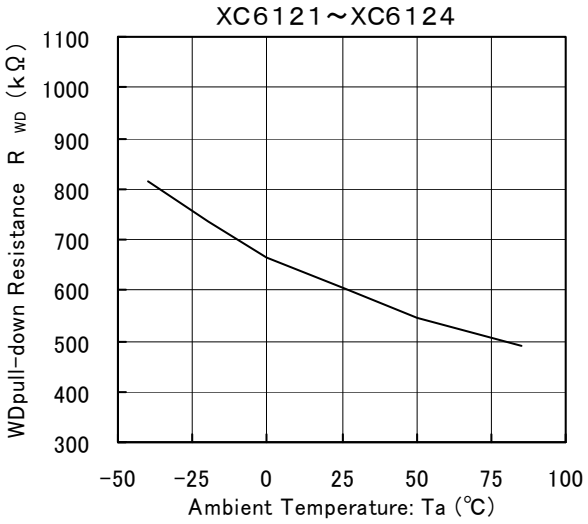


(10.) Watchdog High Level Threshould vs. Ambient Temperature

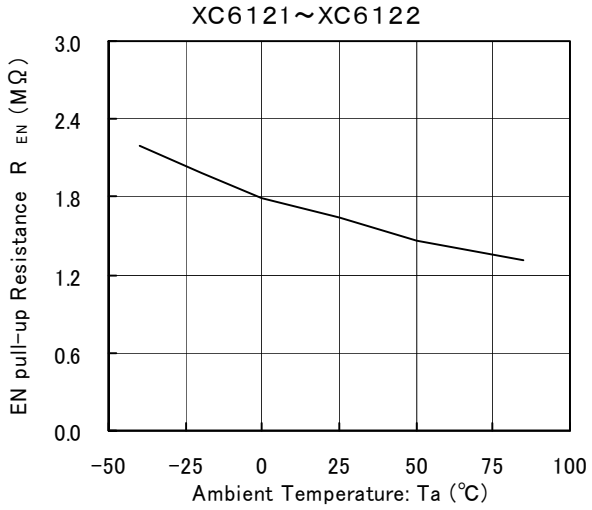


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

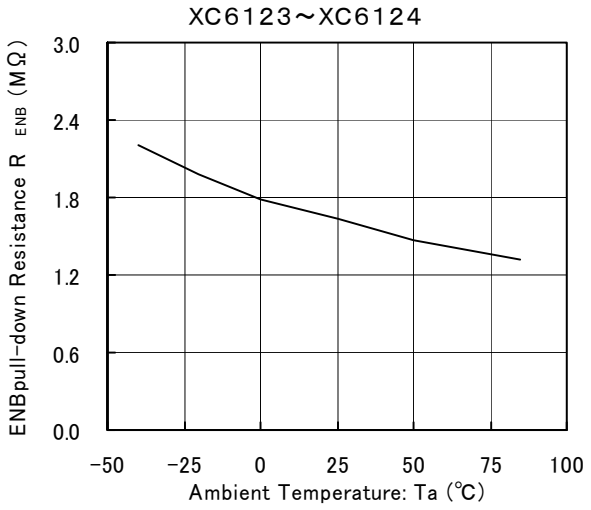
（11.）Watchdog Pull-Down Resistance vs. Ambient Temperature



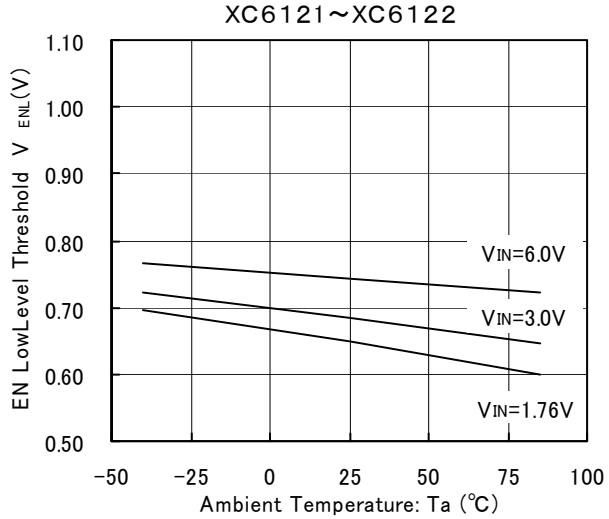
（12.）EN Pull-Up Resistance vs. Ambient Temperature



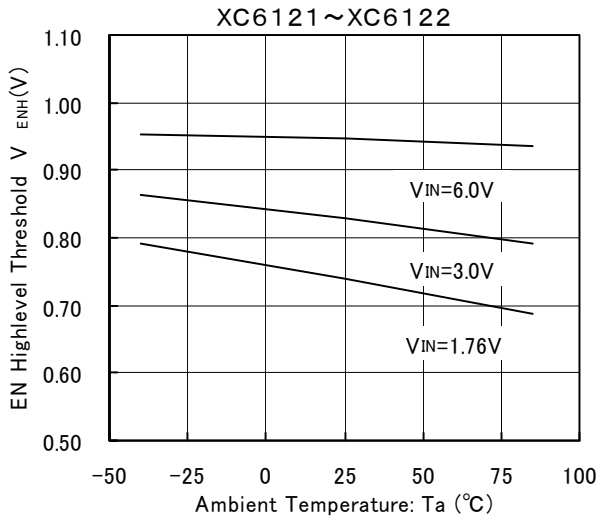
（13.）ENB Pull-Down Resistance vs. Ambient Temperature



（14.）EN Ligh Level Voltage vs. Ambient Temperature

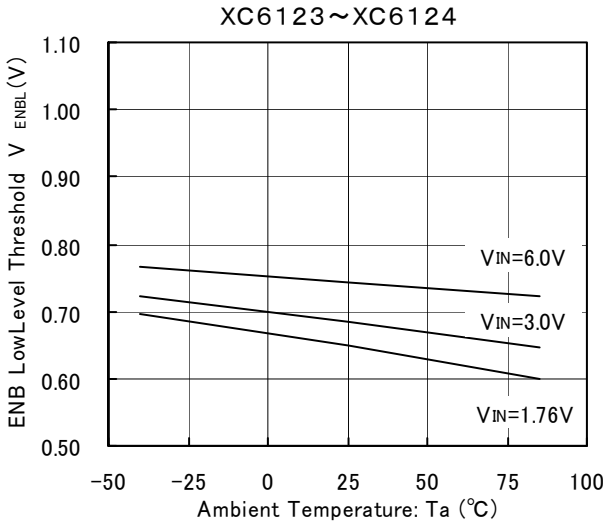


（15.）EN High Level Voltage vs. Ambient Temperature

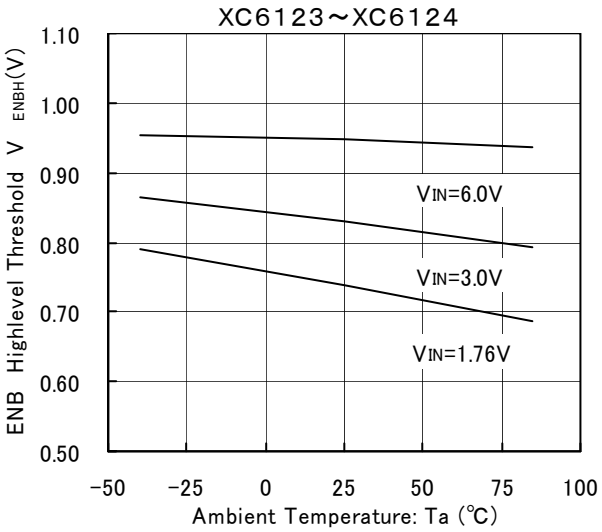


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

（16.）ENB Low Level Voltage vs. Ambient Temperature



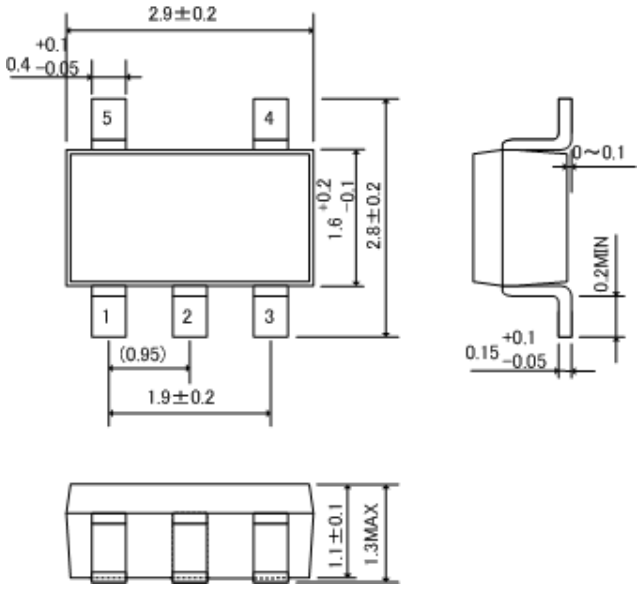
（17.）ENB High Level Voltage vs. Ambient Temperature



■ PACKAGING INFORMATION

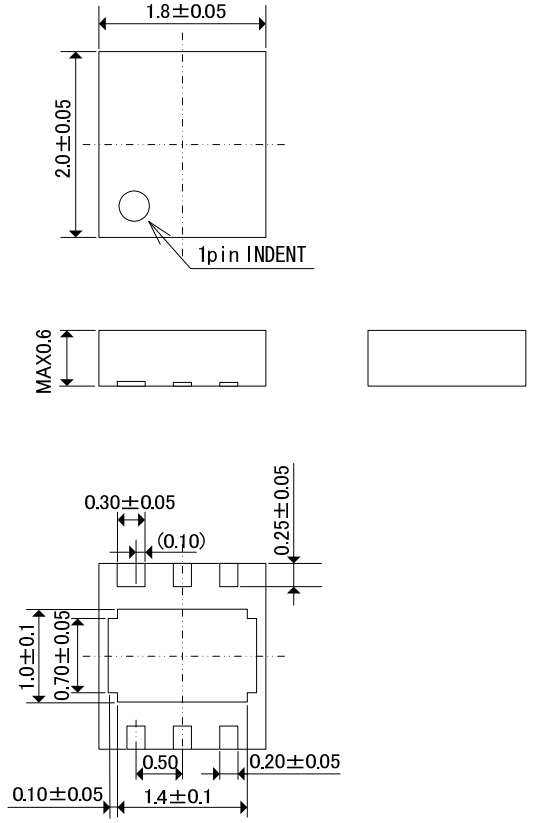
●SOT-25

Unit :mm

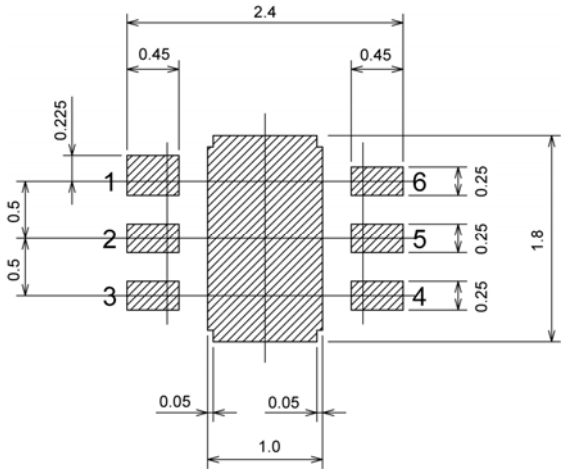


●USP-6C

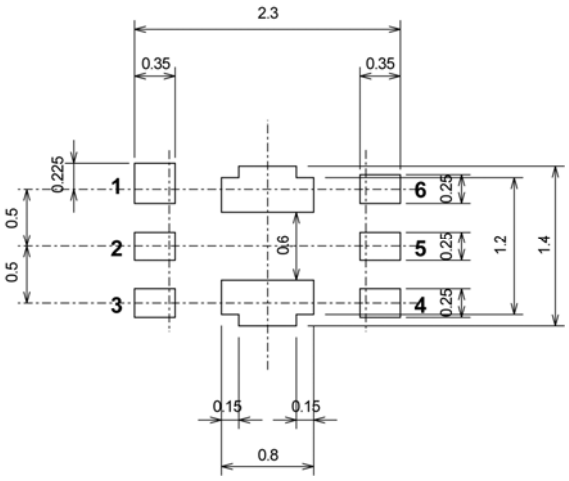
Unit :mm



●USP-6C Reference Pattern Layout



●USP-6C Reference Metal Mask Design



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