ALPHA & OMEGA SEMICONDUCTOR

AOL1436
N-Channel Enhancement Mode Field Effect Transistor

General Description

The AOL1436 uses advanced trench technology to provide excellent $R_{DS(ON)}$, shoot-through immunity and body diode characteristics. This device is ideally suite for use as a High side switch in CPU core power conversion. *Standard Product AOL1436 is Pb-free (meets ROHS & Sony 259 specifications).*

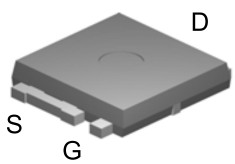
Features

V_{DS} (V) = 25V
I_D = 50A (V_{GS} = 10V)
$R_{DS(ON)}$ < 6mΩ (V_{GS} = 20V)
$R_{DS(ON)}$ < 8.2mΩ (V_{GS} = 12V)
$R_{DS(ON)}$ < 11.5mΩ (V_{GS} = 10V)

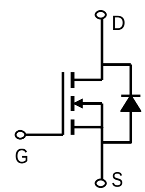
UIS Tested!
Rg,Ciss,Coss,Crss Tested!

Ultra SO-8[TM] Top View

Fits SOIC8 footprint !



Bottom tab connected to drain



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current [B]	T_C=25°C [G]	I_D	50	A
	T_C=100°C		48	
Pulsed Drain Current [C]		I_{DM}	120	
Continuous Drain Current [A]	T_A=25°C	I_{DSM}	20	A
	T_A=70°C		16	
Avalanche Current [C]		I_{AR}	28	A
Repetitive avalanche energy L=0.3mH [C]		E_{AR}	118	mJ
Power Dissipation [B]	T_C=25°C	P_D	43	W
	T_C=100°C		22	
Power Dissipation [A]	T_A=25°C	P_{DSM}	5	W
	T_A=70°C		3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	20	25	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		46	55	°C/W
Maximum Junction-to-Case [D]	Steady-State	$R_{\theta JC}$	2.5	3.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±30V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	2	3.2	4	V
$I_{D(ON)}$	On state drain current	V_{GS}=12V, V_{DS}=5V	120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=20V, I_D=20A		5	6	mΩ
		V_{GS}=12V, I_D=20A		6.6	8.2	mΩ
		V_{GS}=10V, I_D=20A		8.6	11.5	mΩ
		T_J=125°C		11		
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		43		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.72	1	V
I_S	Maximum Body-Diode Continuous Current				50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=12.5V, f=1MHz		1100	1350	pF
C_{oss}	Output Capacitance			420		pF
C_{rss}	Reverse Transfer Capacitance			200		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.8	1.5	Ω
SWITCHING PARAMETERS						
Q_g(12V)	Total Gate Charge	V_{GS}=10V, V_{DS}=12.5V, I_D=20A		20	24	nC
Q_g(10V)	Total Gate Charge			17		
Q_{gs}	Gate Source Charge			6.5		nC
Q_{gd}	Gate Drain Charge			6.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=12.5V, R_L=0.68Ω, R_{GEN}=0.6Ω		9.5		ns
t_r	Turn-On Rise Time			13.5		ns
$t_{D(off)}$	Turn-Off DelayTime			11.5		ns
t_f	Turn-Off Fall Time			5.4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=100A/µs		32		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=100A/µs		19		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on t<10s $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 us pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

Rev1: Jan 2007

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

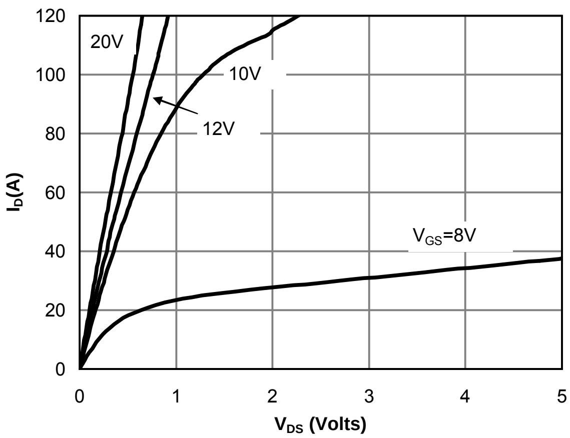


Figure 1: On-Region Characteristics

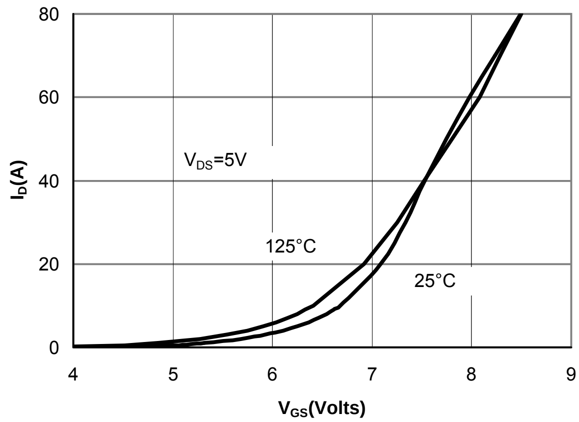


Figure 2: Transfer Characteristics

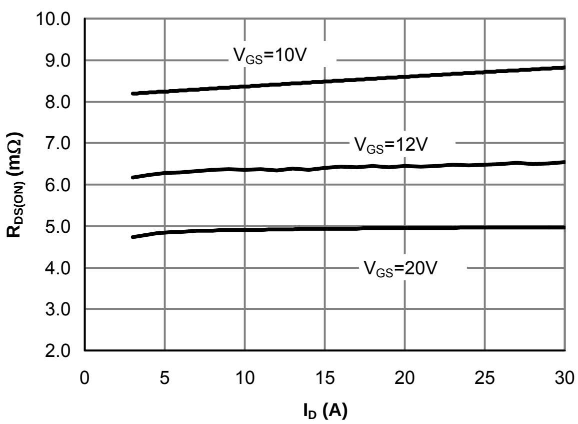


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

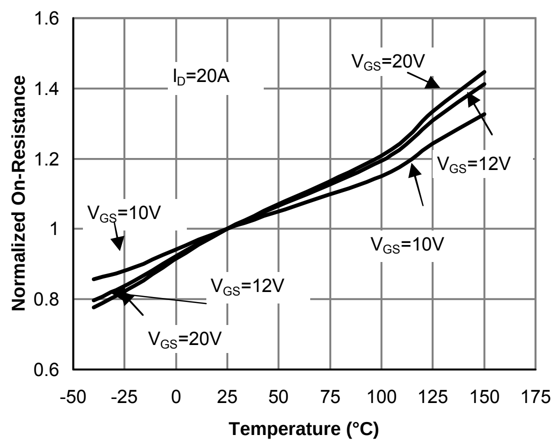


Figure 4: On-Resistance vs. Junction Temperature

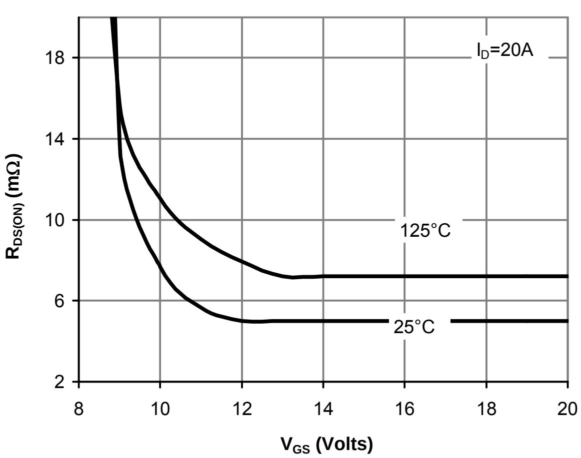


Figure 5: On-Resistance vs. Gate-Source Voltage

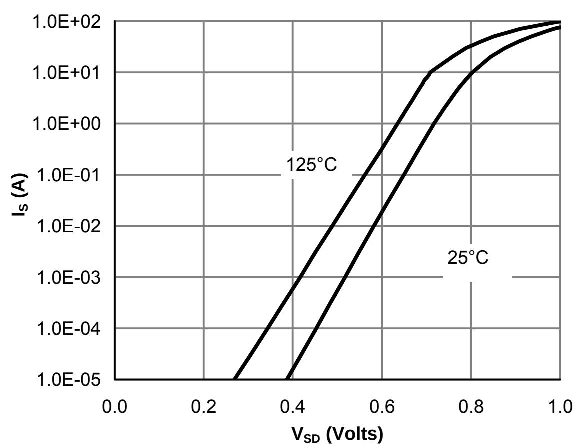


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

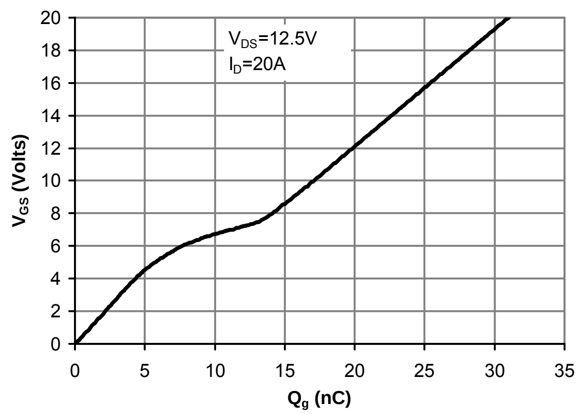


Figure 7: Gate-Charge Characteristics

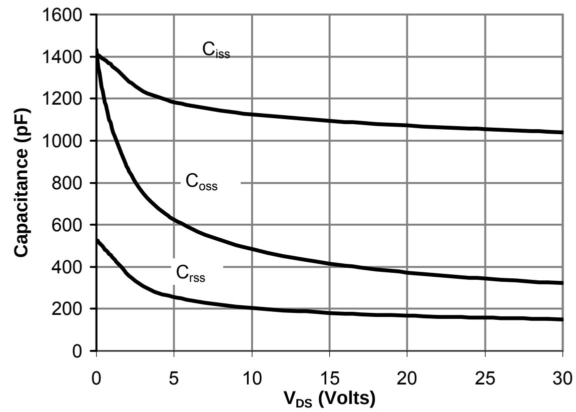


Figure 8: Capacitance Characteristics

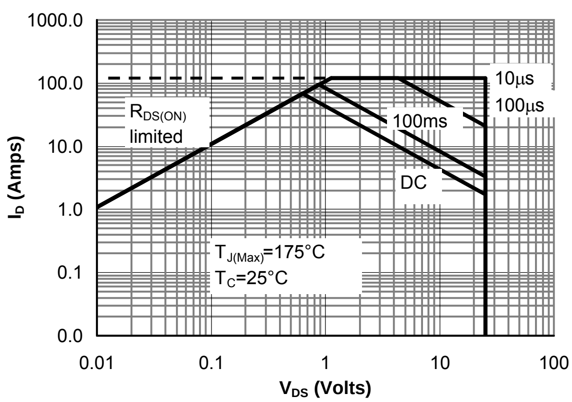


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

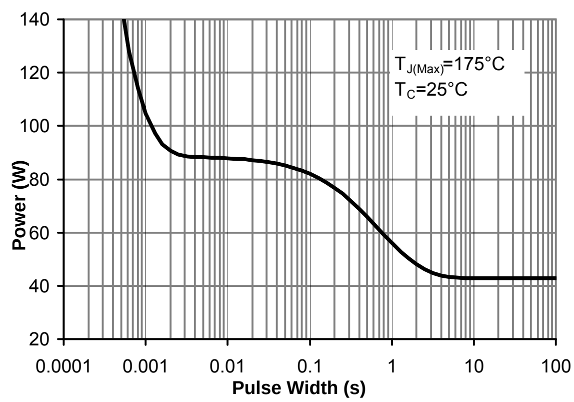


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

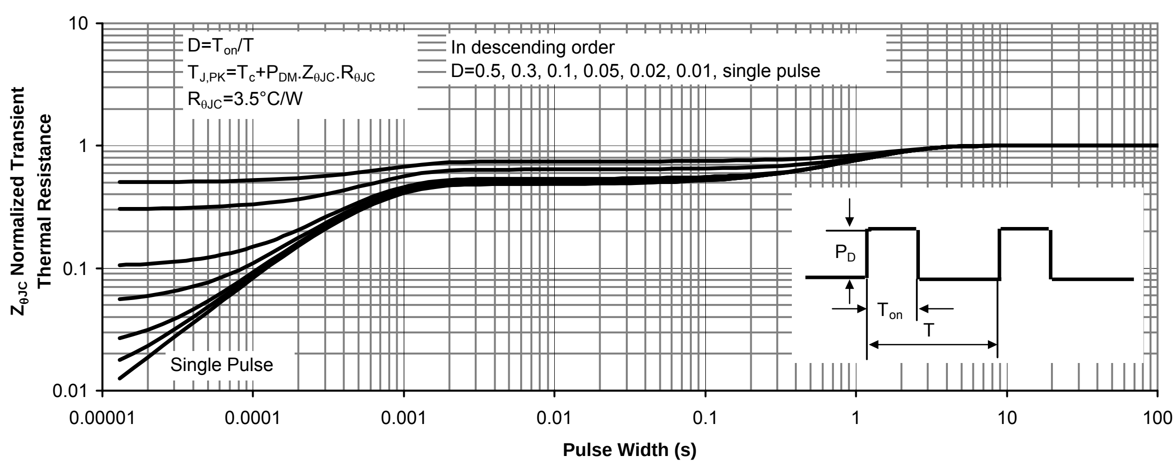


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

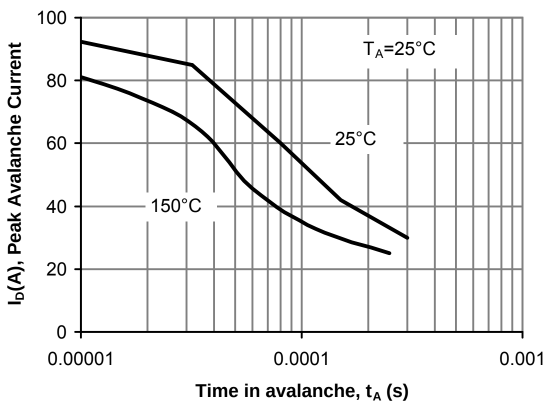


Figure 12: Single Pulse Avalanche capability

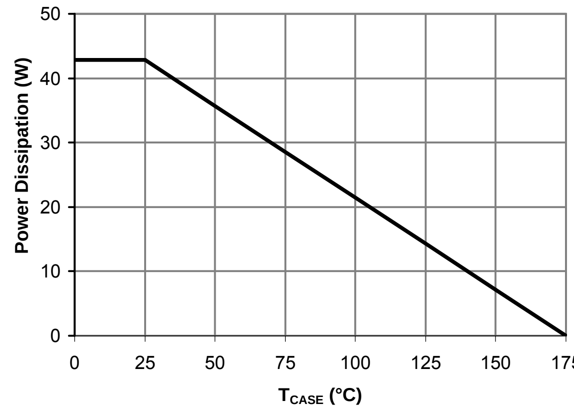


Figure 13: Power De-rating (Note B)

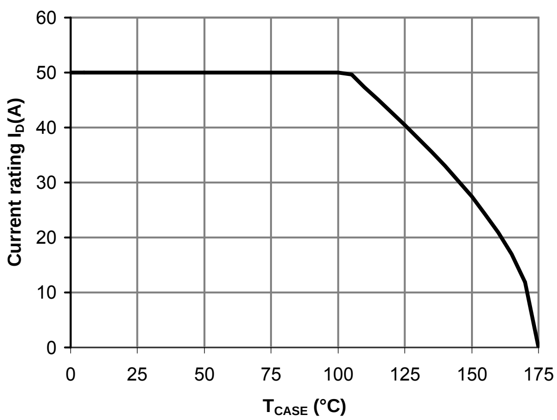


Figure 14: Current De-rating (Note B)

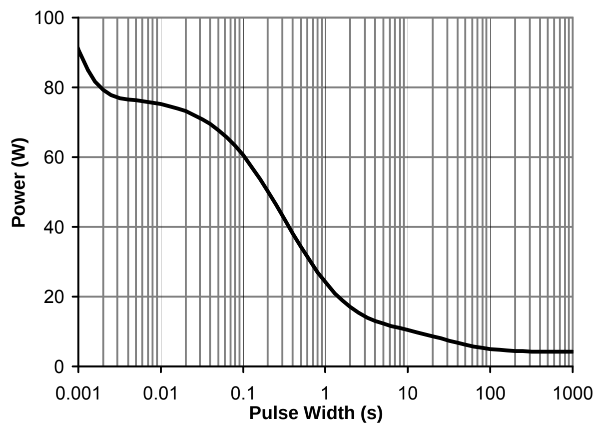


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

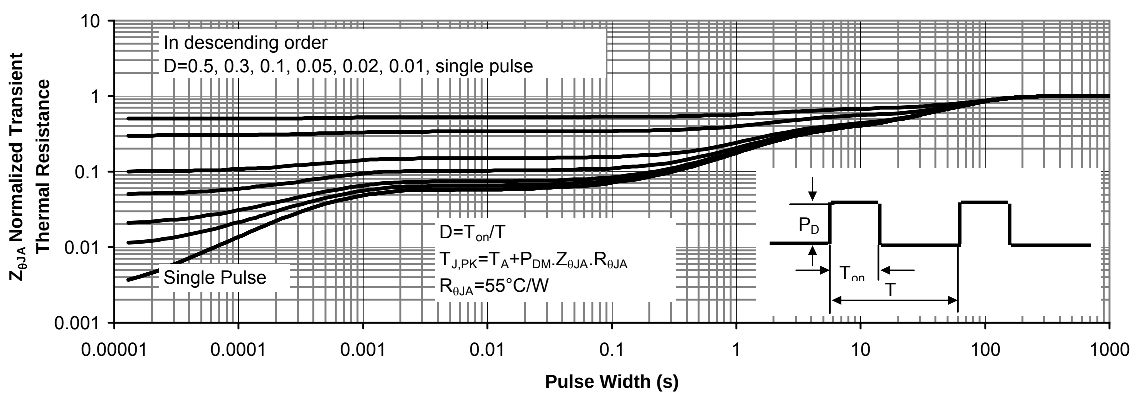


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)