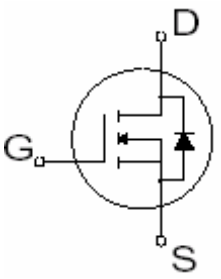
GOOD-ARK

SSFP6N10

StarMOS^T Power MOSFET

- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



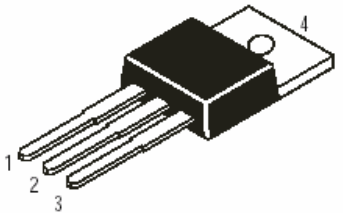
V_{DSS} = 100V

I_{D25} = 5.6A

$R_{DS(ON)}$ = 0. 4 Ω

Description

StarMOS is a new generation of high voltage N–Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1–Gate
Pin2–Drain
Pin1–Source

Application

- Switching application

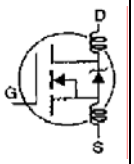
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D@Tc=25˚C	Continuous Drain Current,V_{GS}@10V	5.6	A
I_D@Tc=100˚C	Continuous Drain Current,V_{GS}@10V	4.0	
I_{DM}	Pulsed Drain Current ①	20	
P_D@Tc=25˚C	Power Dissipation	33	W
	Linear Derating Factor	0.22	W/˚C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	63	mJ
I_{AR}	Avalanche Current ①	5.6	A
E_{AR}	Repetitive Avalanche Energy ①	3.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	－55 to +175	℃
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque,6-32 or M3 screw	10 lbf•in(1.1N•m)	

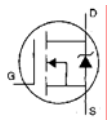
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	4.51	℃/W
$R_{\theta CS}$	Case-to-Sink,Flat,Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62.5	

Electrical Characteristics @T_J=25℃(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS}=0V,I_D=250μA
△$V_{(BR)DSS}$/△T_J	Breakdown Voltage Temp.Coefficient	—	0.11	—	V/℃	Reference to 25℃,I_D=250μA
$R_{DS(on)}$	Static Drain-to-Source On-resistance	—	—	0. 4	Ω	V_{GS}=10V,I_D=2.8A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=5V,I_D=250μA
gfs	Forward Transconductance	—	3.49	—	S	V_{DS}=40V,I_D=2.8A
I_{DSS}	Drain-to-Source Leakage current	—	—	10	μA	V_{DS}=100V,V_{GS}=0V
		—	—	100		V_{DS}=80V,V_{GS}=0V,T_J=150℃
I_{GSS}	Gate-to-Source Forward leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse leakage	—	—	-100		V_{GS}=-20V
Qg	Total Gate Charge	—	8.5	12	nC	ID=5.6A
Qgs	Gate-to-Source charge	—	1.6	—		VDS=80V
Qgd	Gate-to-Drain("Miller") charge	—	4.1	—		VGS=10V See Fig.6 and12④⑤
td(on)	Turn-on Delay Time	—	10	30	nS	V_{DD}=50V
tr	Rise Time	—	14	40		I_D=5.6A
td(off)	Turn-Off Delay Time	—	28	70		R_G=24Ω
tf	Fall Time	—	18	50		See Figure13④⑤
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	13	—		
Ciss	Input Capacitance	—	190	240	pF	V_{GS}=0V
Coss	Output Capacitance	—	55	65		V_{DS}=25V
Crss	Reverse Transfer Capacitance	—	21	25		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	20		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J=25℃,I_S=5.6A,V_{GS}=0V ④
trr	Reverse Recovery Time	—	85	—	nS	T_J=25℃,I_F=5.6A
Qrr	Reverse Recovery Charge	—	0.23	—	nC	di/dt=100A/μs ④
ton	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by Ls + L_D)				

Notes:

① Repetitive rating;pulse width limited by max.junction temperature(see figure 11)

② L =3mH, I_{AS} = 5.6 A, V_{DD} = 25V, R_G = 27Ω, Starting TJ = 25°C

③ I_{SD}≤5.6A,di/dt≤250A/μS,V_{DD}≤$V_{(BR)DSS}$, T_J≤25℃

④ Pulse width=250μS; duty cycle≤2%