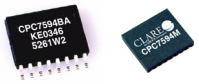
CPC7594

Line Card Access Switch



Features

- TTL logic level inputs for 3.3V logic interfaces
- Smart logic for power up / hot plug state control
- Small 16-pin SOIC or 16-pin DFN Package
- DFN package printed-circuit board footprint is 60 percent smaller than the SOIC version, 70 percent smaller than 4th generation EMR solutions.
- Monolithic IC reliability
- Low matched R_{ON}
- Eliminates the need for zero cross switching
- Flexible switch timing to transition from ringing mode to talk mode.
- Clean, bounce-free switching
- Tertiary protection consisting of integrated current limiting, voltage clamping, and thermal shutdown for SLIC protection
- 5 V operation with power consumption < 10 mW
- Intelligent battery monitor
- Latched logic-level inputs, no external drive circuitry required

Applications

- VoIP Gateways
- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks

Description

The CPC7594 is a member of Clare's next generation Line Card Access Switch family. This monolithic 6-pole solid-state switch is available in either a 16-pin SOIC or a 16-pin DFN package. It provides the necessary functions to replace two 2-Form-C electro-mechanical relays used on traditional analog and contemporary integrated voice and data (IVD) line cards found in Central Office, Access, and PBX equipment. Because this device contains solid state switches for tip and ring line break, ringing injection/return and channel test access, it requires only a +5V supply for operation and TTL logic-level inputs for control.

The CPC7594 is particularly designed for IVD line cards where an EMR is required for line test due to the high frequencies typical of ADSL but solid-state switches are desired for switching and test-in functions.

The CPC7594xC logic differs from the CPC7594xA/B logic by providing a monitor function during the test state.

Ordering Information

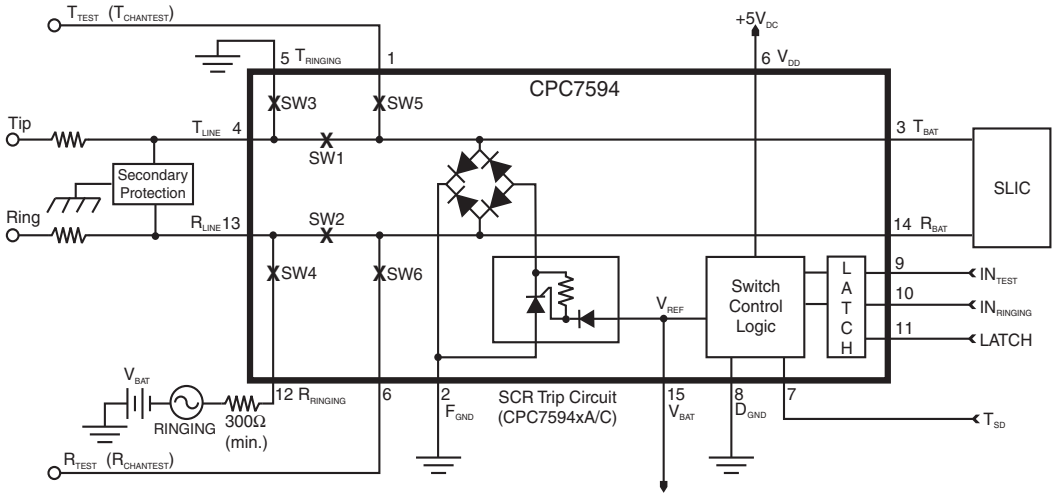
CPC7594 part numbers are specified as shown here:

B - 16-pin SOIC delivered 50/Tube, 1000/Reel
M - 16-pin DFN delivered 52/Tube, 1000/Reel

CPC7594 x x xx — TR - Add for Tape & Reel Version

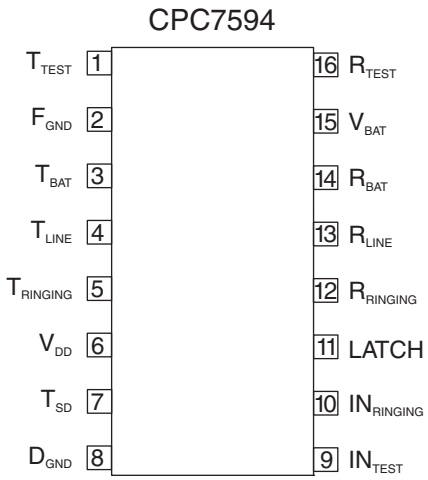
A - With Protection SCR
B - Without Protection SCR
C - With Protection SCR and "Monitor Test State"

Figure 1. CPC7594 Block Diagram



1. Specifications

1.1 Package Pinout



1.2 Pinout

Pin	Name	Description
1	T_{TEST}	Tip lead of the test bus
2	F_{GND}	Fault ground
3	T_{BAT}	Tip lead to the SLIC
4	T_{LINE}	Tip lead of the line side
5	$T_{RINGING}$	Ringing generator return
6	V_{DD}	+5 V supply
7	T_{SD}	Temperature shutdown pin
8	D_{GND}	Digital ground
9	IN_{TEST}	Logic control input
10	$IN_{RINGING}$	Logic control input
11	LATCH	Data latch enable control input
12	$R_{RINGING}$	Ringing generator source
13	R_{LINE}	Ring lead of the line side
14	R_{BAT}	Ring lead to the SLIC
15	V_{BAT}	Battery supply
16	R_{TEST}	Ring lead of the test bus

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
+5 V power supply (V_{DD})	-0.3	7	V
Battery Supply	-	-85	V
D_{GND} to F_{GND} Separation	-5	+5	V
Logic input voltage	-0.3	V_{DD} + 0.3	V
Logic input to switch output isolation	-	320	V
Switch open-contact isolation (SW1, SW2, SW3, SW5, SW6)	-	320	V
Switch open-contact Isolation (SW4)	-	465	V
Operating relative humidity	5	95	%
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C

Absolute maximum electrical ratings are at 25°C.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 ESD Rating

ESD Rating (Human Body Model)
1000 V

1.5 General Conditions

Unless otherwise specified, minimum and maximum values are guaranteed by production testing requirements.

Typical values are characteristic of the device at 25° C and are the result of engineering evaluations. They are provided for information purposes only and are not part of the testing requirements.

Specifications cover the operating temperature range T_A = -40° C to +85° C. Also, unless otherwise specified all testing is performed with V_{DD} = 5 V_{dc}, logic low input voltage is 0 V_{dc} and logic high voltage is 5 V_{dc}.

1.6 Switch Specifications

1.6.1 Break Switches, SW1 and SW2

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW1} (differential) = T_{LINE} to T_{BAT} V_{SW2} (differential) = R_{LINE} to R_{BAT} All-Off state.					
	+25° C, V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 V to -60 V	I_{SW}	-	0.1	1	µA
	+85° C, V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +270 V to -60 V			0.3		
	-40° C, V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
On Resistance	I_{SW}(on) = ±10 mA, ±40 mA, R_{BAT} and T_{BAT} = -2 V					
	+25° C	R_{ON}	-	14.7	-	Ω
	+85° C			21.1	28	
	-40° C			10.7	-	
On Resistance Matching	Per SW1 & SW2 On Resistance test conditions.	ΔR_{ON}	-	0.15	0.8	Ω
DC current limit	V_{SW} (on) = ±10 V, +25° C	I_{SW}	-	300	-	mA
	V_{SW} (on) = ±10 V, +85° C		80	160		
	V_{SW} (on) = ±10 V, -40° C		-	400	425	
Dynamic current limit (t ≤ 0.5 µs)	Break switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	2.5	-	A
Logic input to switch output isolation	+25° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±320 V	I_{SW}	-	0.1	1	µA
	+85° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±330 V		-	0.3		
	-40° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±310 V		-	0.1		
dv/dt sensitivity	-	-	-	500	-	V/µs

1.6.2 Ringing Return Switch, SW3

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW3} (differential) = T_{LINE} to $T_{RINGING}$ All-Off state.					
	+25° C, V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 V to -60 V	I_{SW}	-	0.1	1	µA
	+85° C, V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +270 V to -60 V			0.3		
	-40° C, V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
On Resistance	I_{SW}(on) = ±0 mA, ±10 mA, +25° C	R_{ON}	-	51	-	Ω
	I_{SW}(on) = ±0 mA, ±10 mA, +85° C			75	100	
	I_{SW}(on) = ±0 mA, ±10 mA, -40° C			39	-	
DC current limit	V_{SW} (on) = ± 10 V, +25° C	I_{SW}	-	135	-	mA
	V_{SW} (on) = ± 10 V, +85° C		70	85		
	V_{SW} (on) = ± 10 V, -40° C		-	210		
Dynamic current limit (t ≤ 0.5 µs)	Ringing switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	2.5	-	A
Logic input to switch output isolation	+25° C, Logic inputs = gnd, V_{SW} ($T_{RINGING}$, T_{LINE}) = ±320 V	I_{SW}	-	0.1	1	µA
	+85° C, Logic inputs = gnd, V_{SW} ($T_{RINGING}$, T_{LINE}) = ±330 V			0.3		
	-40° C, Logic inputs = gnd, V_{SW} ($T_{RINGING}$, T_{LINE}) = ±310 V			0.1		
dv/dt sensitivity	-	-	-	500	-	V/µs

1.6.3 Ringing Switch, SW4

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW4} (differential) = R_{LINE} to $R_{RINGING}$ All-Off state.					
	+25° C V_{SW} (differential) = -255 V to +210 V V_{SW} (differential) = +255 V to -210 V	I_{SW}	-	0.05	1	µA
	+85° C V_{SW} (differential) = -270 V to +210 V V_{SW} (differential) = +270 V to -210 V			0.1		
	-40° C V_{SW} (differential) = -245 V to +210 V V_{SW} (differential) = +245 V to -210 V			0.05		
On Resistance	I_{SW} (on) = ±70 mA, ±80 mA	R_{ON}	-	6	15	Ω
On Voltage	I_{SW} (on) = ± 1 mA	V_{ON}	-	1.5	3	V
On-State Leakage Current	Inputs set for ringing -Measure ringing generator current to ground.	$I_{RINGING}$	-	0.1	0.25	mA
Steady-State Current*	Inputs set for ringing mode.	I_{SW}	-	-	150	mA
Surge Current*	Ringing switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	-	2	A
Release Current	SW4 transition from on to off.	$I_{RINGING}$	-	420	-	µA
Logic input to switch output isolation	+25° C, Logic inputs = gnd, V_{SW} ($R_{RINGING}$, R_{LINE}) = ±320 V	I_{SW}	-	0.10	1	µA
	+85° C, Logic inputs = gnd, V_{SW} ($R_{RINGING}$, R_{LINE}) = ±330 V			0.12		
	-40° C, Logic inputs = gnd, V_{SW} ($R_{RINGING}$, R_{LINE}) = ±310 V			0.10		
dv/dt sensitivity	-	-	-	500	-	V/µs

**Secondary protection and current limiting must prevent exceeding this parameter.*

1.6.4 Test Switches, SW5 and SW6

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW1} (differential) = T_{TEST} to T_{BAT} V_{SW2} (differential) = R_{TEST} to R_{BAT} All-Off state.					
	+25° C, V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 V to -60 V	I_{SW}	-	0.1	1	µA
	+85° C, V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +270 V to -60 V			0.2		
	-40° C, V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
On Resistance	I_{SW}(on) = ±10 mA, ±40 mA, R_{BAT} and T_{BAT} = -2 V					
	+25° C	R_{ON}	-	38	-	Ω
	+85° C			46	70	
	-40° C			28	-	
DC current limit	V_{SW} (on) = ±10 V, +25° C	I_{SW}	-	125	-	mA
	V_{SW} (on) = ±10 V, +85° C		80	95		
	V_{SW} (on) = ±10 V, -40° C		-	165	250	
Dynamic current limit ($t \leq 0.5$ µs)	Break switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	2.5	-	A
Logic input to switch output isolation	+25° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±320 V	I_{SW}	-	0.1	1	µA
	+85° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±330 V		-	0.3		
	-40° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±310 V		-	0.1		
dv/dt sensitivity	-	-	-	500	-	V/µs

1.7 Digital I/O Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input Characteristics						
Input voltage, Logic low	Input voltage falling	V_{IL}	0.8	1.0	-	V
Input voltage, Logic high	Input voltage rising	V_{IH}		1.7	2.0	
Input leakage current, $IN_{RINGING}$ and IN_{TEST}, Logic high	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{HI} = 2.4 V	I_{IH}	-	0.1	1	µA
Input leakage current, $IN_{RINGING}$ and IN_{TEST}, Logic low	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IL} = 0.4 V	I_{IL}	-	0.1	1	µA
Input leakage current, LATCH Logic high	V_{DD} = 4.5 V, V_{BAT} = -75 V, V_{IH} = 2.4 V	I_{IH}	7	19	-	µA
LATCH Pull-up Minimum Load	V_{DD} = 4.5 V, V_{BAT} = -75 V, I_{IN} = -10 µA Latch input transitions to logic high.	Logic = High	True			
Input leakage current, LATCH Logic low	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IL} = 0.4 V	I_{IL}	-	46	125	µA
Input leakage current, T_{SD} Logic high	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IH} = 2.4 V	I_{IH}	10	16	30	µA
Input leakage current, T_{SD} Logic low	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IL} = 0.4 V	I_{IL}	10	16	30	µA
Output Characteristics						
Output voltage, T_{SD} Logic high	V_{DD} = 5.5 V, V_{BAT} = -75 V, I_{TSD} = 10µA	V_{TSD_off}	2.4	V_{DD}	-	V
Output voltage, T_{SD} Logic low	V_{DD} = 5.5 V, V_{BAT} = -75 V, I_{TSD} = 1mA	V_{TSD_on}	-	0	0.4	V

1.8 Voltage and Power Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Voltage Requirements						
V_{DD}	-	V_{DD}	4.5	5.0	5.5	V
V_{BAT}[1]	-	V_{BAT}	-19	-48	-72	V
[1] V_{BAT} is used only for internal protection circuitry. If V_{BAT} rises above-10 V, the device will enter the all-off state and will remain in the all-off state until the battery drops below approximately -15 V						
Power Specifications						
Power consumption	V_{DD} = 5 V, V_{BAT} = -48 V, Measure I_{DD} and I_{BAT},					
	Talk and All-Off States	P	-	5.5	10	mW
	All other states	P	-	6.5	10	mW
V_{DD} current	V_{DD} = 5 V, V_{BAT} = -48 V					
	Talk and All-Off states	I_{DD}		1.1	2.0	mA
	Ringing and Test states	I_{DD}	-	1.3	2.0	mA
V_{BAT} current	V_{DD} = 5 V, V_{BAT} = -72 V, All states	I_{BAT}	-	0.1	10	µA

1.9 Protection Circuitry Electrical Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Protection Diode Bridge						
Forward Voltage drop, continuous current (50/60 Hz)	Apply ± dc current limit of break switches	V_F	-	2.1	3.0	V
Forward Voltage drop, surge current	Apply ± dynamic current limit of break switches	V_F	-	5	-	
Protection SCR (CPC7594xA and CPC7594xC)						
Surge current	-	-	-	-	*	A
Trigger current: Current into V_{BAT} pin.	SCR activates, +25° C	I_{TRIG}	-	134	-	mA
	SCR activates, +85° C			87		
Hold current: Current through protection SCR	SCR remains active, +25° C	I_{HOLD}	-	250	-	mA
	SCR remains active, +85° C		110	184		
Gate trigger voltage	$I_{GATE} = I_{TRIGGER}$§	V_{TBAT} or V_{RBAT}	V_{BAT} -4	-	V_{BAT} -2	V
Reverse leakage current	V_{BAT} = -48 V	I_{VBAT}	-	0.02	1.0	µA
On-state voltage	0.5 A, t = 0.5 µs	V_{TBAT} or V_{RBAT}	-	-3	-	V
	2.0 A, t = 0.5 µs			-5		
Temperature Shutdown Specifications						
Shutdown activation temperature	Not production tested - limits are guaranteed by design and Quality Control sampling audits.	T_{TSD_on}	110	125	150	°C
Shutdown circuit hysteresis		T_{TSD_off}	10	-	25	°C

*Passes GR1089 and ITU-T K.20 with appropriate secondary protection in place.
§V_{BAT} must be capable of sourcing $I_{TRIGGER}$ for the internal SCR to activate.

1.10 Truth Tables

1.10.1 CPC7594xA and CPC7594xB Truth Table

State	$IN_{RINGING}$	IN_{TEST}	LATCH	T_{SD}	Break Switches	Ringing Switches	Test Switches
Talk	0	0	0	Z [1]	On	Off	Off
Test	0	1			Off	Off	On
Ringing	1	0			Off	On	Off
All-Off	1	1			Off	Off	Off
Latched	X	X	1		Unchanged		
All-Off	X	X	X	0	Off	Off	Off

[1] Z = High Impedance. Because T_{SD} has an internal pull up at this pin, it should be controlled with an open-collector or open-drain type device.

1.10.2 CPC7594xC Truth Table

State	$IN_{RINGING}$	IN_{TEST}	LATCH	T_{SD}	Break Switches	Ringing Switches	Test Switches
Talk	0	0	0	Z [1]	On	Off	Off
Test/Monitor	0	1			On	Off	On
Ringing	1	0			Off	On	Off
All-Off	1	1			Off	Off	Off
Latched	X	X	1		Unchanged		
All-Off	X	X	X	0	Off	Off	Off

[1] Z = High Impedance. Because T_{SD} has an internal pull up at this pin, it should be controlled with an open-collector or open-drain type device.

2. Functional Description

2.1 Introduction

2.1.1 CPC7594xA and CPC7594xB Logic States

- **Talk**. Break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.
- **Ringing**. Break switches SW1 and SW2 open, ringing switches SW3 and SW4 closed, and test switches SW5 and SW6 open.
- **Test**. Break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and channel test switches SW5 and SW6 closed.
- **All-off**. Break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.

2.1.2 CPC7594xC Logic States

The CPC7594xC replaces the Test state with the Test/Monitor state as defined below.

- **Test/Monitor**. Break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 closed.

The CPC7594 offers break-before-make and make-before-break switching from the ringing state to the talk state with simple TTL level logic input control. Solid-state switch construction means no impulse noise is generated when switching during ring cadence or ring trip, eliminating the need for external zero-cross switching circuitry. State control is via TTL logic-level input so no additional driver circuitry is required. The linear break switches SW1 and SW2 have exceptionally low R_{ON} and excellent matching characteristics. The ringing switch, SW4, has a minimum open contact breakdown voltage of 465 V at +25°C sufficiently high with proper protection to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Integrated into the CPC7594 is an over-voltage clamping circuit, active current limiting, and a thermal shutdown mechanism to provide protection for the SLIC during a fault condition. Positive and negative lightning surge currents are reduced by the current limiting circuitry and hazardous potentials are diverted away from the SLIC via the protection diode bridge or the optional integrated protection SCR. Power-cross potentials are also reduced by the current limiting and thermal shutdown circuits.

To protect the CPC7594 from an over-voltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the tip and ring terminals to a level below the maximum breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is highly recommended. With proper selection of the secondary protector, a line card using the CPC7594 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

The CPC7594 operates from a single +5 V supply. This gives the device extremely low power consumption in any state with virtually any range of battery voltage. The battery voltage used by the CPC7594 has a two fold function. It is used as a reference and as a current source for the internal integrated protection circuitry under surge conditions. Second, it is used as a reference. In the event of battery voltage loss, the CPC7594 enters the all-off state.

2.2 Under Voltage Switch Lock Out Circuitry

2.2.1 Introduction

Smart logic in the CPC7594 now provides for switch state control during both power up and power loss transitions. An internal detector is used to evaluate the V_{DD} supply to determine when to de-assert the under voltage switch lock out circuitry with a rising V_{DD} and when to assert the under voltage switch lock out circuitry with a falling V_{DD}. Any time unsatisfactory low V_{DD} conditions exist the lock out circuit overrides user switch control by blocking the information at the external input pins and conditioning internal switch commands to the all off state. Upon restoration of V_{DD} the switches will remain in the all-off state until the LATCH input is pulled low.

The rising V_{DD} lock out release threshold is internally set to ensure all internal logic is properly biased and functional before accepting external switch commands from the inputs to control the switch states. For a falling V_{DD} event, the lock out threshold is set to assure proper logic and switch behavior up to the moment the switches are forced off and external inputs are suppressed.

To facilitate hot plug insertion and power up control the LATCH pin has an integrated weak pull up resistor to the V_{DD} power rail that will hold a non-driven LATCH pin at a logic high state. This enables board designers to use the CPC7594 with FPGAs and other devices that provide high impedance outputs during power up and configuration. The weak pull up allows a fan out of up to 32 when the system's LATCH control driver has a logic low minimum sink capability of 4mA.

2.2.2 Hot Plug and Power Up Circuit Design Considerations

There are six possible start up scenarios that can occur during power up. They are:

1. All inputs defined at power up & LATCH = 0
2. All inputs defined at power up & LATCH = 1
3. All inputs defined at power up & LATCH = Z
4. All inputs not defined at power up & LATCH = 0
5. All inputs not defined at power up & LATCH = 1
6. All inputs not defined at power up & LATCH = Z

Under all of the start up situations listed above the CPC7594 will hold all of it's switches in the all-off state during power up. When V_{DD} requirements have been satisfied the LCAS will complete it's start up procedure in one of three conditions.

For start up scenario 1 the CPC7594 will transition from the all off state to the state defined by the inputs when V_{DD} is valid.

For start up scenarios 2, 3, 5, and 6 the CPC7594 will power up in the all-off state and remain there until the LATCH pin is pulled low. This allows for an indefinite all off state for boards inserted into a powered system but are not configured for service or boards that need to wait for other devices to be configured first.

Start up scenario 4 will start up with all switches in the all-off state but upon the acceptance of a valid V_{DD} the LCAS will revert to one of the legitimate states listed in the truth tables and there after may randomly change states based on input pin leakage currents and loading. Because the LCAS state after power up can not be predicted with this start up condition it should never be utilized.

On designs that do not wish to individually control the LATCH pins of multi-port cards it is possible to bus many (or all) of the LATCH pins together to create a single board level input enable control.

2.3 Switch Logic

2.3.1 Start-up

The CPC7594 uses smart logic to monitor the V_{DD} supply. Any time the V_{DD} is below an internally set threshold, the smart logic places the control logic to the all-off state. An internal pullup at the LATCH pin locks the CPC7594 in the all-off state following start-up until the LATCH pin is pulled down to a logic low. Prior to the assertion of a logic low at the LATCH pin, the switch control inputs must be properly conditioned.

2.3.2 Switch Timing

The CPC7594 provides, when switching from the ringing state to the talk state, the ability to control the release timing of the ringing switches SW3 and SW4 relative to the state of the switches SW1 and SW2 using simple TTL logic-level inputs. The two available techniques are referred to as make-before-break and break-before-make operation. When the break switch contacts of SW1 and SW2 are closed (made) before the ringing switch contacts of SW3 and SW4 are opened (broken), this is referred to as make-before-break operation. Break-before-make operation occurs when the ringing contacts of SW3 and SW4 are opened (broken) before the switch contacts of SW1 and SW2 are closed (made). With the CPC7594, make-before-break and break-before-make operations can easily be accomplished by applying the proper sequence of logic-level inputs to the device.

The logic sequences for either mode of operation are provided in "Make-Before-Break Ringing to Talk Transition Logic Sequence" on page 14, "Break-Before-Make Ringing to Talk Transition Logic Sequence" on page 14, and "Alternate Break-Before-Make Ringing to Talk Transition Logic Sequence" on page 15. Logic states and input control settings are provided in "CPC7594xA and CPC7594xB Truth Table" on page 11 and "CPC7594xC Truth Table" on page 11.

2.3.3 Make-Before-Break Operation

To use make-before-break operation, change the logic inputs from the ringing state directly to the talk state. Application of the talk state opens the ringing return switch, SW3, as the break switches SW1 and SW2 close. The ringing switch, SW4, remains closed until the next zero-crossing of the ringing current. While in the make-before-break state, ringing potentials in excess of the CPC7594 protection circuitry thresholds will be diverted away from the SLIC.

Make-Before-Break Ringing to Talk Transition Logic Sequence

State	$IN_{RINGING}$	IN_{TEST}	LATCH	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)	Test Switches
Ringing	1	0	0	Z	-	Off	On	On	Off
Make-before-break	0	0			SW4 waiting for next zero-current crossing to turn off. Maximum time is one-half of the ringing cycle. In this transition state current limited by the dc break switch current limit value will be sourced from the ring node of the SLIC.	On	Off	On	Off
Talk	0	0			Zero-cross current has occurred	On	Off	Off	Off

2.3.4 Break-Before-Make Operation

Break-before-make operation of the CPC7594 can be achieved using two different techniques.

The first method uses manipulation of the $IN_{RINGING}$ and IN_{TEST} logic inputs as shown in "Break-Before-Make Ringing to Talk Transition Logic Sequence" on page 14.

1. At the end of the ringing state apply the all off state (1,1). This releases the ringing return switch (SW3) while the ringing switch (SW4) remains on, waiting for the next zero current event.
2. Hold the all off state for at least one-half of a ringing cycle to assure that a zero crossing event occurs and that SW4, the ringing switch, has opened.
3. Apply inputs for the next desired state. For the talk state, the inputs would be (0,0).

Break-before-make operation occurs when the ringing switches open before the break switches SW1 and SW2 close.

Break-Before-Make Ringing to Talk Transition Logic Sequence

State	$IN_{RINGING}$	IN_{TEST}	LATCH	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)	Test Switches
Ringing	1	0	0	Z	-	Off	On	On	Off
All-Off	1	1			Hold this state for at least one-half of the ringing cycle. SW4 waiting for zero current to turn off.	Off	Off	On	Off
Break-Before-Make	1	1			Zero current has occurred. SW4 has opened	Off	Off	Off	Off
Talk	0	0			Break switches close.	On	Off	Off	Off

2.3.5 Alternate Break-Before-Make Operation

The alternate break-before-make technique is available for all versions of the CPC7594. As shown in "CPC7594xA and CPC7594xB Truth Table" on page 11 and "CPC7594xC Truth Table" on page 11, the bi-directional T_{SD} interface disables all of the switches when pulled to a logic low. Although logically disabled, an active ringing switch (SW4) will remain closed until the next zero crossing current event.

As shown in the table "Alternate Break-Before-Make Ringing to Talk Transition Logic Sequence" on page 15, this operation is similar to the one shown in "Alternate Break-Before-Make Operation" on page 14, except in the method used to select the all off state, and in when the $IN_{RINGING}$ and IN_{TEST} inputs are reconfigured for the talk state.

1. Pull T_{SD} to a logic low to end the ringing state. This opens the ringing return switch (SW3) and prevents any other switches from closing.
2. Keep T_{SD} low for at least one-half the duration of the ringing cycle period to allow sufficient time for a zero crossing current event to occur and for the circuit to enter the break-before-make state.
3. During the T_{SD} low period, set the $IN_{RINGING}$ and IN_{TEST} inputs to the talk state (0, 0).
4. Release T_{SD}, allowing the internal pull-up to activate the break switches.

When using T_{SD} as an input, the two recommended states are “0” which overrides the logic input pins and forces an all off state and “Z” which allows normal switch control via the logic input pins. This requires the use of an open-collector or open-drain type buffer.

Forcing T_{SD} to a logic high prevents the user from detecting a thermal shutdown condition and is therefore not recommended.

Alternate Break-Before-Make Ringing to Talk Transition Logic Sequence

State	$IN_{RINGING}$	IN_{TEST}	LATCH	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)	Test Switches
Ringing	1	0	0	Z	-	Off	On	On	Off
All-Off	1	0	X	0	Hold this state for at least one-half of the ringing cycle. SW4 waiting for zero current to turn off.	Off	Off	On	Off
Break-Before-Make	0	0			SW4 has opened	Off	Off	Off	Off
Talk	0	0	0	Z	Close Break Switches	On	Off	Off	Off

2.4 Data Latch

The CPC7594 has an integrated transparent data latch. The latch enable operation is controlled by TTL logic input levels at the LATCH pin. Data input to the latch is via the input pins $IN_{RINGING}$ and IN_{TEST} while the output of the data latch are internal nodes used for state control. When the LATCH enable control pin is at a logic 0 the data latch is transparent and the input control signals flow directly through the data latch to the state control circuitry. A change in input will be reflected by a change in the switch state.

Whenever the LATCH enable control pin is at logic 1, the data latch is active and data is locked. Subsequent changes to the input controls $IN_{RINGING}$ and IN_{TEST} will not result in a change to the control logic or affect the existing switch state.

The switches will remain in the state they were in when the LATCH changes from logic 0 to logic 1 and will not respond to changes in input as long as the LATCH is at logic 1. However, neither the T_{SD} input nor the T_{SD} output control functions are affected by the latch function. Since internal thermal shutdown control and external “All-off” control is not affected by the state of the LATCH enable input, T_{SD} will override state control.

2.5 T_{SD} Pin Description

The T_{SD} pin is a bi-directional I/O structure with an internal pull-up current source having a nominal value of 16 µA biased from V_{DD}.

As an output, this pin indicates the status of the thermal shutdown circuitry. Typically, during normal operation, this pin will be pulled up to V_{DD} but under fault conditions that create excess thermal loading the CPC7594 will enter thermal shutdown and a logic low will be output.

As an input, the T_{SD} pin is utilized to place the CPC7594 into the "All-Off" state by simply pulling the input to a logic low. For applications using low-voltage logic devices (lower than V_{DD}), Clare recommends the use of an open-collector or an open-drain type output to control T_{SD}. This avoids sinking the T_{SD} pull up bias current to ground during normal operation when the all-off state is not required. In general, Clare recommends all applications use an open-collector or open-drain type device to drive this pin.

Unlike the CPC7584, driving T_{SD} to a logic 1 or tying this pin to V_{CC} will not prevent normal operation of the thermal shutdown circuitry inside the CPC7594. As a result the T_{SD} pin may be held at a logic high. However, the CPC7594 T_{SD} pin has only two recommended operating states when it is used as an input control. A logic 0, which forces the device to the all-off state and a high impedance (Z) state for normal operation. This requires the use of an open-collector or open-drain type buffer.

2.6 Ringing Switch Zero-Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ringing switch is designed to delay the change in state until the next zero-crossing. Once on, the switch requires a zero-current cross to turn off, and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter the logic input until the next zero crossing. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing switches. See Clare's application note AN-144, **Impulse Noise Benefits of Line Card Access Switches** for more information. The attributes of ringing switch SW4 may make it possible to eliminate the need for a zero-cross switching scheme. A minimum impedance of 300 Ω in series with the ringing generator is recommended.

2.7 Power Supplies

Both a +5 V supply and battery voltage are connected to the CPC7594. Switch state control is powered exclusively by the +5 V supply. As a result, the CPC7594 exhibits extremely low power consumption during active and idle states.

Although battery power is not used for switch control, it is required to supply trigger current for the integrated internal protection circuitry SCR during fault conditions. This integrated SCR is designed to activate whenever the voltage at T_{BAT} or R_{BAT} drops 2 to 4 V below the applied voltage on the V_{BAT} pin. Because the battery supply at this pin is required to source trigger current during negative overvoltage fault conditions at tip and ring, it is important that the net supplying this current be a low impedance path for high speed transients such as lightning. This will permit trigger currents to flow enabling the SCR to activate and thereby prevent a fault induced negative overvoltage event at the T_{BAT} or R_{BAT} nodes.

2.8 Battery Voltage Monitor

The CPC7594 also uses the V_{BAT} voltage to monitor battery voltage. If system battery voltage is lost, the CPC7594 immediately enters the all-off state. It remains in this state until the battery voltage is restored. The device also enters the all-off state if the battery voltage rises more positive than about –10 V with respect to ground and remains in the all-off state until the battery voltage drops below approximately –15 V with respect to ground. This battery monitor feature draws a small current from the battery (less than 1 μA typical) and will add slightly to the device's overall power dissipation.

This monitor function performs properly if the CPC7594 and SLIC share a common battery supply origin. Otherwise, if battery is lost to the CPC7594 but not to the SLIC, then the V_{BAT} pin will be internally biased by the potential applied at the T_{BAT} or R_{BAT} pins via the internal protection circuitry SCR trigger current path.

2.9 Protection

2.9.1 Diode Bridge/SCR

The CPC7594 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge to ground via F_{GND}. Voltage is clamped to a diode drop above ground. During a negative transient of 2 to 4 V more negative than the voltage source at V_{BAT}, the SCR conducts and faults are shunted to F_{GND} via the SCR or the diode bridge.

In order for the SCR to crowbar (or foldback), the SCR's on-voltage (see "Protection Circuitry Electrical Specifications" on page 10) must be less than the applied voltage at the V_{BAT} pin. If the V_{BAT} voltage is less negative than the SCR on-voltage or if the V_{BAT} supply is unable to source the trigger current, the SCR will not crowbar.

For power induction or power-cross fault conditions, the positive cycle of the transient is clamped to a diode drop above ground and the fault current directed to ground. The negative cycle of the transient will cause the SCR to conduct when the voltage exceeds the V_{BAT} reference voltage by two to four volts, steering the fault current to ground.

Note: The CPC7594xB does not contain the protection SCR but instead uses diodes to clamp both polarities of a transient fault. These diodes direct the negative potential's fault current to the V_{BAT} pin.

2.9.2 Current Limiting function

If a lightning strike transient occurs when the device is in the talk state, the current is passed along the line to the integrated protection circuitry and restricted by the dynamic current limit response of the active switches. During the talk state, when a 1000V 10x1000 µs lightning pulse (GR-1089-CORE) is applied to the line though a properly clamped external protector, the current seen at T_{LINE} and R_{LINE} will be a pulse with a typical magnitude of 2.5 A and a duration less than 0.5 µs.

If a power-cross fault occurs with the device in the talk state, the current is passed though break switches SW1 and SW2 on to the integrated protection circuit but is limited by the dynamic DC current limit response of the two break switches. The DC current limit specified over temperature is between 80 mA and 425 mA and the circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to a power cross fault condition, the measured current at T_{LINE} and R_{LINE} will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will enter the all-off state.

2.10 Thermal Shutdown

The thermal shutdown mechanism activates when the device die temperature reaches a minimum of 110° C, placing the device in the all-off state regardless of logic input. During thermal shutdown events the T_{SD} pin will output a logic low with a nominal 0 V level. A logic high is output from the T_{SD} pin during normal operation with a typical output level equal to V_{DD}.

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross event, the device temperature will rise and the thermal shutdown mechanism will activate forcing the switches to the all-off state. At this point the current measured into T_{LINE} or R_{LINE} will drop to zero. Once the device enters thermal shutdown it will remain in the all-off state until the temperature of the device drops below the de-activation level of the thermal shutdown circuit. This permits the device to autonomously return to normal operation. If the transient has not passed, current will again flow up to the value allowed by the dynamic DC current limiting of the switches and heating will resume, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector will activate shunting the fault current to ground.

2.11 External Protection Elements

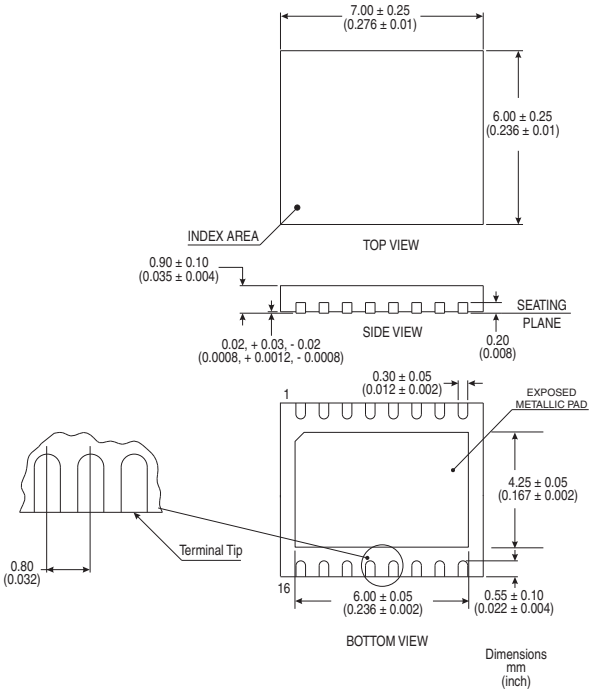
The CPC7594 requires only over voltage secondary protection on the loop side of the device. The integrated protection feature described above negates the need for additional external protection on the SLIC side. The secondary protector must limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7594. A foldback or crowbar type protector is recommended to minimize stresses on the CPC7594.

Consult Clare's application note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces" for equations related to the specifications of external secondary protectors, fused resistors and PTCs.

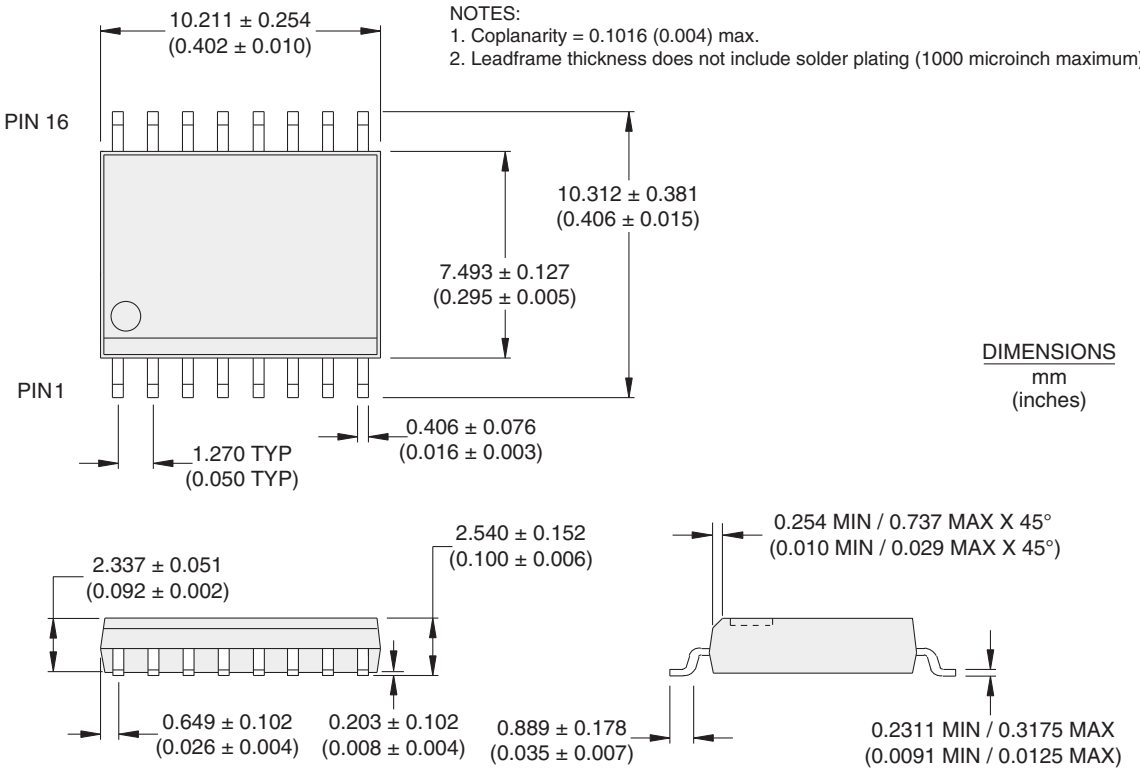
3. Manufacturing Information

3.1 Mechanical Dimensions

3.1.1 DFN

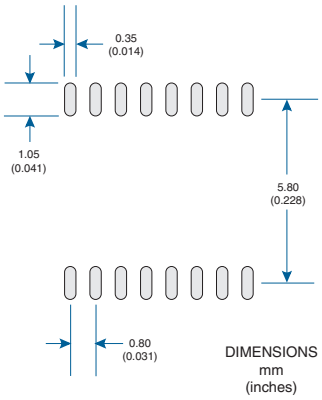


3.1.2 SOIC



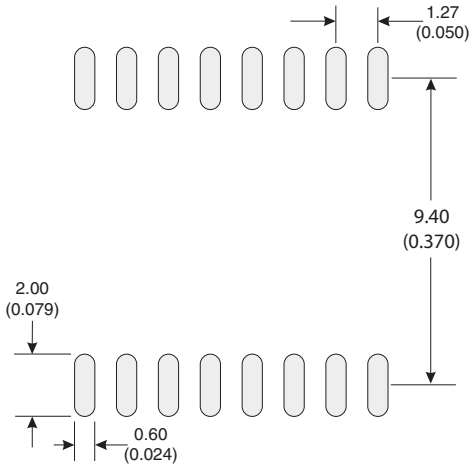
3.2 Printed-Circuit Board Layout

3.2.1 DFN



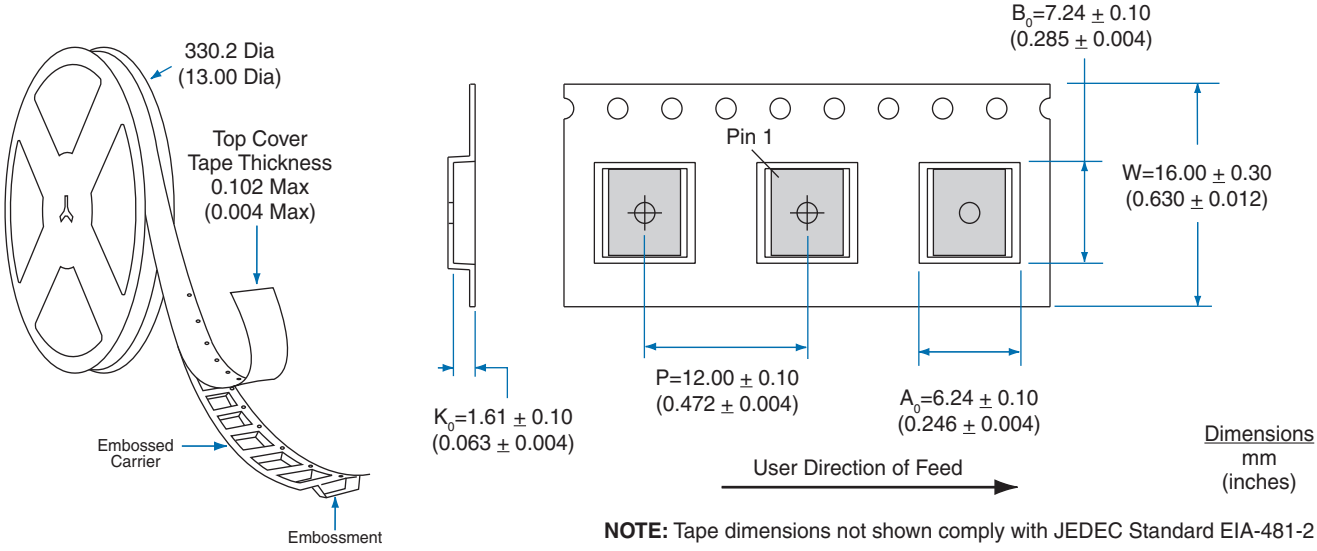
NOTE: As the metallic pad on the bottom of the DFN package is connected to the substrate of the die, Clare recommends that no printed circuit board traces or vias be placed under this area to maintain minimum creepage and clearance values.

3.2.2 SOIC



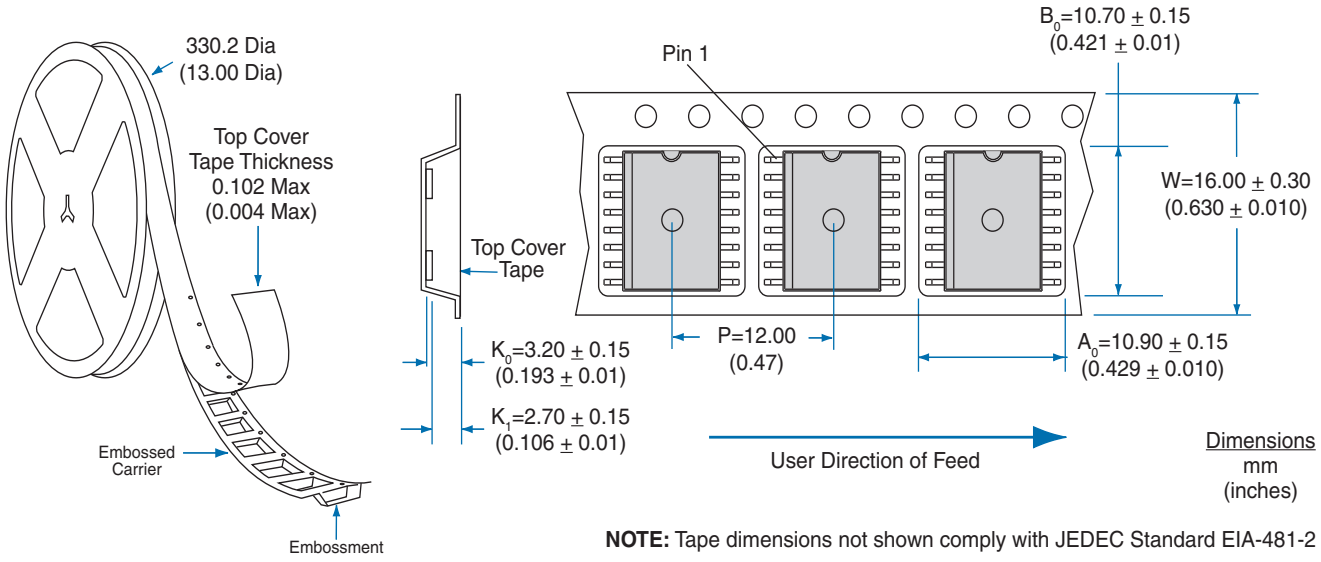
3.3 Tape and Reel Packaging

3.3.1 DFN



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

3.3.2 SOIC



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

3.4 Soldering

3.4.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity for this product using IPC/JEDEC standard J-STD-020. Moisture uptake from atmospheric humidity occurs by diffusion. During the solder reflow process, in which the component is attached to the PCB, the whole body of the component is exposed to high process temperatures. The combination of moisture uptake and high reflow soldering temperatures may lead to moisture induced delamination and cracking of the component. To prevent this, this component must be handled in accordance with IPC/JEDEC standard J-STD-033 per the labeled moisture sensitivity level (MSL), level 1 for the SOIC package, and level 3 for the DFN package.

3.4.2 Reflow Profile

For proper assembly, this component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

3.5 Washing

Clare does not recommend ultrasonic cleaning of this part.

For additional information please visit www.clare.com

Specifications: DS-CPC7594 - R03

10/14/09