AOT500
N-Channel Enhancement Mode Field Effect Transistor

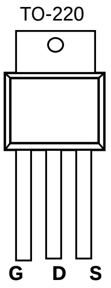
General Description

AOT500 uses an optimally designed temperature compensated gate-drain zener clamp. Under overvoltage conditions, the clamp activates and turns on the MOSFET, safely dissipating the energy in the MOSFET. The built in resistor guarantees proper clamp operation under all circuit conditions, and the MOSFET never goes into avalanche breakdown. Advanced trench technology provides excellent low Rdson, gate charge and body diode characteristics, making this device ideal for motor and inductive load control applications.

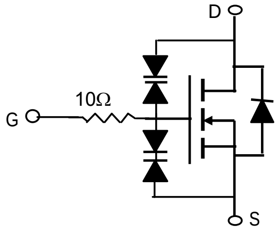
Standard Product AOT500 is Pb-free (meets ROHS & Sony 259 specifications).

Features

V_{DS} (V) = Clamped
I_D = 80A (V_{GS} = 10V)
$R_{DS(ON)}$ < 5.3 mΩ (V_{GS} = 10V)



Top View
Drain
Connected to
Tab



Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	clamped	V
Gate-Source Voltage		V_{GS}	clamped	V
Continuous Drain Current [G]	T_C=25°C	I_D	80	A
	T_C=100°C		57	
Continuous Drain Gate Current		I_{DG}	±50	mA
Continuouse Gate Source Current		I_{GS}	±50	
Pulsed Drain Current [C]		I_{DM}	250	A
Avalanche Current L=100uH[H]		I_{AR}	50	A
Repetitive avalanche energy [H]		E_{AR}	125	mJ
Power Dissipation [B]	T_C=25°C	P_D	115	W
	T_C=100°C		58	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	Steady-State	$R_{\theta JA}$	60	75	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	0.7	1.3	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
$BV_{DSS(z)}$	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	33			V
BV_{CLAMP}	Drain-Source Clamping Voltage	I_D=1A, V_{GS}=0V	36		44	V
$I_{DSS(z)}$	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0V			30	µA
BV_{GSS}	Gate-Source Voltage	V_{DS}=0V, I_D=250µA	20			V
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±10V			10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	1.5	2	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	250			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=30A		4.1	5.3	mΩ
		T_J=125°C		6.2		
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=30A		95		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				80	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		4735	6150	pF
C_{oss}	Output Capacitance			765		pF
C_{rss}	Reverse Transfer Capacitance			340		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		13	17	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=30A		69	89	nC
Q_g(4.5V)	Total Gate Charge			34		nC
Q_{gs}	Gate Source Charge			12		nC
Q_{gd}	Gate Drain Charge			15		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.5Ω, R_{GEN}=3Ω		25		ns
t_r	Turn-On Rise Time			35		ns
$t_{D(off)}$	Turn-Off DelayTime			150		ns
t_f	Turn-Off Fall Time			62		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=30A, dI/dt=100A/µs		60	78	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=30A, dI/dt=100A/µs		84		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25°C.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. E_{AR} and I_{AR} are based on a 100uH inductor with Tj(start) = 25C for each pulse.

Rev 0_prelim: December 2007

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

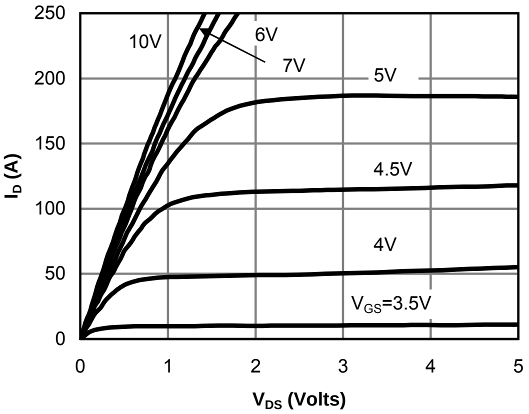


Fig 1: On-Region Characteristics

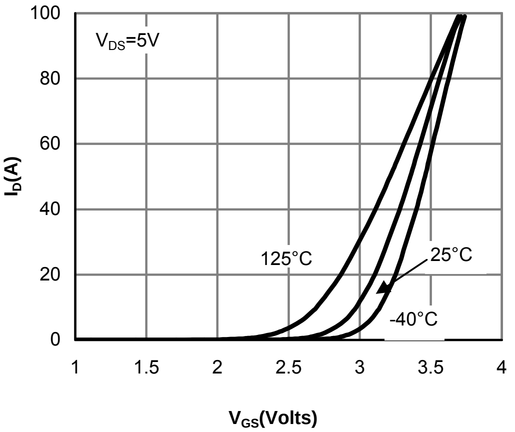


Figure 2: Transfer Characteristics

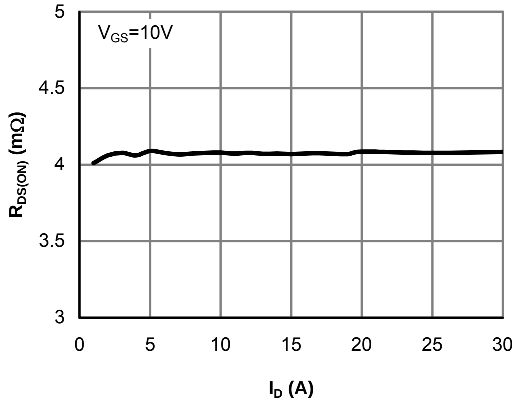


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

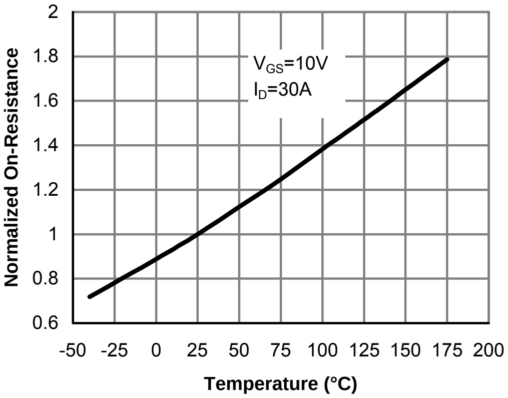


Figure 4: On-Resistance vs. Junction Temperature

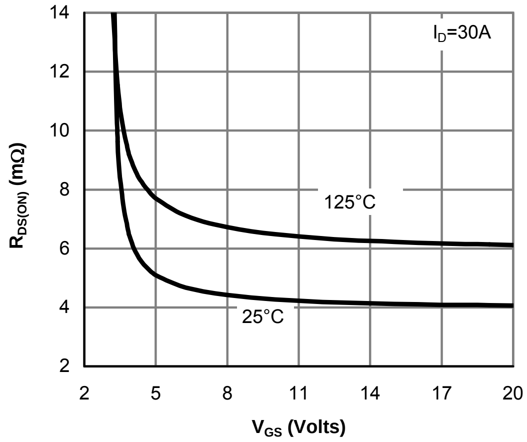


Figure 5: On-Resistance vs. Gate-Source Voltage

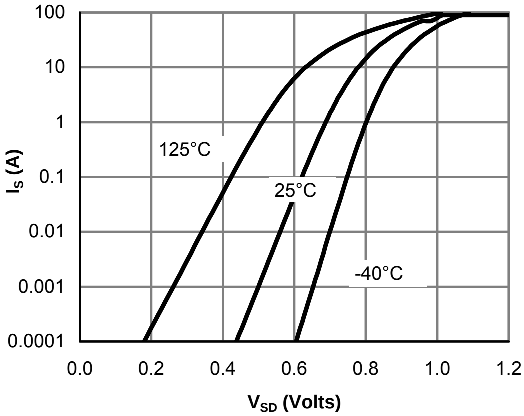


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

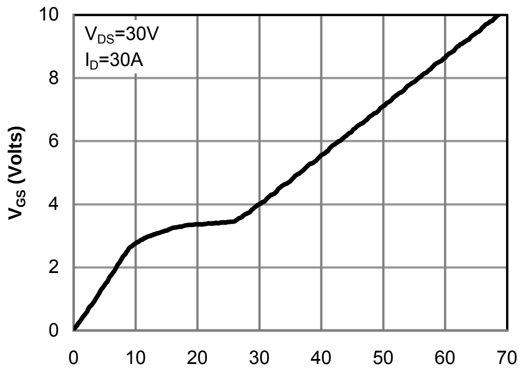


Figure 7: Gate-Charge Characteristics

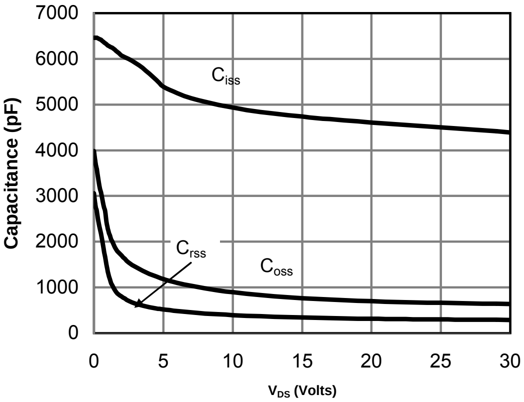


Figure 8: Capacitance Characteristics

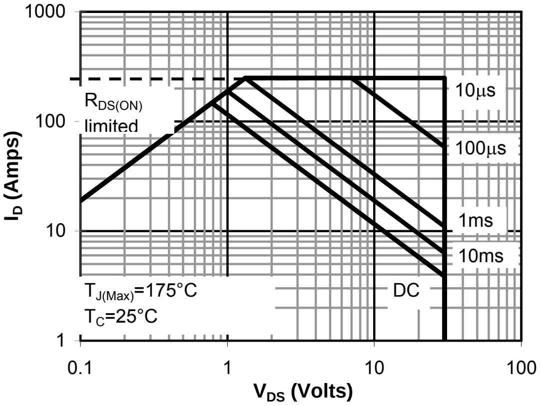


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

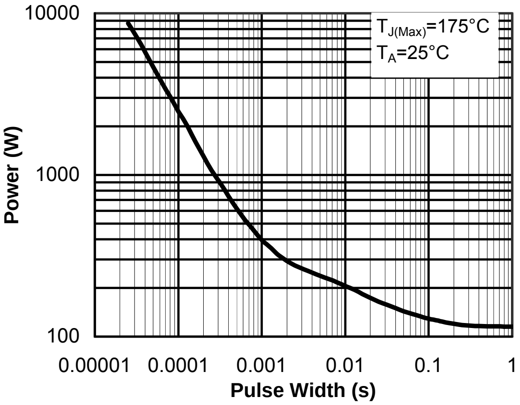


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

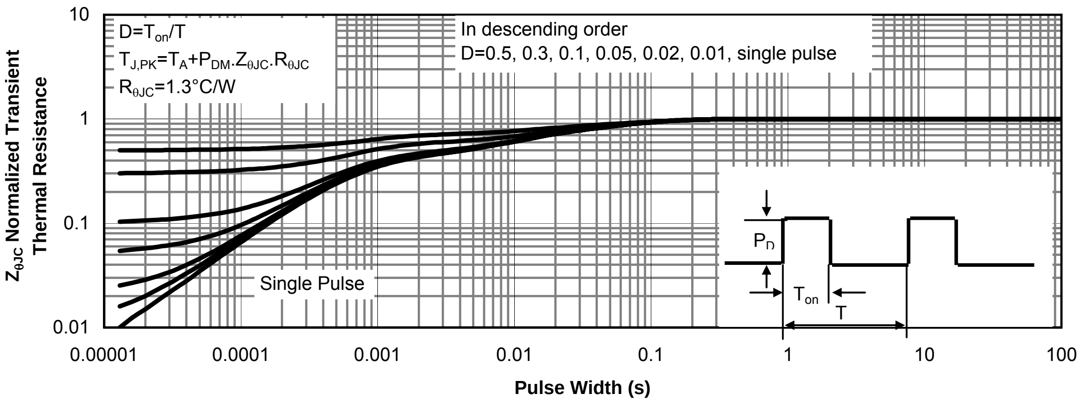


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

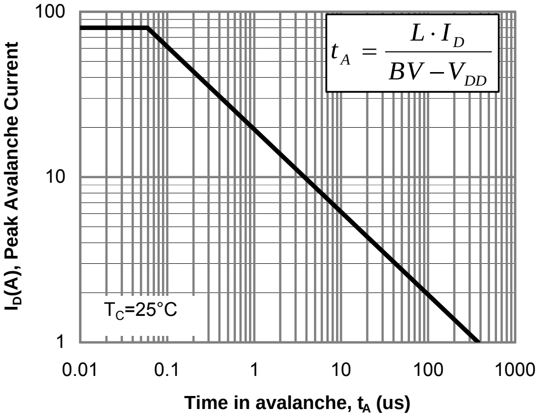


Figure 12: Single Pulse Avalanche capability

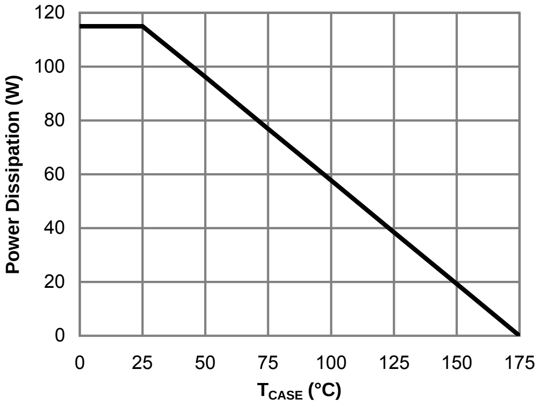


Figure 13: Power De-rating (Note B)

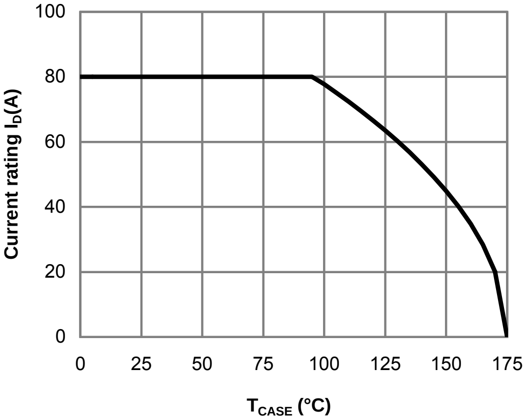


Figure 14: Current De-rating (Note B)

TYPICAL PROTECTION CHARACTERISTICS

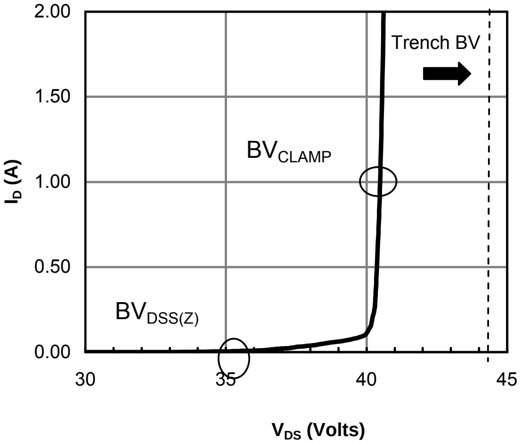


Fig 15: BV_{CLAMP} Characteristic

This device uses built-in Gate to Source and Gate to Drain zener protection. While the Gate-Source zener protects against excessive V_{GS} conditions, the Gate to Drain protection, clamps the VDS well below the device breakdown, preventing an avalanche condition within the MOSFET as a result of voltage over-shoot at the Drain electrode.

It is designed to breakdown well before the device breakdown. During such an event, current flows through the zener clamp, which is situated internally between the Gate to Drain. This current flows at $BV_{DSS(Z)}$, building up the V_{GS} internal to the device. When the current level through the zener reaches approximately 300mA, the V_{GS} is approximately equal to $V_{GS(PLATEAU)}$, allowing significant channel conduction and thus clamping the Drain to Source voltage. The V_{GS} needed to turn the device on is controlled with an internally lumped gate resistor R approximately equal to 10Ω.

$V_{GS(PLATEAU)}$= 10Ω x 300mA =3V

It can also be said that the VDS during clamping is equal to:

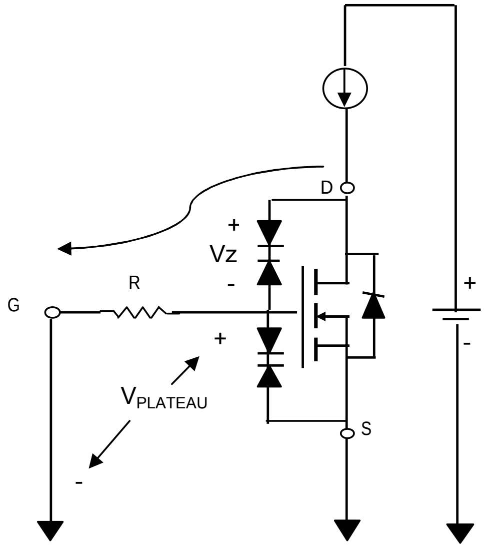
$BV_{DSS} = BV_{CLAMP} + V_{GS(PLATEAU)}$

Additional power loss associated with the protection circuitry can be considered negligible when compare to the conduction losses of the MOSFET itself;

EX:

PL=30μAmax x 16V=0.48mW (Zener leakage loss)

PL(rds)=102A x 6mΩ=300mW (MOSFET loss)



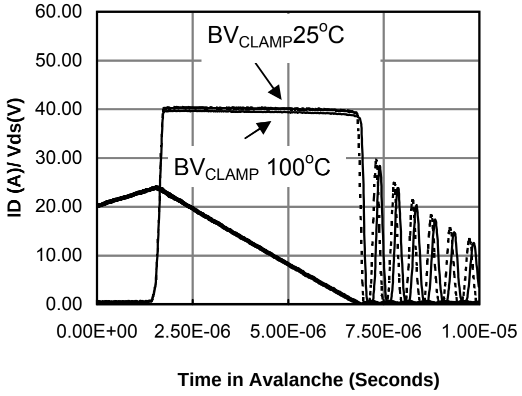


Fig 16: Unclamped Inductive Switching

Fig16: The built-in Gate to Drain clamp prevents the device from going into Avalanche by setting the clamp voltage well below the actual breakdown of the device. When the Drain to Gate voltage approaches the BV clamp, the internal Gate to Source voltage is charged up and channel conduction occurs, sinking the current safely through the device. The BV_{CLAMP} is virtually temperature independent, providing even greater protection during normal operation.