## DESCRIPTION

The M35043-XXXSP/FP is a TV screen display control IC. It uses a silicon gate CMOS process and is housed in a 20-pin shrink DIP package (M35043-XXXSP) or a 20-pin shrink SOP package (M35043-XXXFP).
For M35043-001SP/FP that is a standard ROM version of M35043-XXXSP/FP respectively, the character pattern is also mentioned.
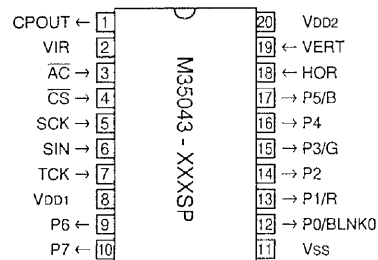
## FEATURES

- Screen composition .................................... 24 columns × 12 lines
- Number of characters displayed ................................... 288 (Max.)
- Character composition ..................................... 12 × 18 dot matrix
- Characters available ............................................ 128 characters
- Character sizes available ..................... 4 (horizontal) × 4 (vertical)
- Display locations available
    Horizontal direction............................................ 1000 locations
    Vertical direction ............................................... 1023 locations
- Blinking................................................................. Character units
    Cycle   : division of vertical synchronization signal into 64 or 32
    Duty    : 25%, 50%, or 75%
- Data input ................................... By the 16-bit serial input function
- Coloring
    Character color ..................................................... Character unit
    Background coloring........................................... Character unit
    Matrix-outline (shadow) coloring .............. 8 colors (RGB output)
                                                Specified by register
    Border coloring ........................................ 8 colors (RGB output)
                                                Specified by register
    Raster coloring ........................................ 8 colors (RGB output)
                                                Specified by register
- Blanking                                                      Blanking off
                                                Character size blanking
                                                Border size blanking
                                                Matrix-outline blanking
                                                All blanking (all raster area)
- Output ports
    4 shared output ports (toggled between RGB output)
    4 dedicated output ports
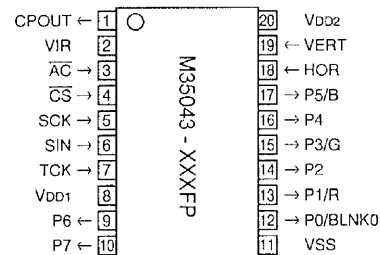- Display RAM erase function
- Display input frequency range ................... Fosc = 30MHz-60MHz

## APPLICATION

Monitor

## PIN CONFIGURATION (TOP VIEW)

```
CPOUT ← | 1|            |20|  VDD2
  VIR   | 2|            |19| ← VERT
   AC → | 3|  M         |18| ← HOR
   CS → | 4|  3         |17| → P5/B
  SCK → | 5|  5         |16| → P4
  SIN → | 6|  0         |15| → P3/G
  TCK → | 7|  4         |14| → P2
  VDD1  | 8|  3         |13| → P1/R
   P6 ← | 9|  -         |12| → P0/BLNK0
   P7 ← |10| XXXSP      |11|  VSS
```

**Outline 20P4B**

```
CPOUT ← | 1| O          |20|  VDD2
  VIR   | 2|            |19| ← VERT
   AC → | 3|  M         |18| ← HOR
   CS → | 4|  3         |17| → P5/B
  SCK → | 5|  5         |16| → P4
  SIN → | 6|  0         |15| → P3/G
  TCK → | 7|  4         |14| → P2
  VDD1  | 8|  3         |13| → P1/R
   P6 ← | 9|  -         |12| → P0/BLNK0
   P7 ← |10| XXXFP      |11|  VSS
```
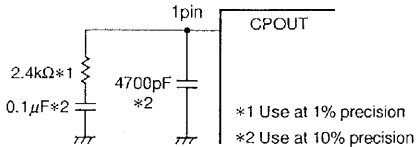
**Outline 20P2Q-A**

## PIN DESCRIPTION

| Pin Number | Symbol | Pin name | Input/Output | Function |
|---|---|---|---|---|
| 1 | CPOUT | Phase difference | Output | Connect loop filter to this pin.<br><br>2.4kΩ*1  4700pF *2  0.1μF*2<br>1pin CPOUT<br>*1 Use at 1% precision<br>*2 Use at 10% precision |
| 2 | VIR | Frequency control | – | Connect to GND. |
| 3 | $\overline{AC}$ | Auto-clear input | Input | When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor. |
| 4 | $\overline{CS}$ | Chip select input | Input | This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor. |
| 5 | SCK | Serial clock input | Input | When $\overline{CS}$ pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included. |
| 6 | SIN | Serial data input | Input | This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Includes built-in pull-up resistor. |
| 7 | TCK | Test clock | Input | Input for test. Please connect to GND using circuit earthing pin. |
| 8 | $V_{DD1}$ | Power pin | – | Please connect to +5V with the power pin. |
| 9 | P6 | Port P6 output | Output | This is the output port. Port data is set by PTD6. |
| 10 | P7 | Port P7 output | Output | This is the output port. Port data is set by PTD7. |
| 11 | $V_{SS}$ | Earthing pin | – | Please connect to GND using circuit earthing pin. |
| 12 | P0/BLNK0 | Port P0 output | Output | This pin can be toggled between port pin output and BLNK0 signal output. |
| 13 | P1/R | Port P1 output | Output | This pin can be toggled between port pin output and R signal output. |
| 14 | P2 | Port P2 output | Output | This is the output port. Port data is set by PTD2. |
| 15 | P3/G | Port P3 output | Output | This pin can be toggled between port pin output and G signal output. |
| 16 | P4 | Port P4 output | Output | This is the output port. Port data is set by PTD4. |
| 17 | P5/B | Port P5 output | Output | This pin can be toggled between port pin output and B signal output. |
| 18 | HOR | Horizontal synchronization signal input | Input | This pin inputs the horizontal synchronization signal. Hysteresis input. |
| 19 | VERT | Vertical synchronization signal input | Input | This pin inputs the vertical synchronization signal. Hysteresis input. |
| 20 | $V_{DD2}$ | Power pin | – | Please connect to +5V with the power pin. |
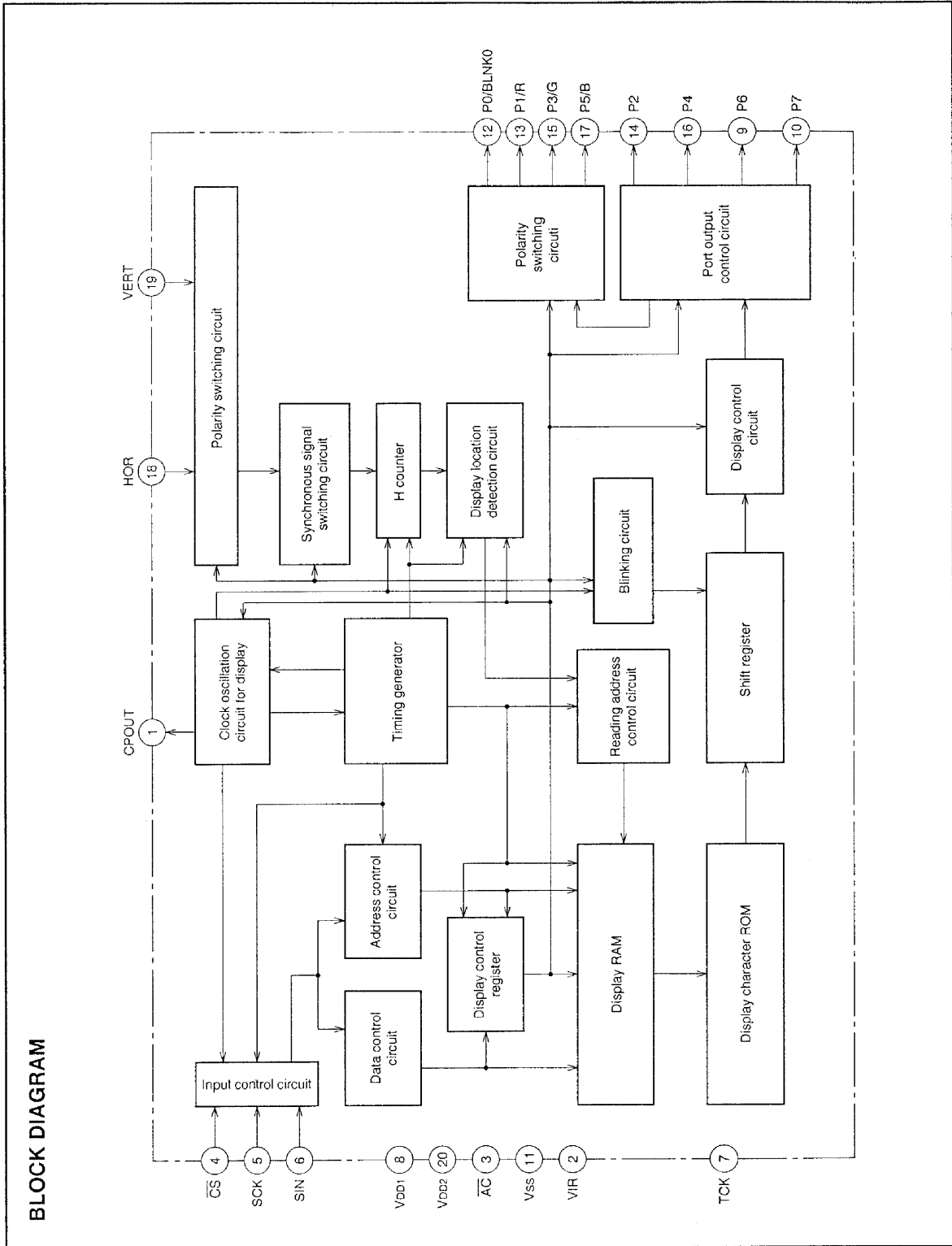
## BLOCK DIAGRAM

PO/BLNK0 (12)
P1/R (13)
P3/G (15)
P5/B (17)
P2 (14)
P4 (16)
P6 (9)
P7 (10)

VERT (19)
HOR (18)
CPOUT (1)

Polarity switching circuit

Polarity switching circuti

Port output control circuit

Synchronous signal switching circuit

H counter

Display location detection circuit

Display control circuit

Blinking circuit

Clock oscillation circuit for display

Timing generator

Reading address control circuit

Shift register

Address control circuit

Display control register

Display RAM

Display character ROM

Input control circuit

Data control circuit

CS (4)
SCK (5)
SIN (6)
VDD1 (8)
VDD2 (20)
AC (3)
VSS (11)
VIR (2)
TCK (7)

## MEMORY CONSTITUTION

Address $000_{16}$ to $11F_{16}$ are assigned to the display RAM, address $120_{16}$ to $128_{16}$ are assigned to the display control registers. The internal circuit is reset and all display control registers (address $120_{16}$ to $128_{16}$) are set to "0" and display RAM (address $000_{16}$ to $11F_{16}$) are set to "$FF_{16}$" when the AC pin level is "L".
Memory constitution is shown in Figure 1.

## SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 2.

| | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $000_{16}$ | 0 | BB | BG | BR | BLINK | B | G | R | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| ⋮ | ⋮ | | Background coloring | | Blinking | Character color | | | ⋮ | Character code | | | | | | |
| $11F_{16}$ | 0 | BB | BG | BR | BLINK | B | G | R | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| $120_{16}$ | 0 | 0 | DIVS2 | DIVS1 | DIVS0 | DIV10 | DIV9 | DIV8 | DIV7 | DIV6 | DIV5 | DIV4 | DIV3 | DIV2 | DIV1 | DIV0 |
| $121_{16}$ | 0 | 0 | PTD7 | PTD6 | PTD5 | PTD4 | PTD3 | PTD2 | PTD1 | PTD0 | PTC5 | PTC4 | PTC3 | PTC2 | PTC1 | PTC0 |
| $122_{16}$ | 0 | 0 | SPACE2 | SPACE1 | SPACE0 | TEST9 | HP9 | HP8 | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 |
| $123_{16}$ | 0 | 0 | TEST3 | TEST2 | TEST1 | TEST0 | VP9 | VP8 | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 |
| $124_{16}$ | 0 | 0 | TEST5 | TEST4 | DSP11 | DSP10 | DSP9 | DSP8 | DSP7 | DSP6 | DSP5 | DSP4 | DSP3 | DSP2 | DSP1 | DSP0 |
| $125_{16}$ | 0 | 0 | VSZ1H1 | VSZ1H0 | VSZ1L1 | VSZ1L0 | V1SZ1 | V1SZ0 | LIN9 | LIN8 | LIN7 | LIN6 | LIN5 | LIN4 | LIN3 | LIN2 |
| $126_{16}$ | 0 | 0 | VSZ2H1 | VSZ2H0 | VSZ2L1 | VSZ2L0 | V18SZ1 | V18SZ0 | LIN17 | LIN16 | LIN15 | LIN14 | LIN13 | LIN12 | LIN11 | LIN10 |
| $127_{16}$ | 0 | 0 | HSZ21 | HSZ20 | HSZ11 | HSZ10 | BETA14 | TEST8 | TEST7 | TEST6 | FB | FG | FR | RB | RG | RR |
| $128_{16}$ | 0 | 0 | BLINK2 | BLINK1 | BLINK0 | DSPON | STOP | RAMERS | SYAD | BLK1 | BLK0 | POLH | POLV | VMASK | B/F̄ | BCOL |

Fig. 1 Memory constitution

| Row / Line | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $000_{16}$ | $001_{16}$ | $002_{16}$ | $003_{16}$ | $004_{16}$ | $005_{16}$ | $006_{16}$ | $007_{16}$ | $008_{16}$ | $009_{16}$ | $00A_{16}$ | $00B_{16}$ | $00C_{16}$ | $00D_{16}$ | $00E_{16}$ | $00F_{16}$ | $010_{16}$ | $011_{16}$ | $012_{16}$ | $013_{16}$ | $014_{16}$ | $015_{16}$ | $016_{16}$ | $017_{16}$ |
| 2 | $018_{16}$ | $019_{16}$ | $01A_{16}$ | $01B_{16}$ | $01C_{16}$ | $01D_{16}$ | $01E_{16}$ | $01F_{16}$ | $020_{16}$ | $021_{16}$ | $022_{16}$ | $023_{16}$ | $024_{16}$ | $025_{16}$ | $026_{16}$ | $027_{16}$ | $028_{16}$ | $029_{16}$ | $02A_{16}$ | $02B_{16}$ | $02C_{16}$ | $02D_{16}$ | $02E_{16}$ | $02F_{16}$ |
| 3 | $030_{16}$ | $031_{16}$ | $032_{16}$ | $033_{16}$ | $034_{16}$ | $035_{16}$ | $036_{16}$ | $037_{16}$ | $038_{16}$ | $039_{16}$ | $03A_{16}$ | $03B_{16}$ | $03C_{16}$ | $03D_{16}$ | $03E_{16}$ | $03F_{16}$ | $040_{16}$ | $041_{16}$ | $042_{16}$ | $043_{16}$ | $044_{16}$ | $045_{16}$ | $046_{16}$ | $047_{16}$ |
| 4 | $048_{16}$ | $049_{16}$ | $04A_{16}$ | $04B_{16}$ | $04C_{16}$ | $04D_{16}$ | $04E_{16}$ | $04F_{16}$ | $050_{16}$ | $051_{16}$ | $052_{16}$ | $053_{16}$ | $054_{16}$ | $055_{16}$ | $056_{16}$ | $057_{16}$ | $058_{16}$ | $059_{16}$ | $05A_{16}$ | $05B_{16}$ | $05C_{16}$ | $05D_{16}$ | $05E_{16}$ | $05F_{16}$ |
| 5 | $060_{16}$ | $061_{16}$ | $062_{16}$ | $063_{16}$ | $064_{16}$ | $065_{16}$ | $066_{16}$ | $067_{16}$ | $068_{16}$ | $069_{16}$ | $06A_{16}$ | $06B_{16}$ | $06C_{16}$ | $06D_{16}$ | $06E_{16}$ | $06F_{16}$ | $070_{16}$ | $071_{16}$ | $072_{16}$ | $073_{16}$ | $074_{16}$ | $075_{16}$ | $076_{16}$ | $077_{16}$ |
| 6 | $078_{16}$ | $079_{16}$ | $07A_{16}$ | $07B_{16}$ | $07C_{16}$ | $07D_{16}$ | $07E_{16}$ | $07F_{16}$ | $080_{16}$ | $081_{16}$ | $082_{16}$ | $083_{16}$ | $084_{16}$ | $085_{16}$ | $086_{16}$ | $087_{16}$ | $088_{16}$ | $089_{16}$ | $08A_{16}$ | $08B_{16}$ | $08C_{16}$ | $08D_{16}$ | $08E_{16}$ | $08F_{16}$ |
| 7 | $090_{16}$ | $091_{16}$ | $092_{16}$ | $093_{16}$ | $094_{16}$ | $095_{16}$ | $096_{16}$ | $097_{16}$ | $098_{16}$ | $099_{16}$ | $09A_{16}$ | $09B_{16}$ | $09C_{16}$ | $09D_{16}$ | $09E_{16}$ | $09F_{16}$ | $0A0_{16}$ | $0A1_{16}$ | $0A2_{16}$ | $0A3_{16}$ | $0A4_{16}$ | $0A5_{16}$ | $0A6_{16}$ | $0A7_{16}$ |
| 8 | $0A8_{16}$ | $0A9_{16}$ | $0AA_{16}$ | $0AB_{16}$ | $0AC_{16}$ | $0AD_{16}$ | $0AE_{16}$ | $0AF_{16}$ | $0B0_{16}$ | $0B1_{16}$ | $0B2_{16}$ | $0B3_{16}$ | $0B4_{16}$ | $0B5_{16}$ | $0B6_{16}$ | $0B7_{16}$ | $0B8_{16}$ | $0B9_{16}$ | $0BA_{16}$ | $0BB_{16}$ | $0BC_{16}$ | $0BD_{16}$ | $0BE_{16}$ | $0BF_{16}$ |
| 9 | $0C0_{16}$ | $0C1_{16}$ | $0C2_{16}$ | $0C3_{16}$ | $0C4_{16}$ | $0C5_{16}$ | $0C6_{16}$ | $0C7_{16}$ | $0C8_{16}$ | $0C9_{16}$ | $0CA_{16}$ | $0CB_{16}$ | $0CC_{16}$ | $0CD_{16}$ | $0CE_{16}$ | $0CF_{16}$ | $0D0_{16}$ | $0D1_{16}$ | $0D2_{16}$ | $0D3_{16}$ | $0D4_{16}$ | $0D5_{16}$ | $0D6_{16}$ | $0D7_{16}$ |
| 10 | $0D8_{16}$ | $0D9_{16}$ | $0DA_{16}$ | $0DB_{16}$ | $0DC_{16}$ | $0DD_{16}$ | $0DE_{16}$ | $0DF_{16}$ | $0E0_{16}$ | $0E1_{16}$ | $0E2_{16}$ | $0E3_{16}$ | $0E4_{16}$ | $0E5_{16}$ | $0E6_{16}$ | $0E7_{16}$ | $0E8_{16}$ | $0E9_{16}$ | $0EA_{16}$ | $0EB_{16}$ | $0EC_{16}$ | $0ED_{16}$ | $0EE_{16}$ | $0EF_{16}$ |
| 11 | $0F0_{16}$ | $0F1_{16}$ | $0F2_{16}$ | $0F3_{16}$ | $0F4_{16}$ | $0F5_{16}$ | $0F6_{16}$ | $0F7_{16}$ | $0F8_{16}$ | $0F9_{16}$ | $0FA_{16}$ | $0FB_{16}$ | $0FC_{16}$ | $0FD_{16}$ | $0FE_{16}$ | $0FF_{16}$ | $100_{16}$ | $101_{16}$ | $102_{16}$ | $103_{16}$ | $104_{16}$ | $105_{16}$ | $106_{16}$ | $107_{16}$ |
| 12 | $108_{16}$ | $109_{16}$ | $10A_{16}$ | $10B_{16}$ | $10C_{16}$ | $10D_{16}$ | $10E_{16}$ | $10F_{16}$ | $110_{16}$ | $111_{16}$ | $112_{16}$ | $113_{16}$ | $114_{16}$ | $115_{16}$ | $116_{16}$ | $117_{16}$ | $118_{16}$ | $119_{16}$ | $11A_{16}$ | $11B_{16}$ | $11C_{16}$ | $11D_{16}$ | $11E_{16}$ | $11F_{16}$ |

※ The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution

## REGISTERS DESCRIPTION

(1) Address $120_{16}$

| DA | Register | Contents | | Remarks |
|----|----------|----------|------|---------|
| | | Status | Function | |
| 0 | DIV0 | ⓞ / 1 | Set multiply value (frequency value) of horizontal synchronous frequency.<br><br>$$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$$<br><br>N1: frequency value | Display frequency is computed as shown below.<br><br>$\underline{FOSC = fH \times N1}$<br><br>FOSC [MHz] : Display frequency<br>fH [kHz]   : Horizontal synchronous signal frequency to HOR pin.<br>N1   : Shown left<br><br>Set display frequency FOSC to within 30MHz to 60MHz range.<br>When display frequency FOSC, set frequency value N2 in association with DIVS0 and DIVS1. |
| 1 | DIV1 | ⓞ / 1 | | |
| 2 | DIV2 | ⓞ / 1 | | |
| 3 | DIV3 | ⓞ / 1 | | |
| 4 | DIV4 | ⓞ / 1 | | |
| 5 | DIV5 | ⓞ / 1 | | |
| 6 | DIV6 | ⓞ / 1 | | |
| 7 | DIV7 | ⓞ / 1 | | |
| 8 | DIV8 | ⓞ / 1 | | |
| 9 | DIV9 | ⓞ / 1 | | |
| A | DIV10 | ⓞ / 1 | | |
| B | DIVS0 | ⓞ / 1 | Set frequency value N2<br><br>| DIVS | | Frequency value N2 |<br>|---|---|---|<br>| 1 | 0 | |<br>| 0 | 0 | Division into 2 |<br>| 0 | 1 | Division into 3 |<br>| 1 | 0 | Division into 4 |<br>| 1 | 1 | Do not set | | Set frequency value N2 in association with display frequency range.<br><br>| Display frequency | Frequency value N2 |<br>|---|---|<br>| 55 ~ 60 | Division into 2 |<br>| 40 ~ 55 | Division into 3 |<br>| 30 ~ 40 | Division into 4 | |
| C | DIVS1 | ⓞ / 1 | | |
| D | DIVS2 | ⓞ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |

Note: The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(2) Address 121₁₆

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | PTC0 | ⓪ | P0 output (port P0). Port data is set by PTD0. | BLNK0 outputs blanking signal. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP11 settings. |
| | | 1 | BLNK0 output. Polarity is set by PTD0. | |
| 1 | PTC1 | ⓪ | P1 output (port P1). Port data is set by PTD1. | |
| | | 1 | R signal output. Polarity is set by PTD1. | |
| 2 | PTC2 | ⓪ | P2 output (port P2). Port data is set by PTD2. | |
| | | 1 | Do not set. | |
| 3 | PTC3 | ⓪ | P3 output (port P3). Port data is set by PTD3. | |
| | | 1 | G signal output. Polarity is set by PTD3. | |
| 4 | PTC4 | ⓪ | P4 output (port P4). Port data is set by PTD4. | |
| | | 1 | Do not set. | |
| 5 | PTC5 | ⓪ | P5 output (port P5). Port data is set by PTD5. | |
| | | 1 | B signal output. Polarity is set by PTD5. | |
| 6 | PTD0 | ⓪ | "L" output (P0 output) or negative polarity output (BLNK0 output). | P0 pin data control. |
| | | 1 | "H" output (P0 output) or positive polarity output (BLNK0 output). | |
| 7 | PTD1 | ⓪ | "L" output (P1 output) or negative polarity output (R signal output). | P1 pin data control. |
| | | 1 | "H" output (P1 output) or positive polarity output (R signal output). | |
| 8 | PTD2 | ⓪ | "L" output (P2 output). | P2 pin exclusive port output state control. |
| | | 1 | "H" output (P2 output). | |
| 9 | PTD3 | ⓪ | "L" output (P3 output) or negative polarity output (G signal output). | P3 pin data control. |
| | | 1 | "H" output (P3 output) or positive polarity output (G signal output). | |
| A | PTD4 | ⓪ | "L" output (P2 output). | P4 pin exclusive port output state control. |
| | | 1 | "H" output (P2 output). | |
| B | PTD5 | ⓪ | "L" output (P5 output) or negative polarity output (B signal output). | P5 pin data control. |
| | | 1 | "H" output (P5 output) or positive polarity output (B signal output). | |
| C | PTD6 | ⓪ | "L" output (P6 output). | P6 pin exclusive port output state control. |
| | | 1 | "H" output (P6 output). | |
| D | PTD7 | ⓪ | "L" output (P7 output). | P7 pin exclusive port output state control. |
| | | 1 | "H" output (P7 output). | |

(3) Address 122₁₆

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | HP0 (LSB) | Ⓞ | If HS is the horizontal display start location, $HS = T \times (\sum_{n=0}^{9} 2^n HP_n + N)$. | Horizontal display start location is specified using the 10 bits from HP9 to HP0. |
| | | 1 | | Note: HP9 to 0 = (0000000000₂) and (0000010111₂) setting is forbidden |
| 1 | HP1 | Ⓞ | T: The cycle of display frequency | |
| | | 1 | | |
| 2 | HP2 | Ⓞ | | |
| | | 1 | | |
| 3 | HP3 | Ⓞ | 1000 settings are possible. | |
| | | 1 | | |
| 4 | HP4 | Ⓞ | | |
| | | 1 | | |
| 5 | HP5 | Ⓞ | | |
| | | 1 | | |
| 6 | HP6 | Ⓞ | | |
| | | 1 | | |
| 7 | HP7 | Ⓞ | | |
| | | 1 | | |
| 8 | HP8 | Ⓞ | | |
| | | 1 | | |
| 9 | HP9 (MSB) | Ⓞ | | |
| | | 1 | | |
| A | TEST9 | Ⓞ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| B | SPACE0 | Ⓞ | | Leave one line worth of space in the vertical direction. |
| | | 1 | | For example, 6 Ⓢ 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7. |
| C | SPACE1 | Ⓞ | | A line is 18 × N horizontal scan lines. |
| | | 1 | | N is determined by the character size in the vertical direction as follows: |
| D | SPACE2 | Ⓞ | | ×1 N = 1   ×2 N = 2 |
| | | 1 | | ×3 N = 3   ×4 N = 4 |

Function column inner table (HP registers):

| HSZ11 HSZ21 | HSZ10 HSZ20 | N |
|---|---|---|
| 0 | 0 | 6 |
| 0 | 1 | 7 |
| 1 | 0 | 8 |
| 1 | 1 | 9 |

Function column inner table (SPACE registers):

| SPACE 2 | 1 | 0 | Number of Lines and Space (Ⓢ represents space) |
|---|---|---|---|
| 0 | 0 | 0 | 12 |
| 0 | 0 | 1 | 1 Ⓢ 10 Ⓢ 1 |
| 0 | 1 | 0 | 2 Ⓢ 8 Ⓢ 2 |
| 0 | 1 | 1 | 3 Ⓢ 6 Ⓢ 3 |
| 1 | 0 | 0 | 4 Ⓢ 4 Ⓢ 4 |
| 1 | 0 | 1 | 5 Ⓢ 2 Ⓢ 5 |
| 1 | 1 | 0 | 6 Ⓢ 6 |
| 1 | 1 | 1 | 6 Ⓢ Ⓢ 6 |

Ⓢ represents one line worth of spaces.

(4) Address 123₁₆

| DA | Register | Contents | | Remarks |
|----|----------|----------|---|---------|
| | | Status | Function | |
| 0 | VP0 (LSB) | ⓪ | If VS is the vertical display start location, | The vertical start location is specified using the 10 bits from VP9 to VP0. |
| | | 1 | $VS = H \times ( \sum_{n=0}^{9} 2^n VPn )$. | VP9 to VP0 = (0000000000₂) setting is forbidden. |
| 1 | VP1 | ⓪ | H: Cycle with the horizontal synchronizing pulse | Note 1: In case of B/F register is "0". |
| | | 1 | 1023 settings are possible. | |
| 2 | VP2 | ⓪ | | |
| | | 1 | | |
| 3 | VP3 | ⓪ | | |
| | | 1 | | |
| 4 | VP4 | ⓪ | | |
| | | 1 | | |
| 5 | VP5 | ⓪ | | |
| | | 1 | | |
| 6 | VP6 | ⓪ | | |
| | | 1 | | |
| 7 | VP7 | ⓪ | | |
| | | 1 | | |
| 8 | VP8 | ⓪ | | |
| | | 1 | | |
| 9 | VP9 (MSB) | ⓪ | | |
| | | 1 | | |
| A | TEST0 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| B | TEST1 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| C | TEST2 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| D | TEST3 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |

(5) Address 124$_{16}$

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | DSP0 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 1. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 1 | DSP1 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 2. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 2 | DSP2 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 3. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 3 | DSP3 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 4. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 4 | DSP4 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 5. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 5 | DSP5 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 6. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 6 | DSP6 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 7. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 7 | DSP7 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 8. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 8 | DSP8 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 9. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| 9 | DSP9 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. (Note) | Sets the display mode of line 10. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| A | DSP10 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. | Sets the display mode of line 11. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| B | DSP11 | ⓪ | Blanking is in the display mode specified by BLK0 and BLK1. | Sets the display mode of line 12. |
| | | 1 | Blanking is in the display mode specified by except BLK0 and BLK1. | |
| C | TEST4 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| D | TEST5 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |

Note: Refer to DISPLAY FORM1.

(6) Address 125₁₆

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | LIN2 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1.<br>The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 2nd line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1.<br>The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 1 | LIN3 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1.<br>The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 3rd line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1.<br>The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 2 | LIN4 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1.<br>The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 4th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1.<br>The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 3 | LIN5 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1.<br>The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 5th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1.<br>The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 4 | LIN6 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1.<br>The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 6th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1.<br>The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 5 | LIN7 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1.<br>The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 7th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1.<br>The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 6 | LIN8 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1.<br>The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 8th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1.<br>The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 7 | LIN9 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1.<br>The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 9th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1.<br>The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 8 | V1SZ0 | Ⓞ | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction for the 1st line.<br>(display monitor 1 ~ 12 line) |
| | | 1 | | |
| 9 | V1SZ1 | Ⓞ | V1SZ1 / V1SZ0 / Vertical direction size<br>0 / 0 / 1H/dot<br>0 / 1 / 2H/dot<br>1 / 0 / 3H/dot<br>1 / 1 / 4H/dot | |
| | | 1 | | |
| A | VSZ1L0 | Ⓞ | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 ~ LIN17. |
| | | 1 | | |
| B | VSZ1L1 | Ⓞ | VSZ1L1 / VSZ1L0 / Vertical direction size<br>0 / 0 / 1H/dot<br>0 / 1 / 2H/dot<br>1 / 0 / 3H/dot<br>1 / 1 / 4H/dot | |
| | | 1 | | |
| C | VSZ1H0 | Ⓞ | H: Cycle with the horizontal synchronizing pulse | Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 ~ LIN17. |
| | | 1 | | |
| D | VSZ1H1 | Ⓞ | VSZ1H1 / VSZ1H0 / Vertical direction size<br>0 / 0 / 1H/dot<br>0 / 1 / 2H/dot<br>1 / 0 / 3H/dot<br>1 / 1 / 4H/dot | |
| | | 1 | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address 126₁₆

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | LIN10 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 10th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 1 | LIN11 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 11th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 2 | LIN12 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 12th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 3 | LIN13 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 13th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 4 | LIN14 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 14th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 5 | LIN15 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 15th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 6 | LIN16 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 16th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |
| 7 | LIN17 | Ⓞ | The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1. | Character size setting in the vertical direction for the 17th line. |
| | | 1 | The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1. | |

| DA | Register | Status | H: Cycle with the horizontal synchronizing pulse | Remarks |
|---|---|---|---|---|
| 8 | V18SZ0 | Ⓞ | | Character size setting in the vertical direction for the 18th line. (display monitor 1 ~ 12 line) |
| | | 1 | V18SZ1 / V18SZ0 / Vertical direction size: 0 0 → 1H/dot | |
| 9 | V18SZ1 | Ⓞ | 0 1 → 2H/dot; 1 0 → 3H/dot | |
| | | 1 | 1 1 → 4H/dot | |
| A | VSZ2L0 | Ⓞ | | Character size setting in the vertical direction (display monitor for 2 ~ 12 line) at "0" state in register LIN2 ~ LIN17. |
| | | 1 | VSZ2L1 / VSZ2L0 / Vertical direction size: 0 0 → 1H/dot | |
| B | VSZ2L1 | Ⓞ | 0 1 → 2H/dot; 1 0 → 3H/dot | |
| | | 1 | 1 1 → 4H/dot | |
| C | VSZ2H0 | Ⓞ | | Character size setting in the vertical direction (display monitor for 2 ~ 12 line) at "1" state in register LIN2 ~ LIN17. |
| | | 1 | VSZ2H1 / VSZ2H0 / Vertical direction size: 0 0 → 1H/dot | |
| D | VSZ2H1 | Ⓞ | 0 1 → 2H/dot; 1 0 → 3H/dot | |
| | | 1 | 1 1 → 4H/dot | |

(8) Address 127₁₆

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | RR | ⓪ | <table><tr><td>RB</td><td>RG</td><td>RR</td><td>Color</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr></table> | Sets the color of all blankings. |
| | | 1 | 0 0 1 Red | |
| 1 | RG | ⓪ | 0 1 0 Green<br>0 1 1 Yellow<br>1 0 0 Blue | |
| | | 1 | 1 0 1 Magenta | |
| 2 | RB | ⓪ | 1 1 0 Cyan<br>1 1 1 White | |
| | | 1 | | |
| 3 | FR | ⓪ | <table><tr><td>BB</td><td>BG</td><td>BR</td><td>Color</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr></table> | Sets the blanking color of the Border size, or the shadow size. |
| | | 1 | 0 0 1 Red | |
| 4 | FG | ⓪ | 0 1 0 Green<br>0 1 1 Yellow<br>1 0 0 Blue | |
| | | 1 | 1 0 1 Magenta | |
| 5 | FB | ⓪ | 1 1 0 Cyan<br>1 1 1 White | |
| | | 1 | | |
| 6 | TEST6 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| 7 | TEST7 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| 8 | TEST8 | ⓪ | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| 9 | BETA14 | ⓪ | Matrix-outline display (12 × 18 dot) | Set this register to the character font set by display RAM BR, BG and BB. |
| | | 1 | Matrix-outline display (14 × 18 dot) | |
| A | HSZ10 | ⓪ | T: Display frequency cycle | Character size setting in the vertical direction for the first line. |
| | | 1 | <table><tr><td>HSZ11</td><td>HSZ10</td><td>Vertical direction size</td></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr></table> | |
| B | HSZ11 | ⓪ | 0 1 2T/dot<br>1 0 3T/dot | |
| | | 1 | 1 1 4T/dot | |
| C | HSZ20 | ⓪ | T: Display frequency cycle | Character size setting in the vertical direction for the 2nd line to 12th line. |
| | | 1 | <table><tr><td>VSZ21</td><td>HSZ20</td><td>Vertical direction size</td></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr></table> | |
| D | HSZ21 | ⓪ | 0 1 2T/dot<br>1 0 3T/dot | |
| | | 1 | 1 1 4T/dot | |

(9) Address 128₁₆

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | BCOL | ⓪ | Blanking of BLK0, BLK1 | Sets all raster blanking |
| | | 1 | All raster blanking | |
| 1 | B/F̄ | ⓪ | Synchronize with the leading edge of horizontal synchronization. | Synchronize with the front porch or back porch of the horizontal synchronazation signal. |
| | | 1 | Synchronize with the trailing edge of horizontal synchronization. | |
| 2 | VMASK | ⓪ | Do not mask by VERT input signal | This register has or do not have mask at phase comparison operating. |
| | | 1 | Mask by VERT input signal | |
| 3 | POLV | ⓪ | VERT pin polarity is negative electrode | Set VERT pin polarity. |
| | | 1 | VERT pin polarity is positive electrode | |
| 4 | POLH | ⓪ | HOR pin polarity is negative electrode | Set HOR pin polarity. |
| | | 1 | HOR pin polarity is positive electrode | |
| 5 | BLK0 | ⓪ / 1 | BLK: 1 / 0 — Blanking mode; 0 / 0 — Matrix-outline size; 0 / 1 — Character size; 1 / 0 — Border size; 1 / 1 — Matrix-outline size | Set blanking mode. (Note 1) An example of blanking mode at BCOL = "0", DSPn = "0" (n = 0 ~ 11) shown left. |
| 6 | BLK1 | ⓪ / 1 | | |
| 7 | SYAD | ⓪ | Border display of character | (Note 2) |
| | | 1 | Shadow display of character | |
| 8 | RAMERS | ⓪ | RAM not erased | There is no need to reset because there is no register for this bit. |
| | | 1 | RAM erased | |
| 9 | STOP | ⓪ | Oscillation of clock for display | R, G, B and BLNK0 output can be altered. |
| | | 1 | Stop the oscillation of clock for display | |
| A | DSPON | ⓪ | Display OFF | Display can be altered. |
| | | 1 | Display ON | |
| B | BLINK0 | ⓪ / 1 | BLINK: 1 / 0 — Duty; 0 / 0 — Blinking OFF; 0 / 1 — 25%; 1 / 0 — 50%; 1 / 1 — 75% | Blinking duty ratio can be altered. |
| C | BLINK1 | ⓪ / 1 | | |
| D | BLINK2 | ⓪ | Divided into 64 of vertical synchronous signal | Blinking frequency can be altered. |
| | | 1 | Divided into 32 of vertical synchronous signal | |

Notes 1: Refer to DISPLAY FORM 1
       2: Refer to DISPLAY FORM 3

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

## DISPLAY FORM1

Table 1 shows display form of blanking.

**Table 1. Display mode**

| BCOL | Standard blanking | | When the all of registers DSPn (Note 2) are set to "0" | When some of registers DSPi are set to "1" | | BLNK0 output |
|---|---|---|---|---|---|---|
| | BLK1 | BLK0 | | DSPn = 0 | DSPn = 1 | |
| 0 | 0 | 0 | Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4) | Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4) | Matrix-outline display color set: display RAM (Note 3) | DSPn = "0" line ⌐ DSPn = "1" line ⌐ Matrix-outline size |
| | 0 | 1 | Character | Character | Border display color set: display RAM (Note 3) | DSPn = "0" line→Character size DSPn = "1" line→Border size |
| | 1 | 0 | Border display color set: display RAM (Note 3) | Border display color set: display RAM (Note 3) | Matrix-outline display color set: display RAM (Note 3) | DSPn = "0" line→Border size DSPn = "1" line→Matrix-outline size |
| | 1 | 1 | Matrix-outline display color set: display RAM (Note 3) | Matrix-outline display color set: display RAM (Note 3) | Character | DSPn = "0" line→Matrix-outline size DSPn = "1" line→Character size |
| 1 (Note 1) | 0 | 0 | Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4) | Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4) | Matrix-outline display color set: display RAM (Note 3) | All blanking size |
| | 0 | 1 | Character | Character | Border display color set: display RAM (Note 3) | |
| | 1 | 0 | Border display color set: display RAM (Note 3) | Border display color set: display RAM (Note 3) | Matrix-outline display color set: display RAM (Note 3) | |
| | 1 | 1 | Matrix-outline display color set: display RAM (Note 3) | Matrix-outline display color set: display RAM (Note 3) | Character | |

Notes 1: Color setting of raster area is set by register RR, RG and RB.
2: DSPn (n = 0 ~ 11)
3: Set by BR, BG and BB of display RAM.
4: Set border by register FR, FG and FB. Set matrix-outline by BR, BG and BB of display RAM.

## Display form 2

M35043-XXXSP has the following four display forms.

(1) Character size
: Blanking same as the character size.

(2) Border size
: Blanking the background as a size from character.

(3) Matrix-outline size
: Blanking the background 12 × 18 dot.
When set register BETA14 to "1", setting of blanking the background 14 × 18 dot is possible.

(4) All blanking size
: When set register BCOL to "1", all raster area is blanking.



( Register BCOL = "0" )

| 12dots | 12dots | 12dots | 12dots |

Scanning →

Set character color by display RAM*1 (address 0 to 11F16)

Set border color by display RAM*1

Set matrix - outline color by display RAM*3

Set border color by register FR,FG and FB

R,G or B output

Set matrix - outline color by RAM for display*3

BLNK0 output

(1) Character display (character size)*2

(2) Border display (border size)

(3) Matrix - outline display (matrix-outline size)

(4) Matrix - outline and border display (matrix-outline size)

( Register BCOL = "1" )

| 12dots | 12dots | 12dots | 12dots |

Scanning →

Set character color by display RAM*1 (address 0 to 11F16)

Set raster area color by register RR,RG and RB

Set matrix - outline color by display RAM*3

Set border color by register FR,FG and FB

R,G or B output

"H" level

Set border color by display RAM*1

Set matrix - outline color by display RAM*3

BLNK0 output GND level

(1) Character display (all blanking size)*2

(2) Border display (all blanking size)

(3) Matrix - outline display (all blanking size)

(4) Matrix - outline and border display (all blanking size)

*1 Red,Blue,Yellow,Green,Magenta,Cyan, White and Black are set possible.
*2 ( ) is blanking mode.
*3 Matrix - outline horizontal direction size is able to set to 14dots by register BETA14 (BLNK0 output by 14dots).
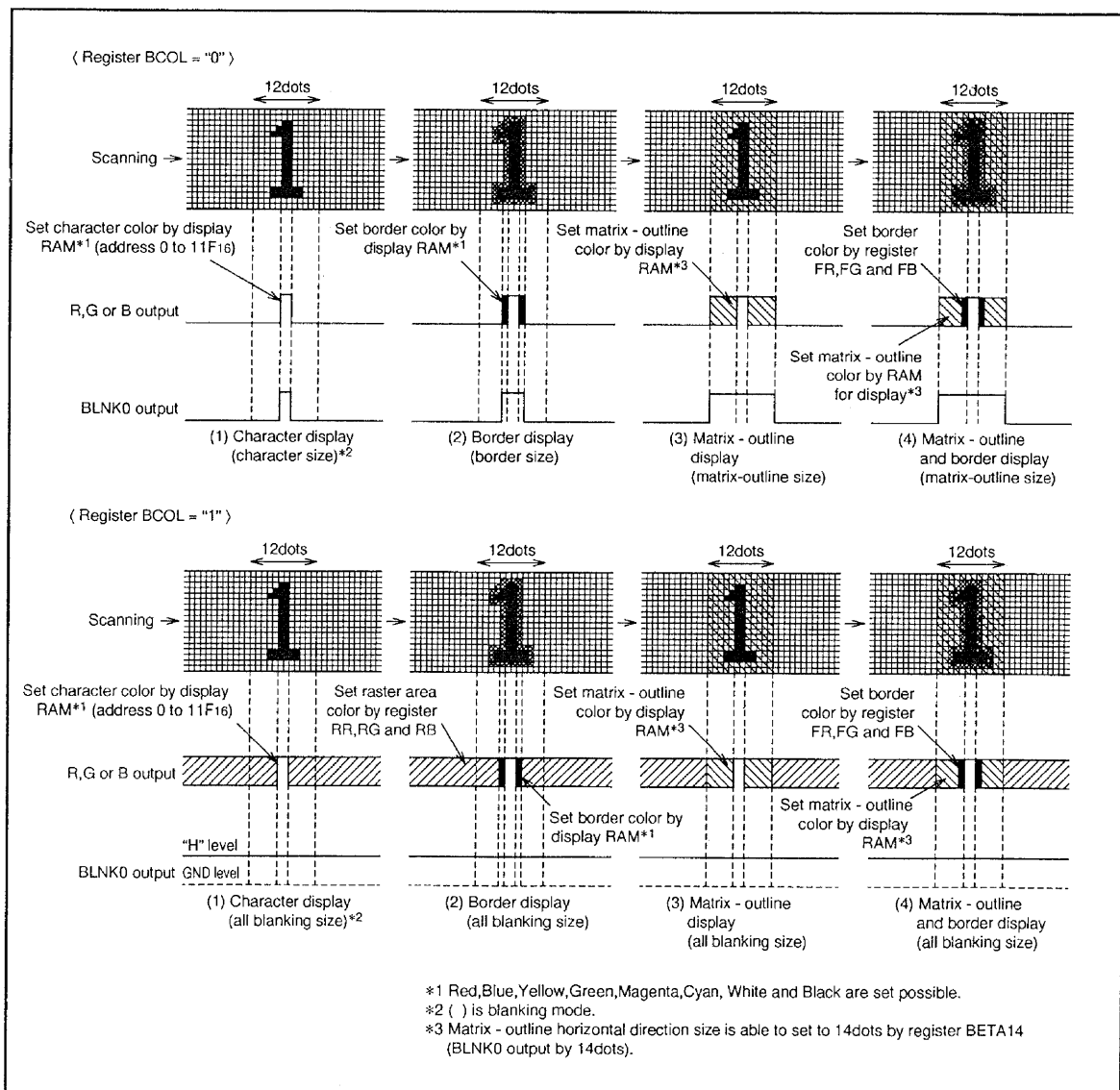
Fig. 3  Display form

## Display form 3

When border display mode, if set SYAD = "0" to "1", it change to
shadow display mode.
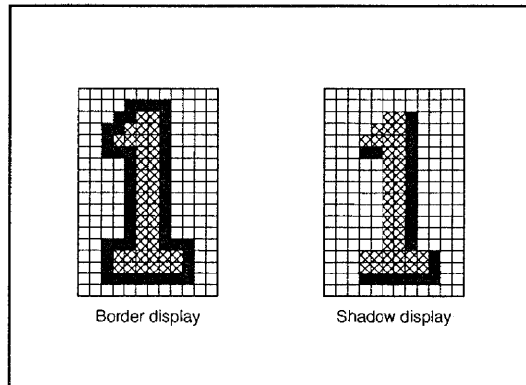Border and shadow display are shown below.



Fig. 4  Border and shadow display

Set shadow display color by display RAM or register FR, FG and FB.

## DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting is shown in Figure 5.

### Example of data setting by the serial input function (M35043-XXXSP/FP)

| | | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Addition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 200 msec hold | | | | | | | | | | | | | | | | System set-up |
| 1 | address 120₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Address set |
| 2 | data 120₁₆ | 0 | 0 | 0 | DIVS1 | DIVS0 | DIV10 | DIV9 | DIV8 | DIV7 | DIV6 | DIV5 | DIV4 | DIV3 | DIV2 | DIV1 | DIV0 | Setting frequency dividing value (Note 1) |
| 3 | data 121₁₆ | 0 | 0 | PTD7 | PTD6 | 1 | PTD4 | 1 | PTD2 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Output setting |
| 4 | data 122₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | HP9 | HP8 | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 | Horizontal display location setting |
| 5 | data 123₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | VP9 | VP8 | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | Vertical display location setting |
| 6 | data 124₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Display form setting |
| 7 | data 125₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Character size setting |
| 8 | data 126₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Character size setting |
| 9 | data 127₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Color, character size setting |
| 10 | data 128₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | POLH | POLV | 0 | 0 | 0 | Display OFF, display form (Note 2) |
| | | 200 msec hold | | | | | | | | | | | | | | | | |
| 11 | data 000₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| 12 ⋮ 297 | | ⋮ | ⋮ | Character background color | | | Blink-ing | Character color | | | ⋮ | Character code | | | | | | Character setting |
| 298 | data 11F₁₆ | 0 | BB | BG | BR | BLINK | B | G | R | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| 299 | address 128₁₆ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Address setting |
| 300 | data 128₁₆ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | POLH | POLV | 0 | 0 | 0 | Display ON, display form (Note 2) |

Notes 1: Input horizontal synchronous signal to HOR pin.
2: Matrix-outline display in this data.

Fig. 5  Example of data setting by the serial input function

## SERIAL DATA INPUT TIMING

(1) Serial data should be input with the LSB first.

(2) The address consists of 16 bits.

(3) The data consists of 16 bits.

(4) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.
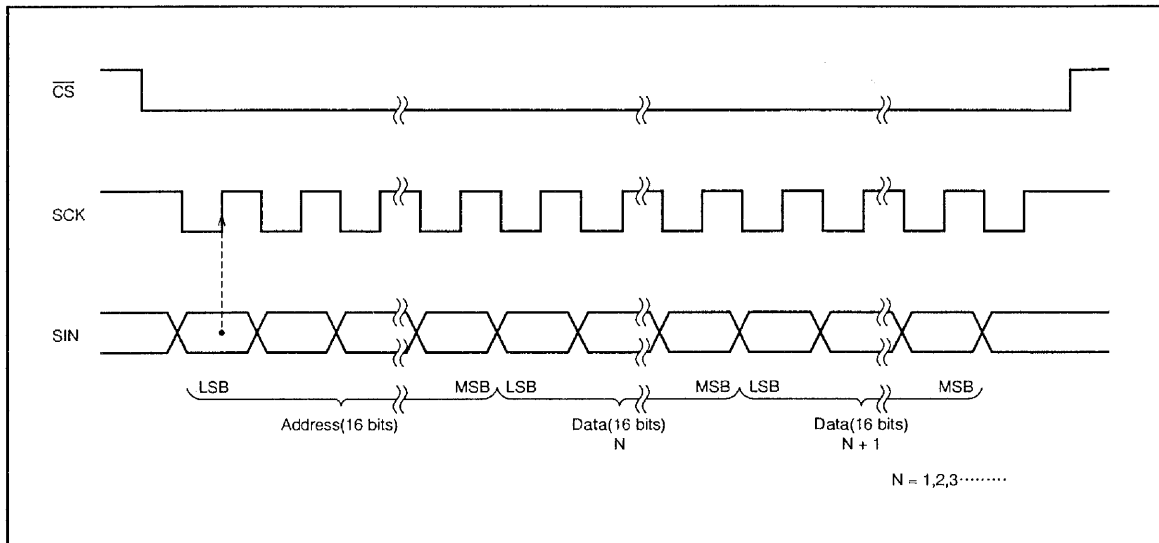


**Fig. 6   Serial input timing**

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## CHARACTER FONT

Images are composed on a 12 x 18 dot matrix, and characters can
be linked vertically and horizontally with other characters to allow the
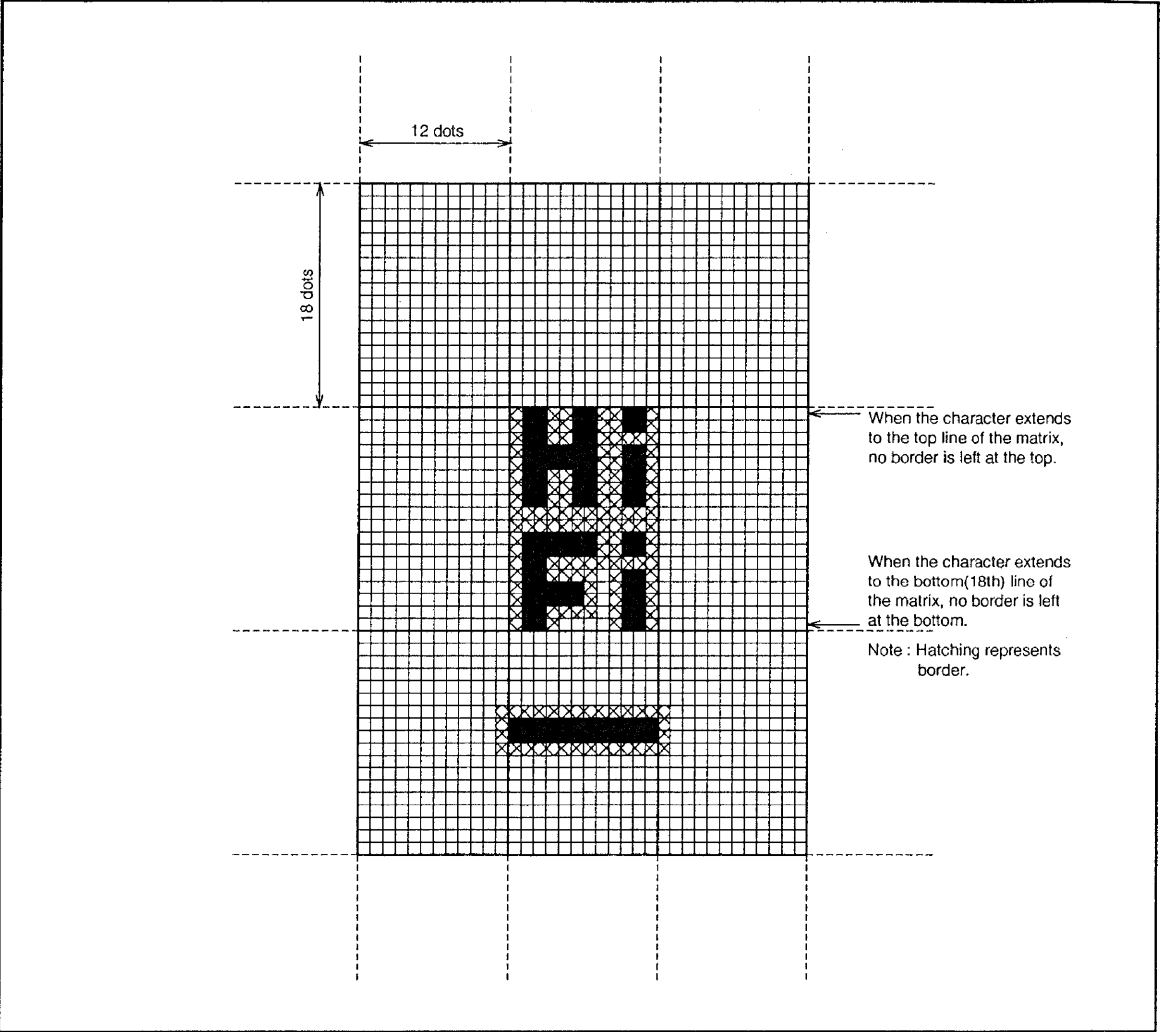display the continuous symbols.



12 dots

18 dots

When the character extends
to the top line of the matrix,
no border is left at the top.

When the character extends
to the bottom(18th) line of
the matrix, no border is left
at the bottom.

Note : Hatching represents
border.

**Fig. 7  Example for displaying a continuous pattern after combining characters in the horizontal or vertical direction**

Character code FF$_{16}$ is fixed as a blank without background.
Therefore, you cannot register a character font in this code.

## TIMING REQUIREMENTS (Ta = −20°C to + 85°C, VDD = 5±0.25V, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| tw(SCK) | SCK width | 200 | — | — | ns | See Figure 8 |
| tsu(CS) | CS setup time | 200 | — | — | ns | |
| th(CS) | CS hold time | 2 | — | — | μs | |
| tsu(SIN) | SIN setup time | 200 | — | — | ns | |
| th(SIN) | SIN hold time | 200 | — | — | ns | |
| tword | 1 word writing time | 10 | — | — | μs | |



**Fig. 8  Serial input timing requirements**

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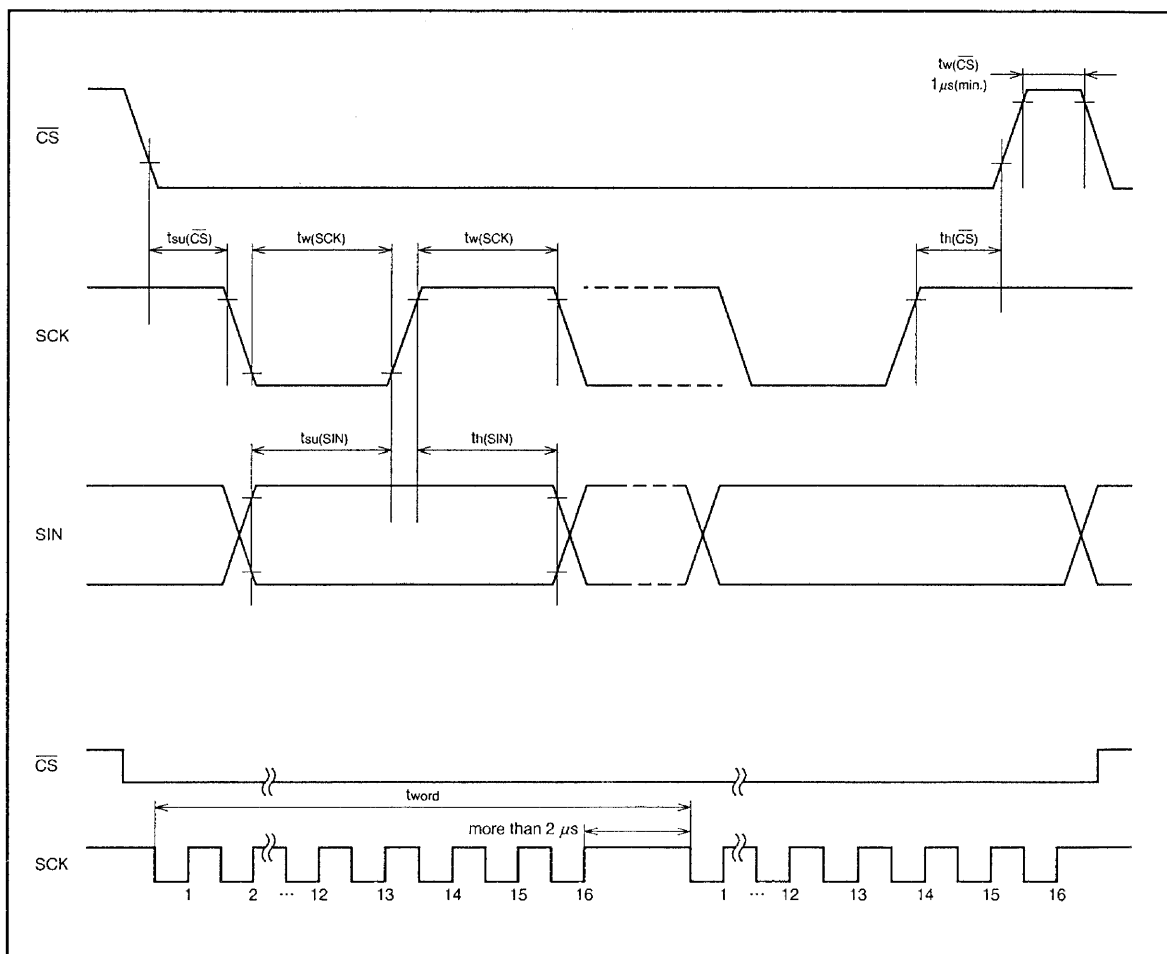
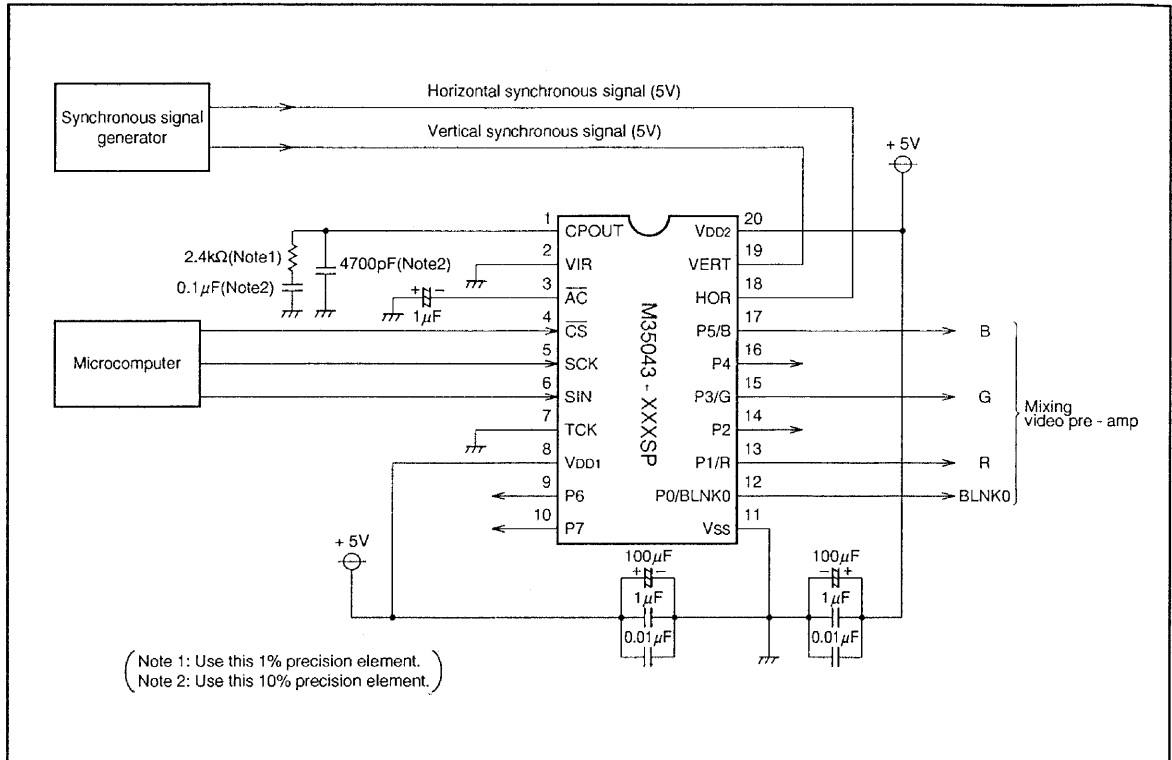## EXAMPLE OF THE M35043-XXXSP/FP PERIPHERAL CIRCUIT



Fig. 9 Example of the M35043-XXXSP peripheral circuit (M35043-XXXFP peripheral circuit is same as that of M35043-XXXSP)

## Note for waveform timing of the horizontal signals to the HOR pin.

Set horizontal synchronous signal edge* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/F register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by B/F register.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS
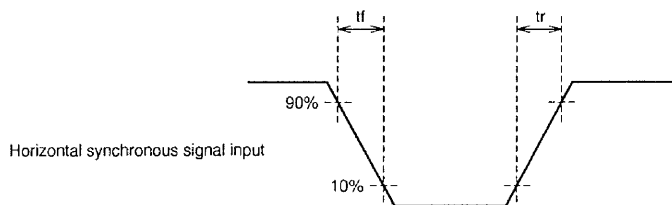
## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | With respect to Vss. | −0.3 to +6.0 | V |
| $V_I$ | Input voltage | | $V_{SS} -0.3 \leq V_I \leq V_{DD} +0.3$ | V |
| $V_O$ | Output voltage | | $V_{SS} \leq V_O \leq V_{DD}$ | V |
| $P_d$ | Power dissipation | Ta = 25°C | 300 | mW |
| $T_{opr}$ | Operating temperature | | −20 to +85 | °C |
| $T_{stg}$ | Storage temperature | | −40 to +125 | °C |

## RECOMMENDED OPERATING CONDITIONS ($V_{DD}$ = 5V, Ta = −20 to +85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $V_{DD}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | "H" level input voltage SIN, SCK, CS, AC HOR, VERT | $0.8V_{DD}$ | $V_{DD}$ | $V_{DD}$ | V |
| $V_{IL}$ | "L" level input voltage SIN, SCK, CS, AC HOR, VERT | 0 | 0 | $0.2V_{DD}$ | V |
| $F_{OSC}$ | Oscillating frequency for display | 30.0 | — | 60.0 | MHz |

## ELECTRICAL CHARACTERISTICS ($V_{DD}$ = 5V, Ta = 25°C, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{DD}$ | Supply voltage | | Ta = −20 to +85°C | 4.75 | 5.0 | 5.25 | V |
| $I_{DD}$ | Supply current | | $V_{DD}$ = 5.25V | — | 30 | 50 | mA |
| $V_{OH}$ | "H" level output voltage | P0 ~ P7 | $V_{DD}$ = 4.75V, IOH = 0.4mA | 3.5 | — | — | V |
| | | CPOUT | $V_{DD}$ = 4.75V, IOH = 0.05mA | | | | |
| $V_{OL}$ | "L" level output voltage | P0 ~ P7 | $V_{DD}$ = 4.75V, IOL = 0.4mA | — | — | 0.4 | V |
| | | CPOUT | $V_{DD}$ = 4.75V, IOL = 0.05mA | | | | |
| $R_I$ | Pull-up resistance SCK, AC, CS, SIN | | $V_{DD}$ = 5.0V | 10 | 30 | 100 | kΩ |

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## Note for Supplying Power

Timing of power supplying to $\overline{AC}$ pin
The internal circuit of M35043-XXXSP/FP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin in hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 10.

Timing of power supplying to $V_{DD1}$ and $V_{DD2}$.
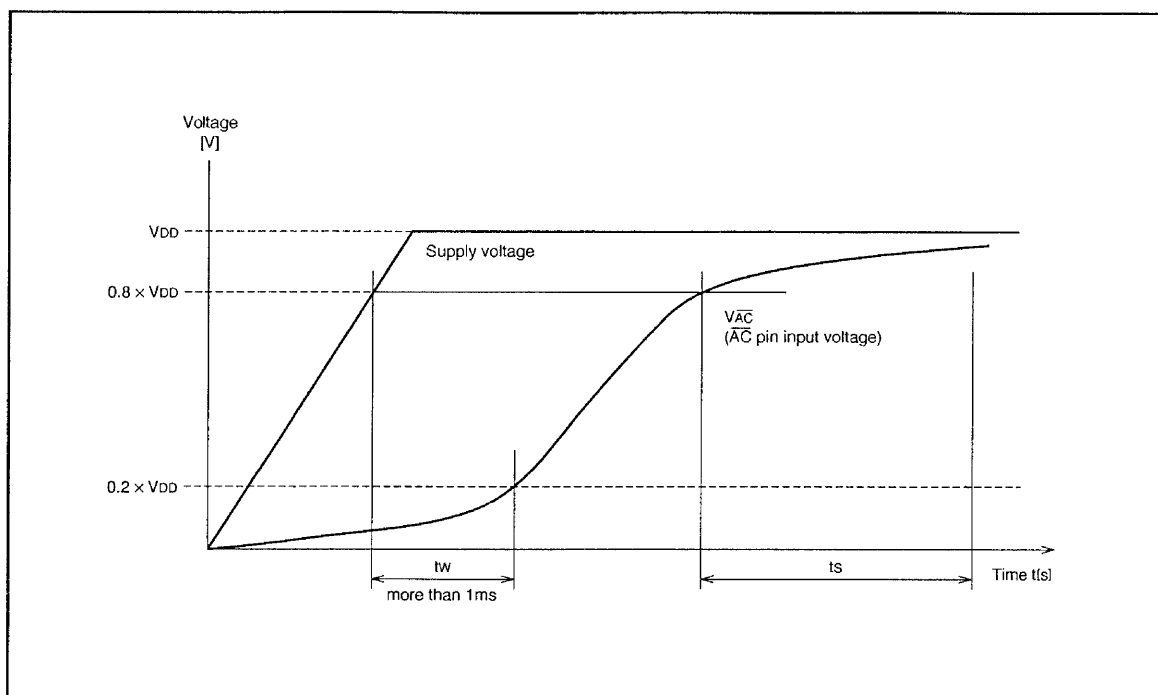Supply power to $V_{DD1}$ and $V_{DD2}$ at the same time.



**Fig. 10  Timing of power supplying to $\overline{AC}$ pin**

After supplying the power ($V_{DD}$ and $V_{SS}$) to M35043-XXXSP/FP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep $V_{IL}$ time; tw of the $\overline{AC}$ pin for more than 1ms.
Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than $0.8 \times V_{DD}$ and keeping 200ms wait time.

## PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1 \mu F$) directly between the $V_{DD1}$ pin and Vss pin, and the $V_{DD2}$ pin and Vss pin using a heavy wire.

## DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.
(1)  M35043-XXXSP/FP mask ROM order confirmation form
(2)  20P4B mask specification form
(3)  ROM data (EPROM 3 sets)
(4)  Floppy disks containing the character font generating program + character data

## STANDARD ROM TYPE : M35043-001SP/FP

M35043-001SP/FP is a standard ROM type of M35043-XXXSP/FP.
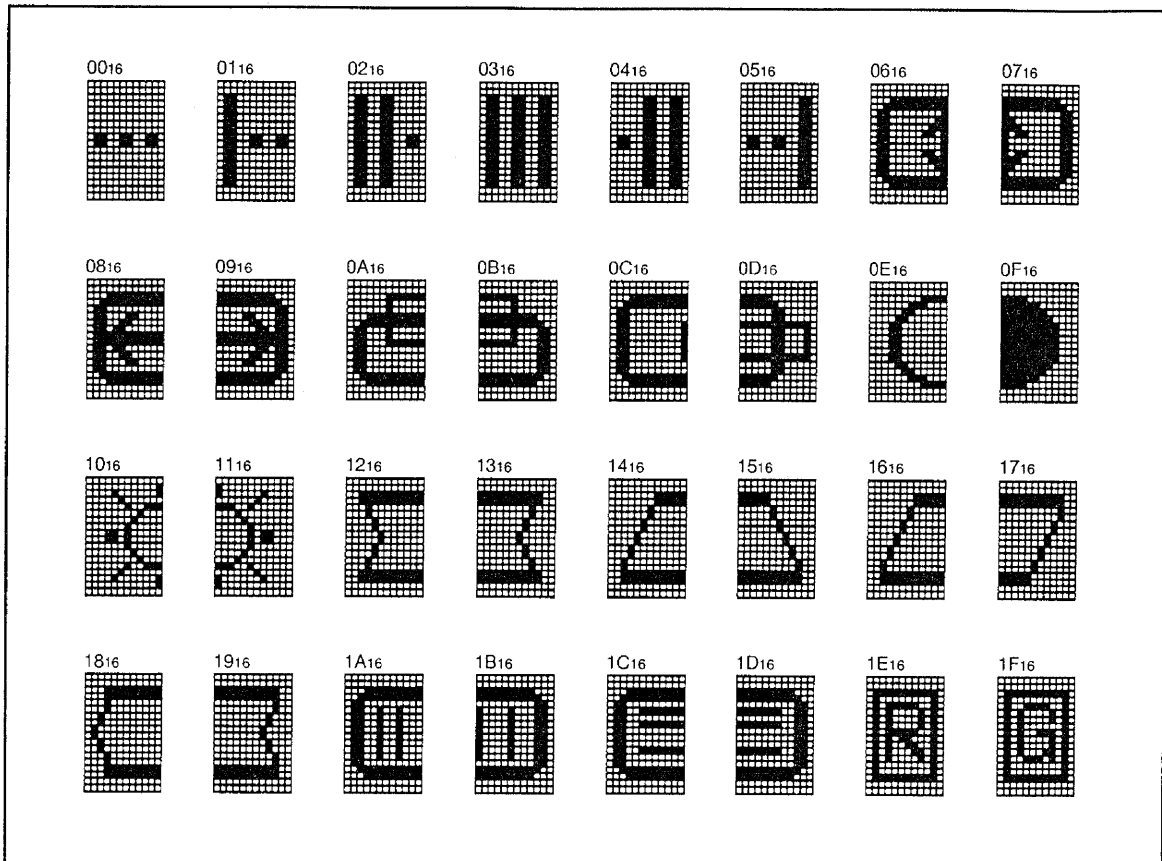The character patterns are fixed to the contents of Figure 11 to 13.



Fig. 11   M35043-001SP/FP character patterns (1)

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Fig. 12  M35043-001SP/FP character patterns (2)

Fig. 13  M35043-001SP/FP character patterns (3)

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