NCP5304

High Voltage, High and Low Side Driver

The NCP5304 is a High Voltage Power gate Driver providing two outputs for direct drive of 2 N-channel power MOSFETs or IGBTs arranged in a half-bridge configuration.

It uses the bootstrap technique to insure a proper drive of the High-side power switch. The driver works with 2 independent inputs with cross conduction protection.

Features

- High Voltage Range: up to 600 V
- dV/dt Immunity ±50 V/nsec
- Gate Drive Supply Range from 10 V to 20 V
- High and Low Drive Outputs
- Output Source / Sink Current Capability 250 mA / 500 mA
- 3.3 V and 5 V Input Logic Compatible
- Up to V_{CC} Swing on Input Pins
- Matched Propagation Delays between Both Channels
- Outputs in Phase with the Inputs
- Cross Conduction Protection with 100 ns Internal Fixed Dead Time
- Under V_{CC} LockOut (UVLO) for Both Channels
- Pin-to-Pin Compatible with Industry Standards
- These are Pb-Free Devices

Typical Applications

- Half-bridge Power Converters
- Full-bridge Converters

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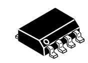
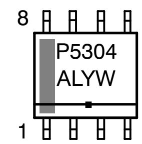
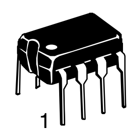
MARKING DIAGRAMS

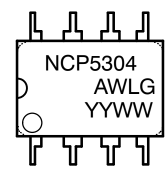


1
SOIC-8
D SUFFIX
CASE 751



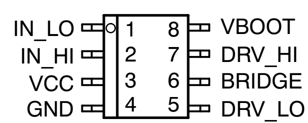


1
PDIP-8
P SUFFIX
CASE 626



NCP5304	= Specific Device Code
A	= Assembly Location
L or WL	= Wafer Lot
Y or YY	= Year
W or WW	= Work Week
G or ▪	= Pb-Free Package

PINOUT INFORMATION



8 Pin Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5304PG	PDIP-8 (Pb-Free)	50 Units / Rail
NCP5304DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

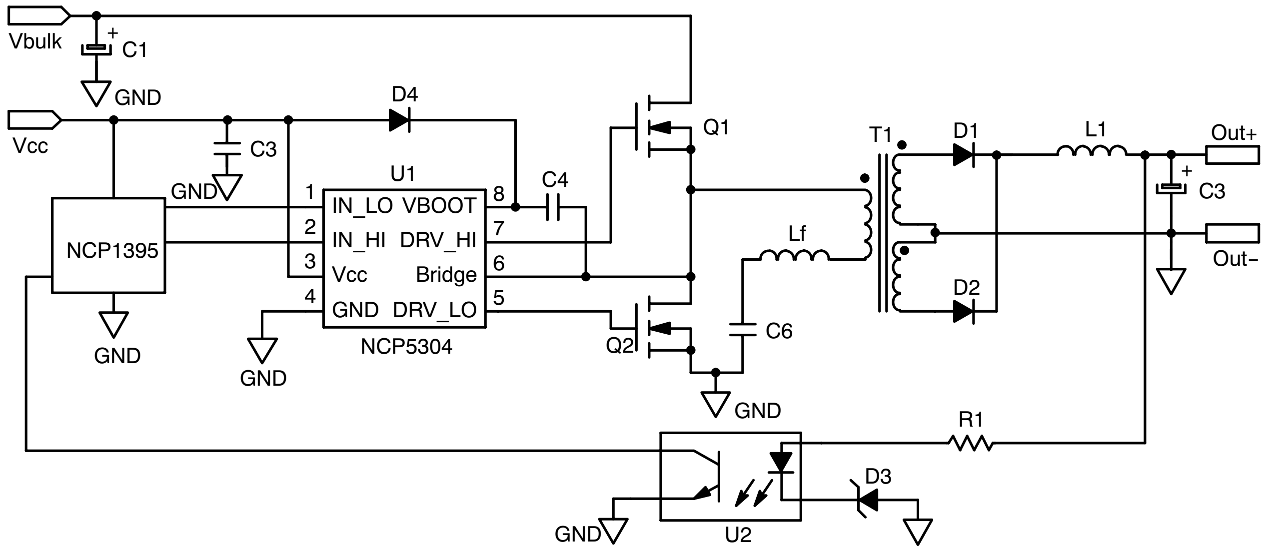


Figure 1. Typical Application Resonant Converter (LLC type)

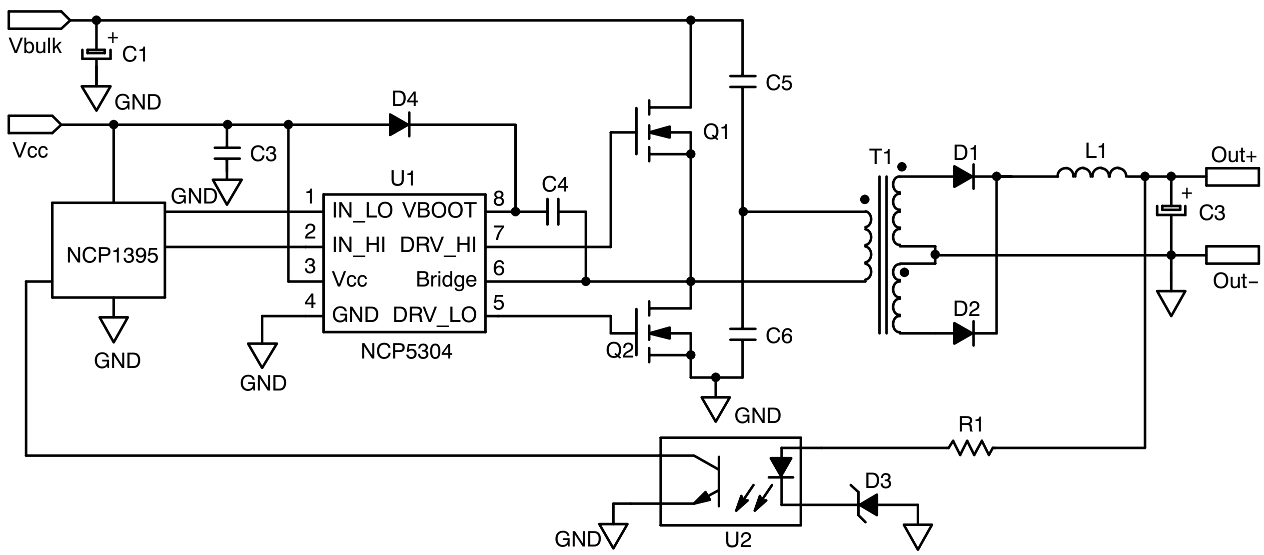


Figure 2. Typical Application Half Bridge Converter

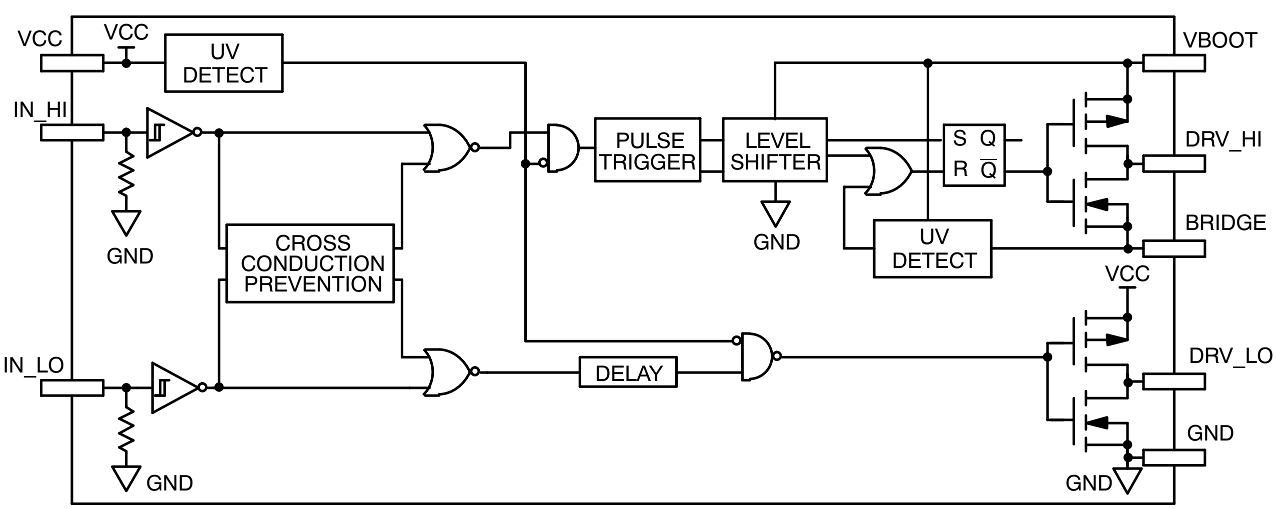


Figure 3. Detailed Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Function
1	IN_LO	Logic Input for Low side driver output in phase
2	IN_HI	Logic Input for High side driver output in phase
3	VCC	Low side and main power supply
4	GND	Ground
5	DRV_LO	Low side gate drive output
6	BRIDGE	Bootstrap return or High side floating supply return
7	DRV_HI	High side gate drive output
8	VBOOT	Bootstrap power supply

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC}	Main power supply voltage	−0.3 to 20	V
$V_{CC\_transient}$	Main transient power supply voltage: IV_{CC_max} = 5 mA during 10 ms	23	V
V_{BRIDGE}	VHV: High Voltage BRIDGE pin	−1 to 600	V
V_{BOOT}-V_{BRIDGE}	VHV: Floating supply voltage	−0.3 to 20	V
V_{DRV_HI}	VHV: High side output voltage	V_{BRIDGE} − 0.3 to V_{BOOT} + 0.3	V
V_{DRV_LO}	Low side output voltage	−0.3 to V_{CC} + 0.3	V
dV_{BRIDGE}/dt	Allowable output slew rate	50	V/ns
V_{IN_XX}	Inputs IN_HI, IN_LO	−1.0 to V_{CC} + 0.3	V
	ESD Capability: − HBM model (all pins except pins 6−7−8 in 8 pins package or 11−12−13 in 14 pins package) − Machine model (all pins except pins 6−7−8 in 8 pins package or 11−12−13 in 14 pins package)	 2 200	 kV V
	Latch up capability per Jedec JESD78		
$R_{\theta JA}$	Power dissipation and Thermal characteristics PDIP−8: Thermal Resistance, Junction−to−Air SO−8: Thermal Resistance, Junction−to−Air	 100 178	°C/W
T_{J_min} T_{J_max}	Operating Junction Temperature	−55 +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTIC (V_{CC} = V_{boot} = 15 V, V_{GND} = V_{bridge}, −40°C < T_J < 125°C, Outputs loaded with 1 nF)

Rating	Symbol	T_J −40°C to 125°C Min	Typ	Max	Units
OUTPUT SECTION					
Output high short circuit pulsed current V_{DRV} = 0 V, PW ≤ 10 μs (Note 1)	$I_{DRVsource}$	–	250	–	mA
Output low short circuit pulsed current V_{DRV} = Vcc, PW ≤ 10 μs (Note 1)	$I_{DRVsink}$	–	500	–	mA
Output resistor (Typical value @ 25°C) Source	R_{OH}	–	30	60	Ω
Output resistor (Typical value @ 25°C) Sink	R_{OL}	–	10	20	Ω
High level output voltage, V_{BIAS}−V_{DRV_XX} @ I_{DRV_XX} = 20 mA	V_{DRV_H}	–	0.7	1.6	V
Low level output voltage V_{DRV_XX} @ I_{DRV_XX} = 20 mA	V_{DRV_L}	–	0.2	0.6	V
DYNAMIC OUTPUT SECTION					
Turn−on propagation delay (Vbridge = 0 V)	t_{ON}	–	100	170	ns
Turn−off propagation delay (Vbridge = 0 V or 50 V) (Note 2)	t_{OFF}	–	100	170	ns
Output voltage rise time (from 10% to 90% @ Vcc = 15 V) with 1 nF load	tr	–	85	160	ns
Output voltage fall time (from 90% to 10% @V_{CC} = 15 V) with 1 nF load	tf	–	35	75	ns
Propagation delay matching between the High side and the Low side @ 25°C (Note 3)	Δt	–	20	35	ns
Internal fixed dead time (Note 4)	DT	65	100	190	ns
Minimum input width that changes the output	t_{PW1}	–	–	50	ns
Maximum input width that does not change the output	t_{PW2}	20	–	–	ns
INPUT SECTION					
Low level input voltage threshold	V_{IN}	–	–	0.8	V
Input pull−down resistor (V_{IN} < 0.5 V)	R_{IN}	–	200	–	kΩ
High level input voltage threshold	V_{IN}	2.3	–	–	V
Logic “1” input bias current @ V_{IN_XX} = 5 V @ 25°C	I_{IN+}	–	5	25	μA
Logic “0” input bias current @ V_{IN_XX} = 0 V @ 25°C	I_{IN-}	–	–	2.0	μA
SUPPLY SECTION					
Vcc UV Start−up voltage threshold	Vcc_stup	8.0	8.9	9.9	V
Vcc UV Shut−down voltage threshold	Vcc_shtdwn	7.3	8.2	9.1	V
Hysteresis on Vcc	Vcc_hyst	0.3	0.7	–	V
Vboot Start−up voltage threshold reference to bridge pin (Vboot_stup = Vboot − Vbridge)	Vboot_stup	8.0	8.9	9.9	V
Vboot UV Shut−down voltage threshold	Vboot_shtdwn	7.3	8.2	9.1	V
Hysteresis on Vboot	Vboot_shtdwn	0.3	0.7	–	V
Leakage current on high voltage pins to GND (V_{BOOT} = V_{BRIDGE} = DRV_HI = 600 V)	I_{HV_LEAK}	–	5	40	μA
Consumption in active mode (Vcc = Vboot, fsw = 100 kHz and 1 nF load on both driver outputs)	ICC1	–	4	5	mA
Consumption in inhibition mode (Vcc = Vboot)	ICC2	–	250	400	μA
Vcc current consumption in inhibition mode	ICC3	–	200	–	μA
Vboot current consumption in inhibition mode	ICC4	–	50	–	μA

1. Parameter guaranteed by design
2. Turn−off propagation delay @ Vbridge = 600 V is guaranteed by design
3. See characterization curve for Δt parameters variation on the full range temperature.
4. Both Integrated a dead time will be mesured and characterised. The first when IN_HI changes (High to Low and Low to High), and the second when HI_LO changes (High to Low and Low to High). These parameters will be updated after the characterization results.
5. Timing diagram definition see: Figure 5 and Figure 6.

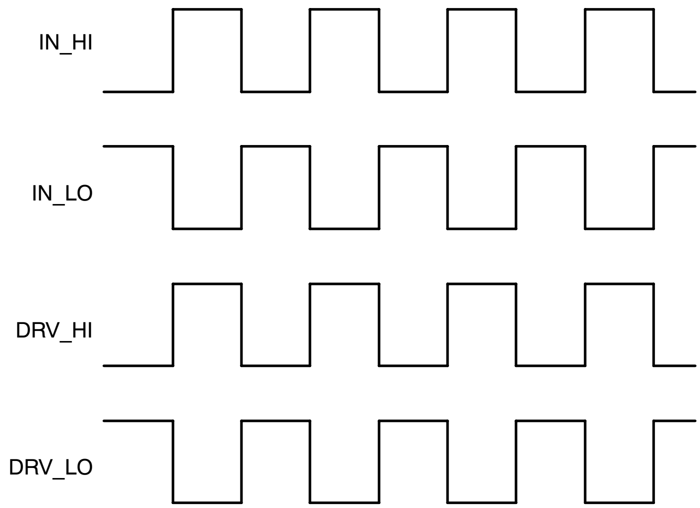


Figure 4. Input/Output Timing Diagram

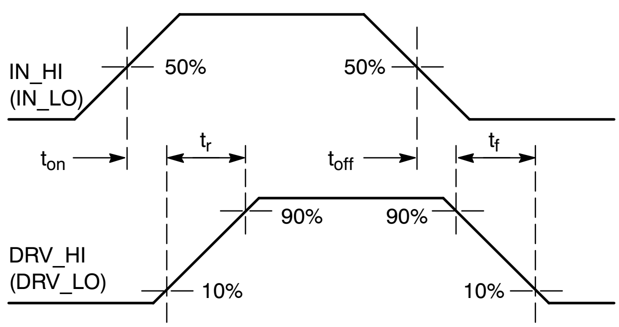


Figure 5. Propagation Delay and Rise / Fall Time Definition

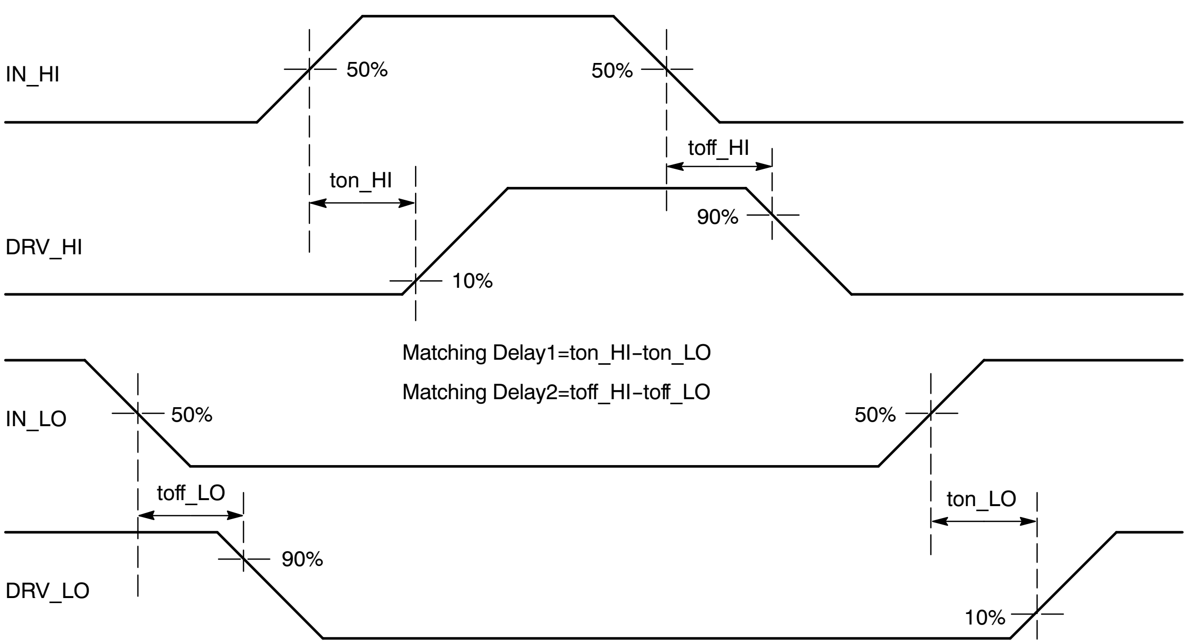


Figure 6. Matching Propagation Delay

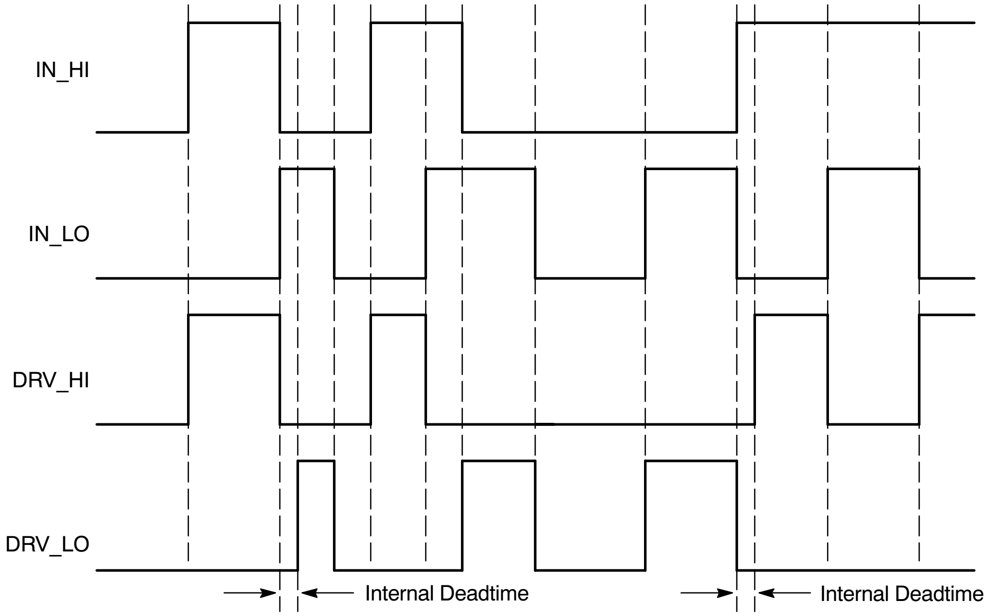


Figure 7. Input/Output Cross Conduction Output Protection Timing Diagram

CHARACTERIZATION CURVES

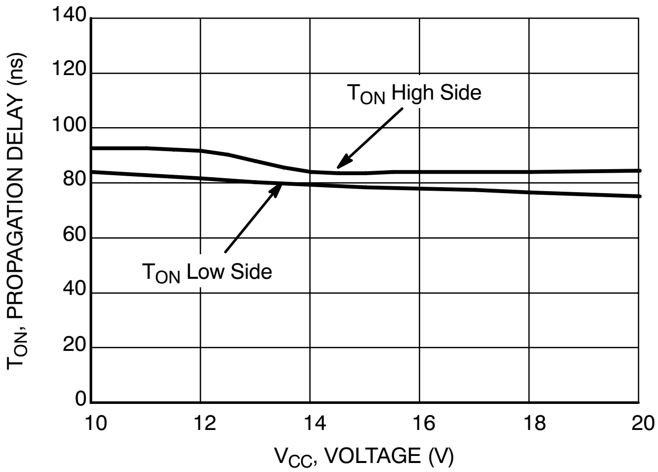


Figure 8. Turn ON Propagation Delay vs. Supply Voltage (V_{CC} = V_{BOOT})

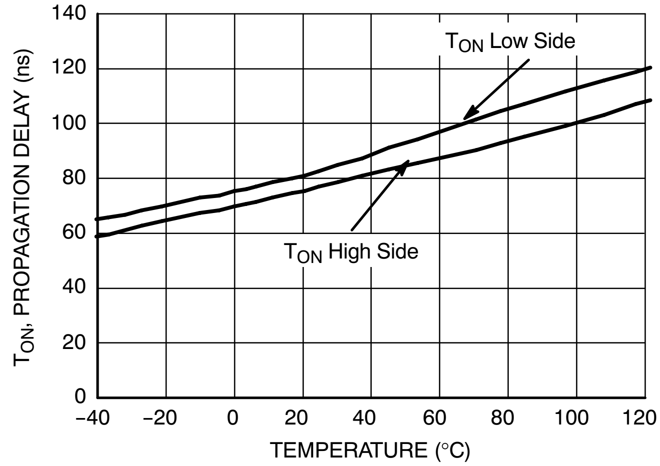


Figure 9. Turn ON Propagation Delay vs. Temperature

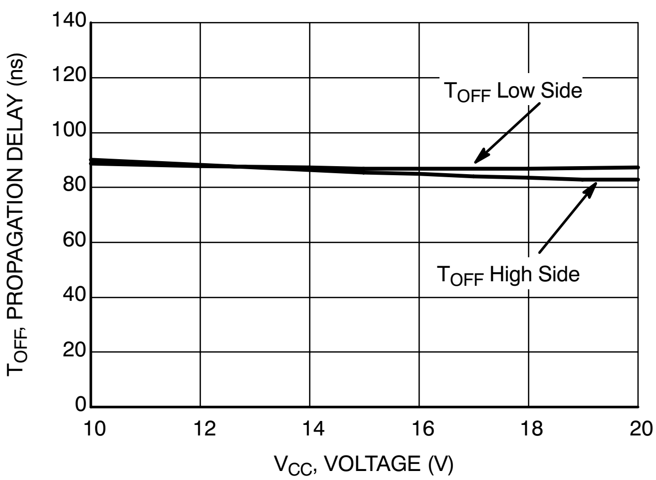


Figure 10. Turn OFF Propagation Delay vs. Supply Voltage (V_{CC} = V_{BOOT})

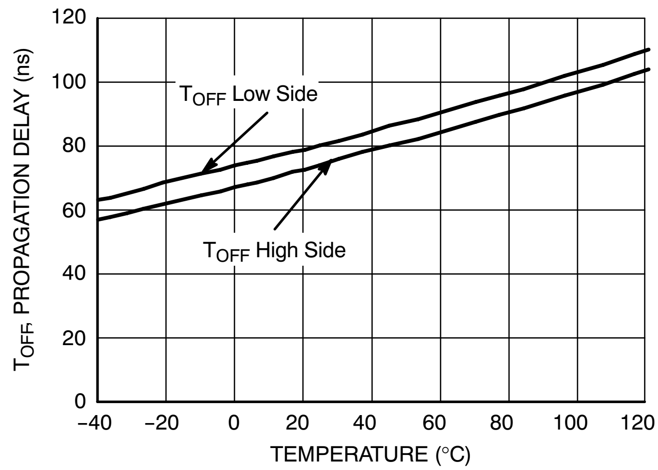


Figure 11. Turn OFF Propagation Delay vs. Temperature

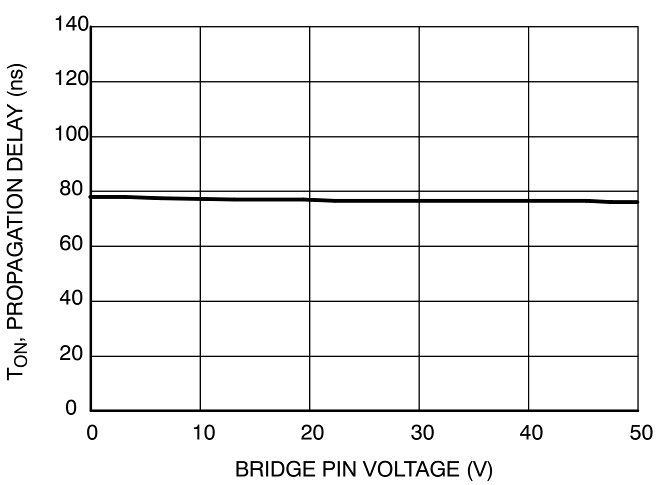


Figure 12. High Side Turn ON Propagation Delay vs. VBRIDGE Voltage

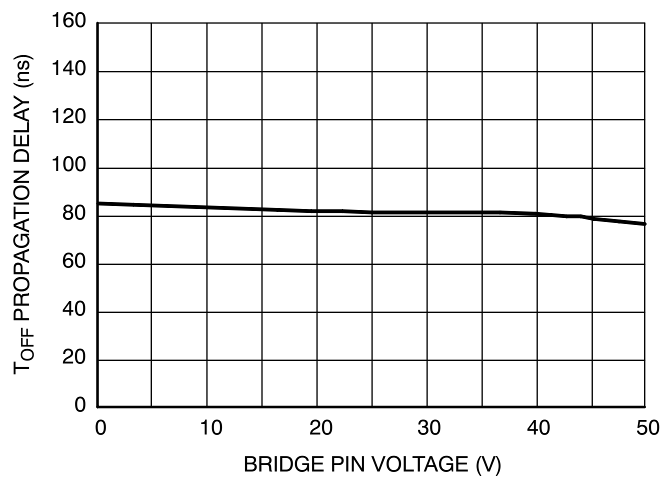


Figure 13. High Side Turn OFF Propagation Delay vs. VBRIDGE Voltage

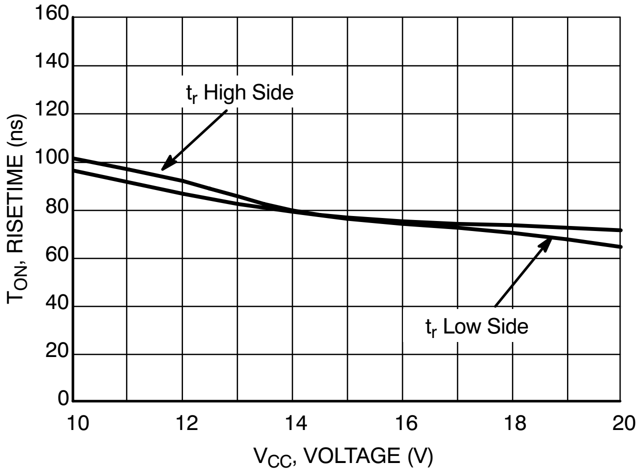


Figure 14. Turn ON Risetime vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

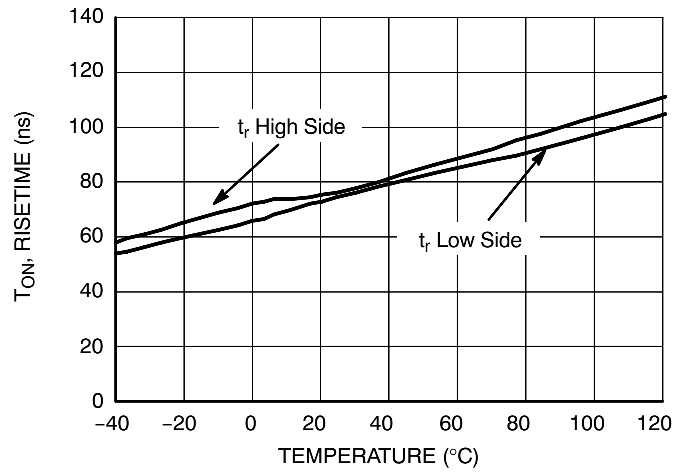


Figure 15. Turn ON Risetime vs. Temperature

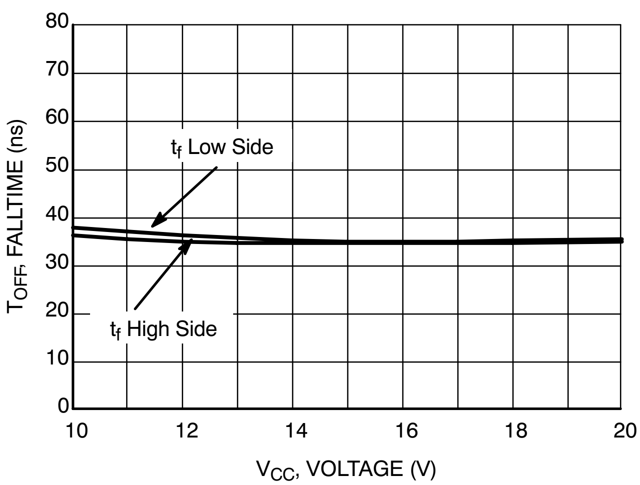


Figure 16. Turn OFF Falltime vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

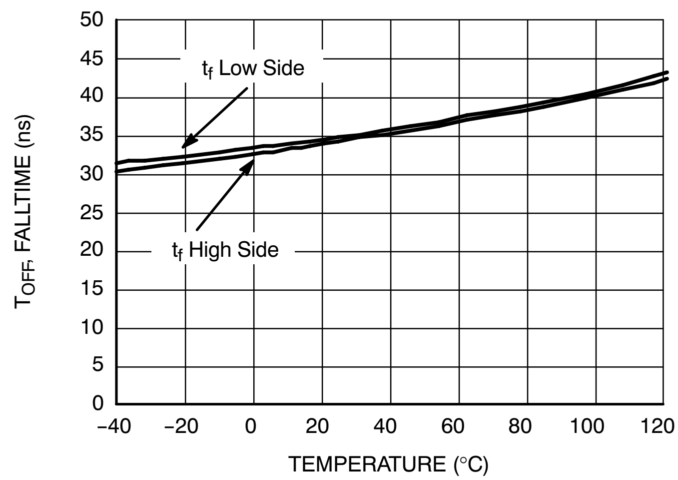


Figure 17. Turn OFF Falltime vs. Temperature

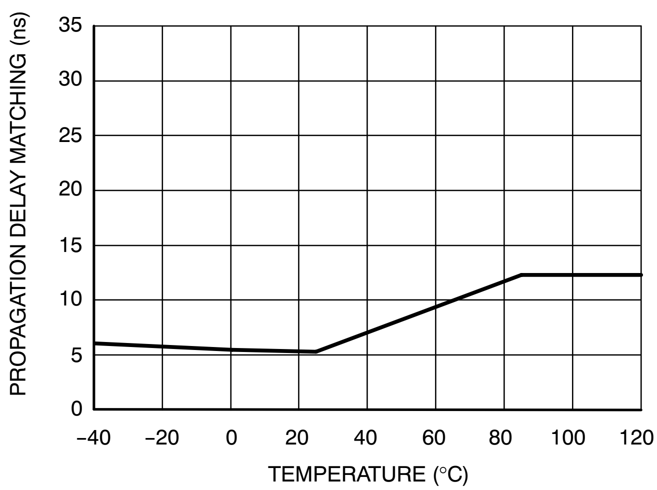


Figure 18. Propagation Delay Matching Between High Side and Low Side Driver vs. Temperature

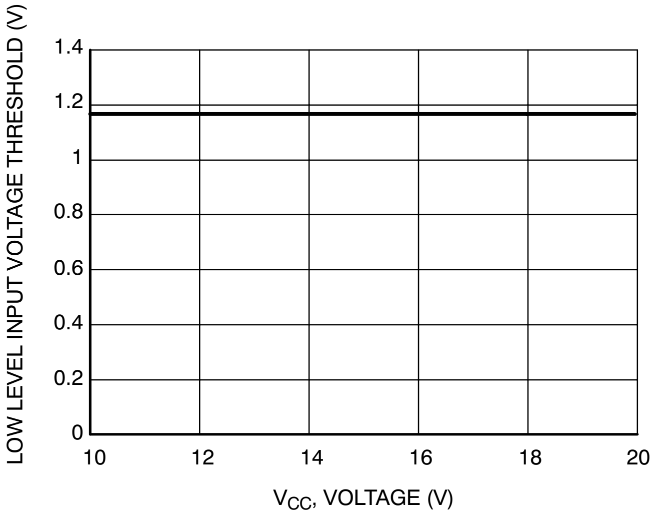


Figure 19. Low Level Input Voltage Threshold vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

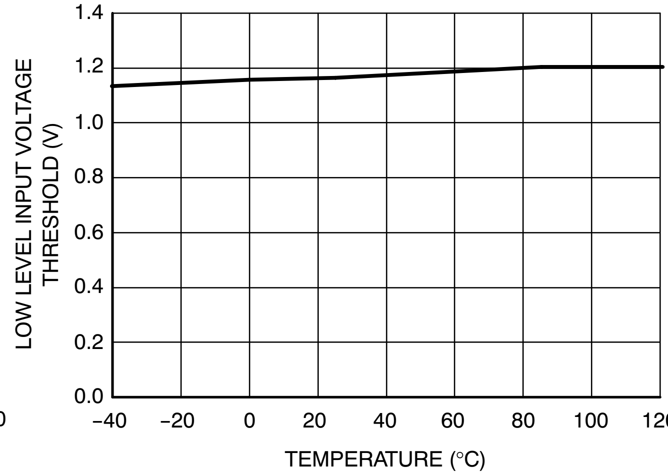


Figure 20. Low Level Input Voltage Threshold vs. Temperature

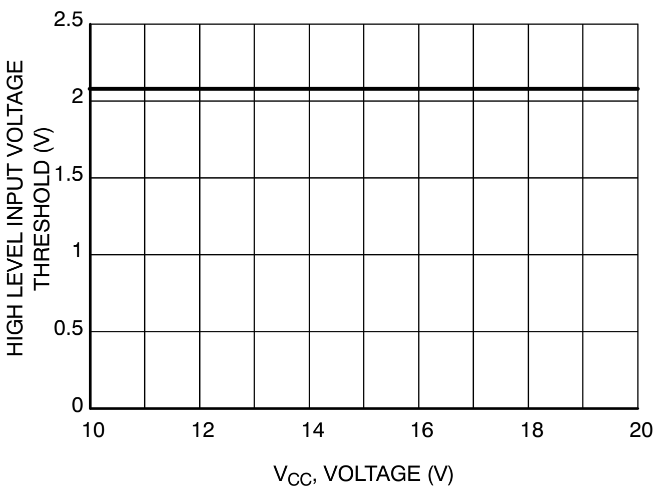


Figure 21. High Level Input Voltage Threshold vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

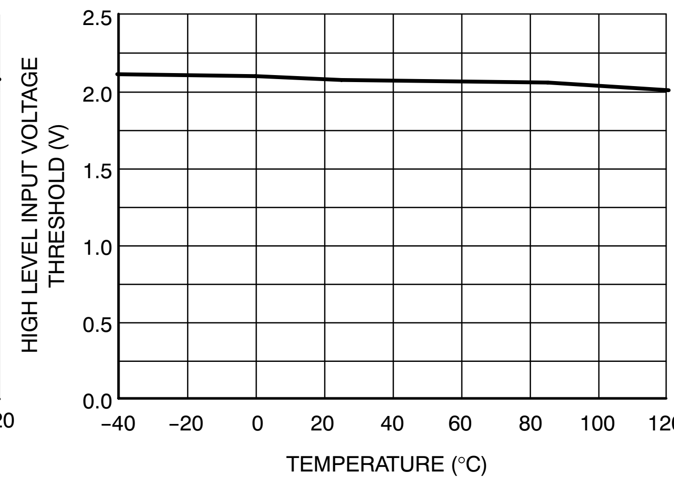


Figure 22. High Level Input Voltage Threshold vs. Temperature

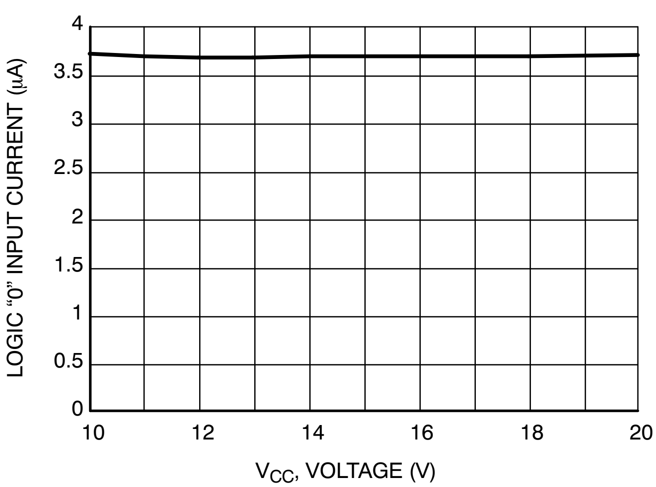


Figure 23. Logic “0” Input Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

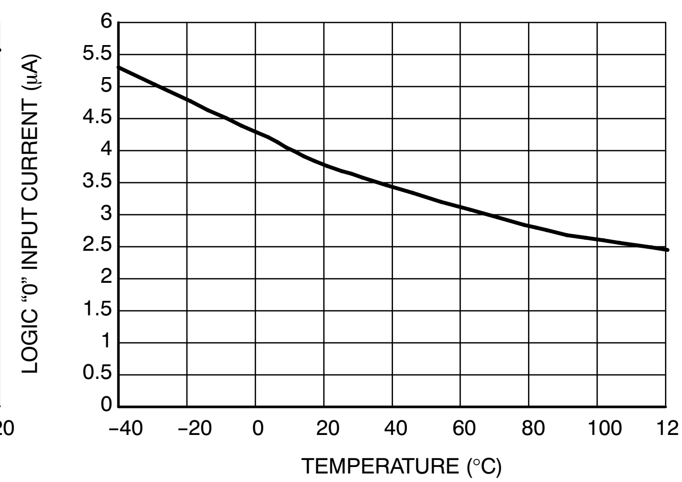


Figure 24. Logic “0” Input Current vs. Temperature

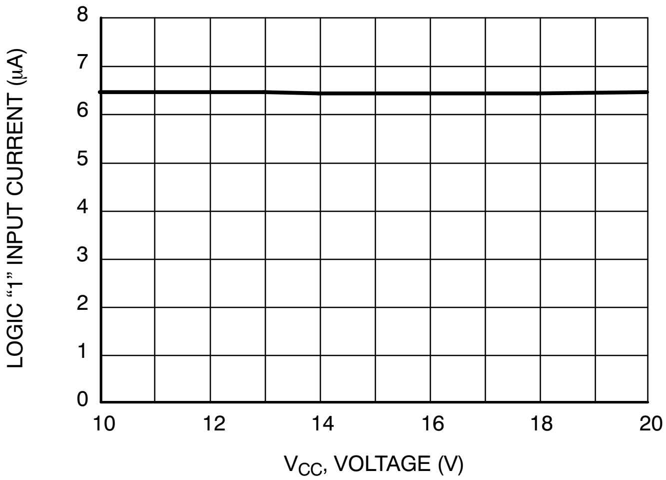


Figure 25. Logic “1” Input Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

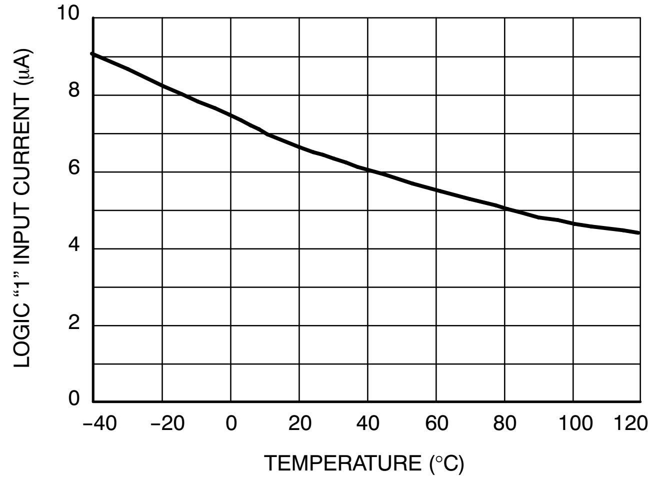


Figure 26. Logic “1” Input Current vs. Temperature

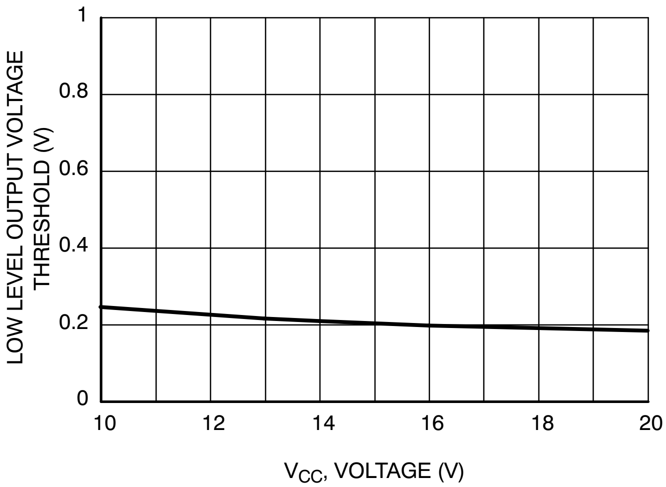


Figure 27. Low Level Output Voltage vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

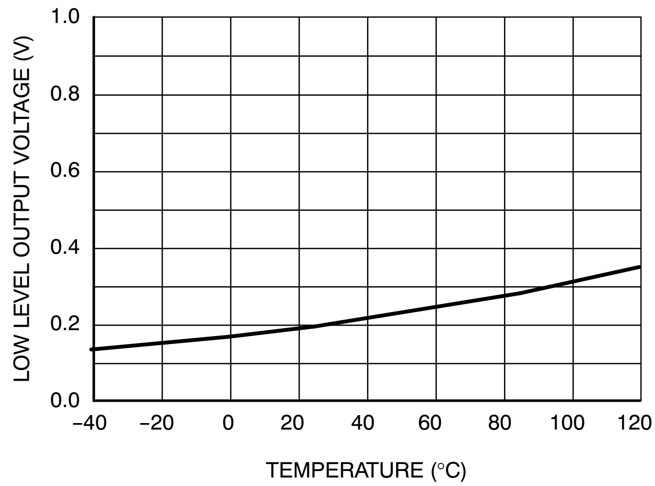


Figure 28. Low Level Output Voltage vs. Temperature

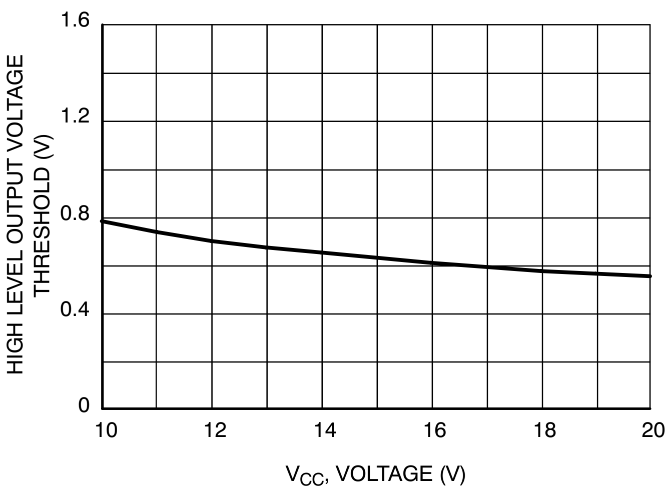


Figure 29. High Level Output Voltage vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

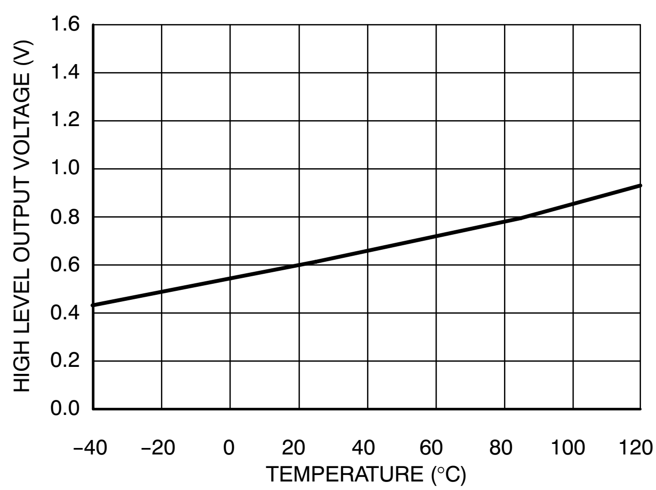


Figure 30. High Level Output Voltage vs. Temperature

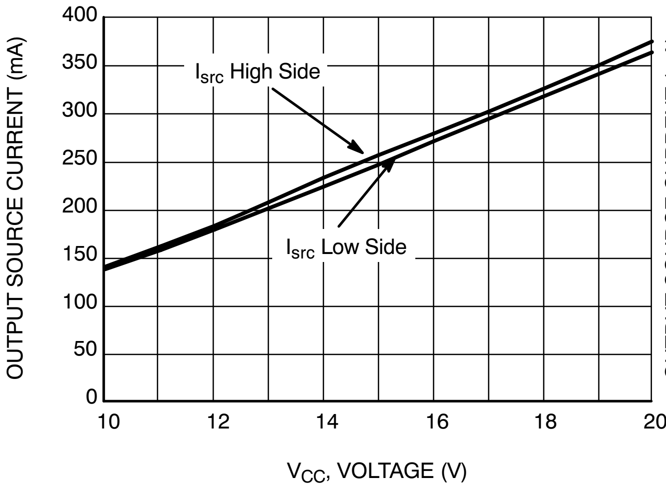


Figure 31. Output Source Current vs. Supply Voltage (V_{CC} = V_{BOOT})

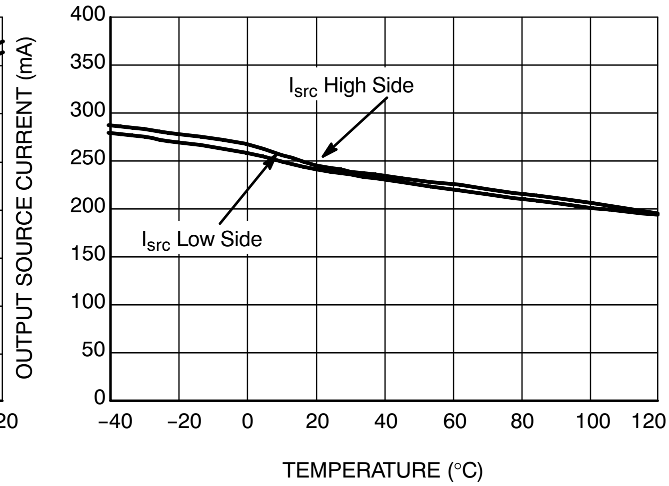


Figure 32. Output Source Current vs. Temperature

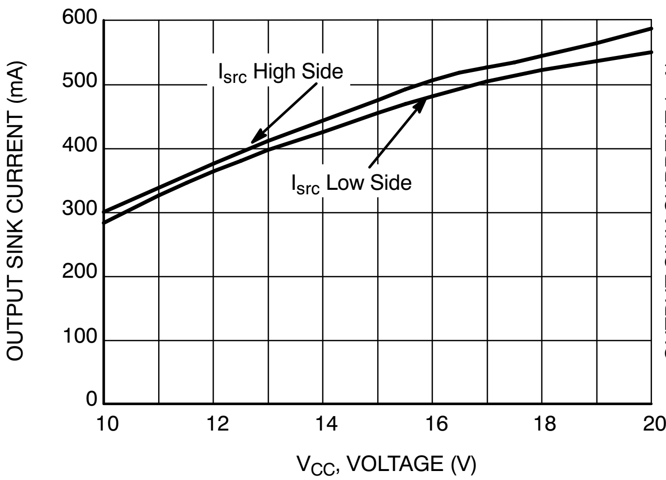


Figure 33. Output Sink Current vs. Supply Voltage (V_{CC} = V_{BOOT})

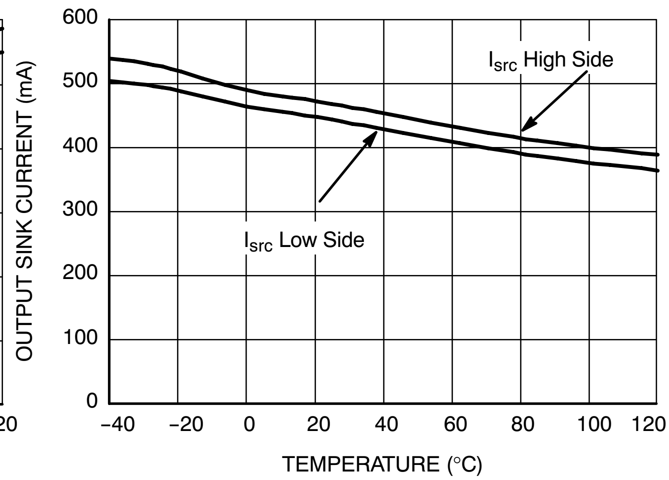


Figure 34. Output Sink Current vs. Temperature

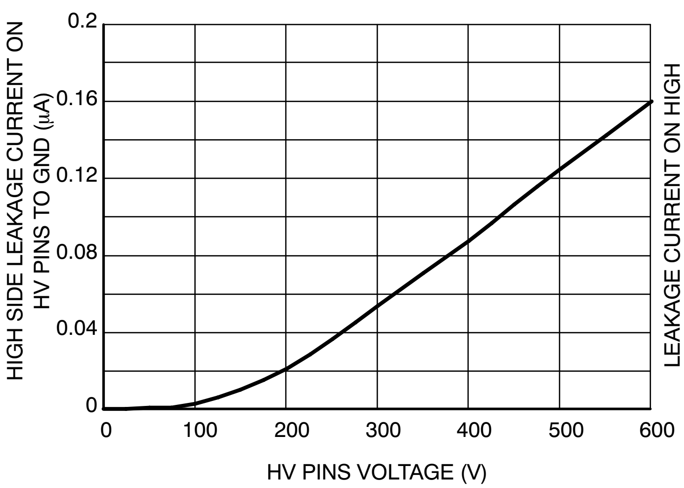


Figure 35. Leakage Current on High Voltage Pins (600 V) to Ground vs. V_{BRIDGE} Voltage (V_{BRIGDE} = V_{BOOT} = VDRV_HI)

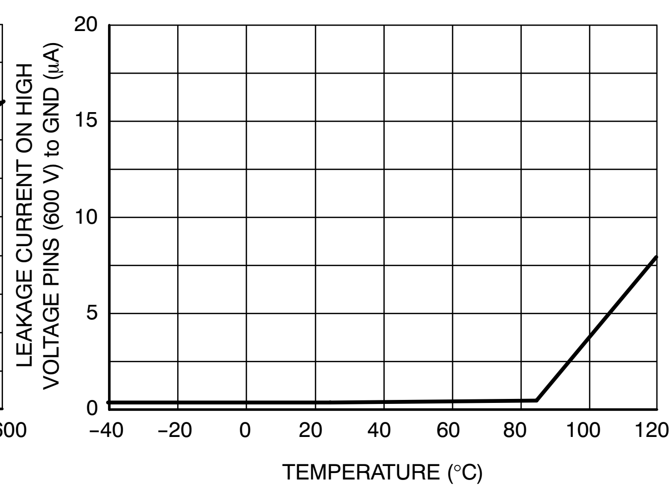


Figure 36. Leakage Current on High Voltage Pins (600 V) to Ground vs. Temperature (VBRIDGE = V_{BOOT} = VDRV_HI = 600 V)

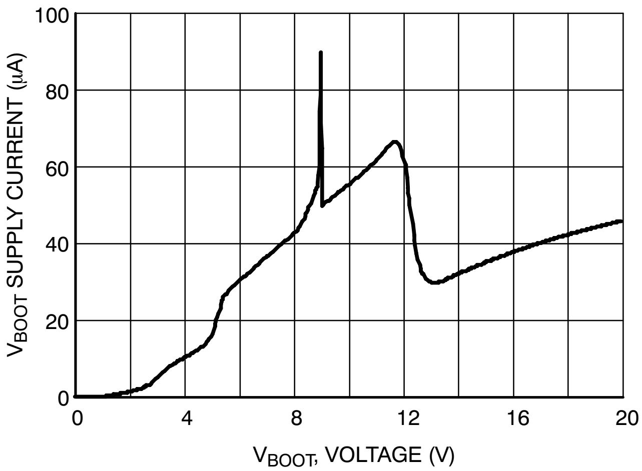


Figure 37. V_{BOOT} Supply Current vs. Bootstrap Supply Voltage

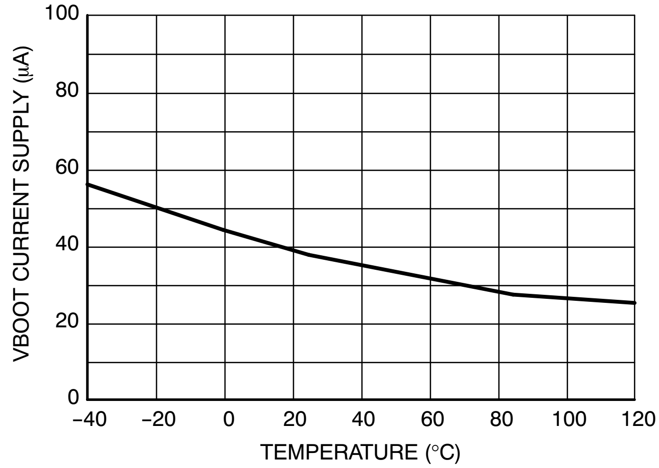


Figure 38. V_{BOOT} Supply Current vs. Temperature

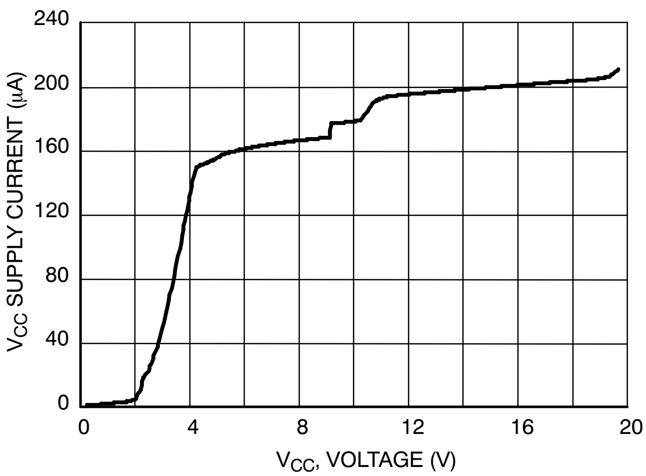


Figure 39. V_{CC} Supply Current vs. V_{CC} Supply Voltage

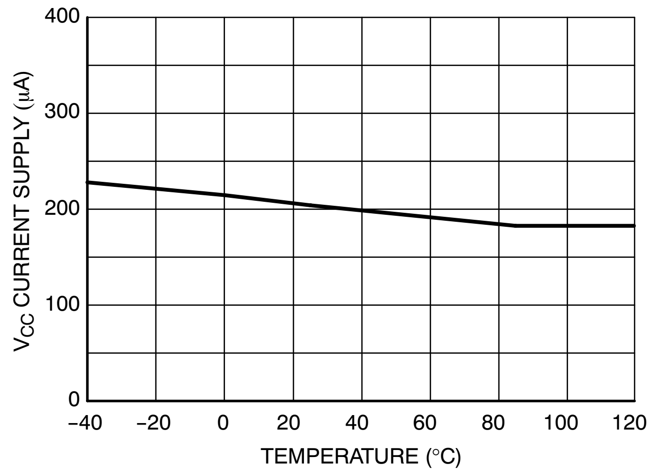


Figure 40. V_{CC} Supply Current vs. Temperature

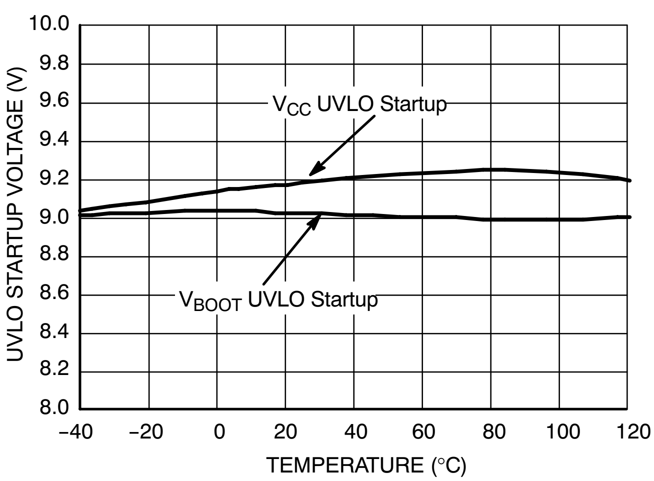


Figure 41. UVLO Startup Voltage vs. Temperature

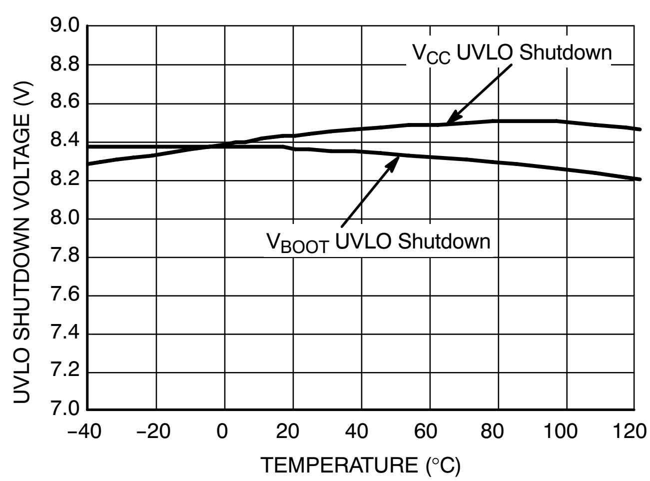


Figure 42. UVLO Shutdown Voltage vs. Temperature

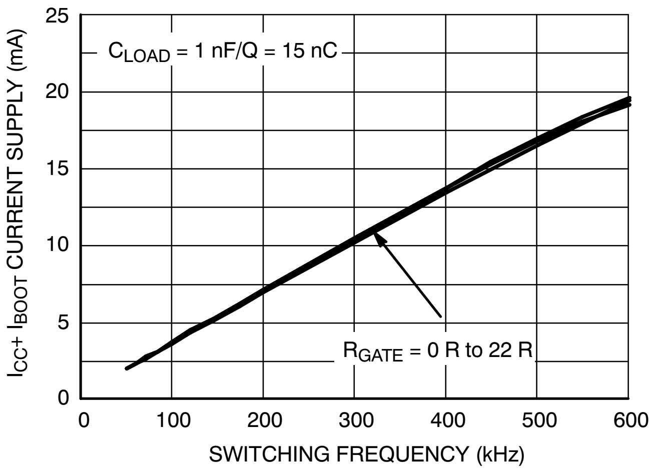


Figure 43. I_{CC1} Consumption vs. Switching Frequency with 15 nC Load on Each Driver @ V_{CC} = 15 V

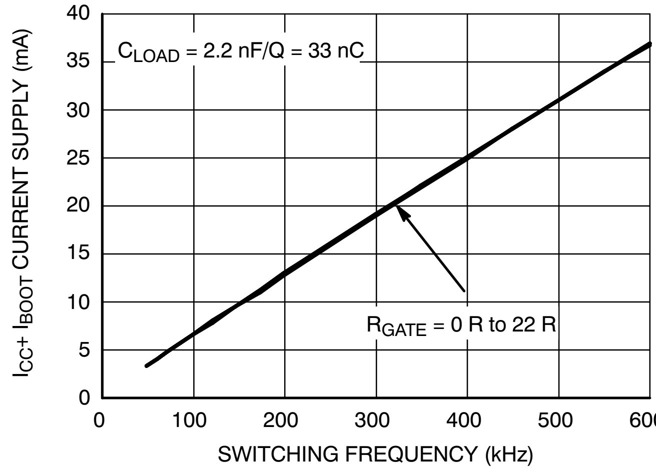


Figure 44. I_{CC1} Consumption vs. Switching Frequency with 33 nC Load on Each Driver @ V_{CC} = 15 V

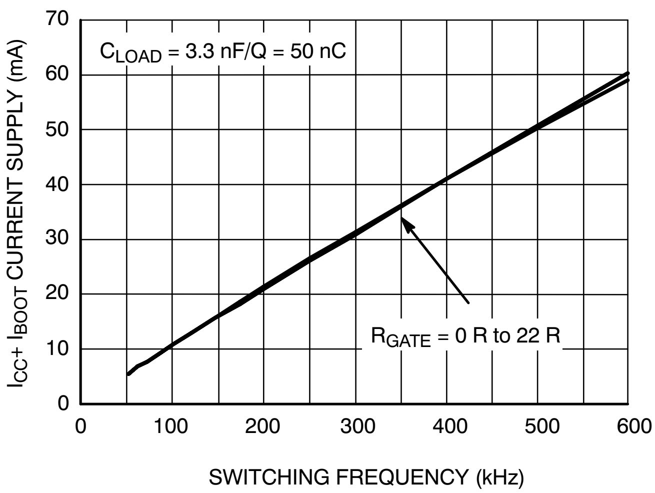


Figure 45. I_{CC1} Consumption vs. Switching Frequency with 50 nC Load on Each Driver @ V_{CC} = 15 V

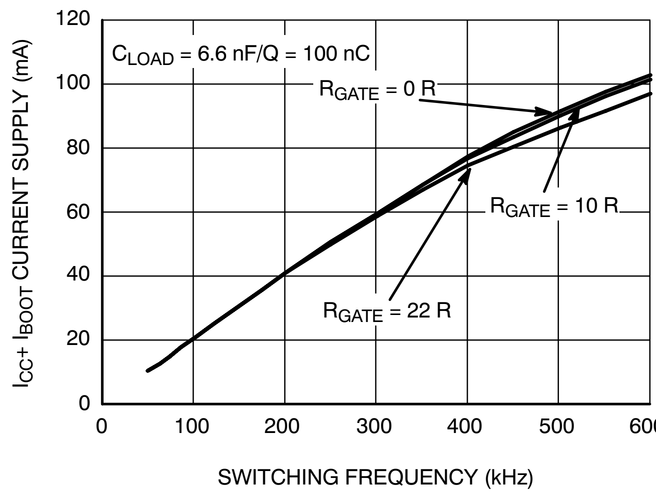
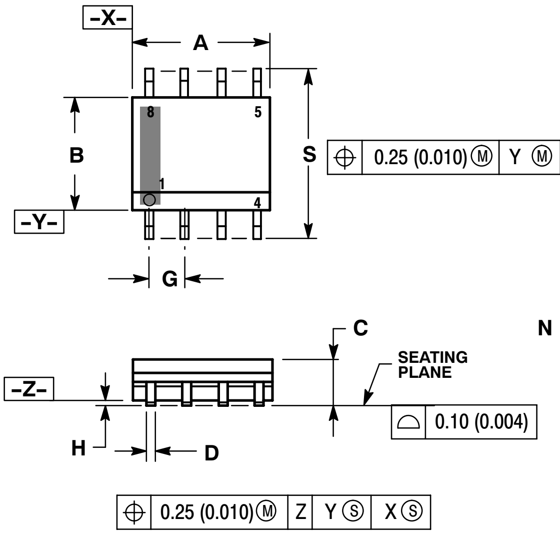
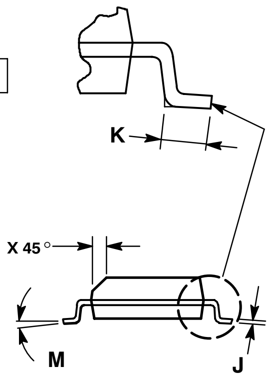


Figure 46. I_{CC1} Consumption vs. Switching Frequency with 100 nC Load on Each Driver @ V_{CC} = 15 V

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AH

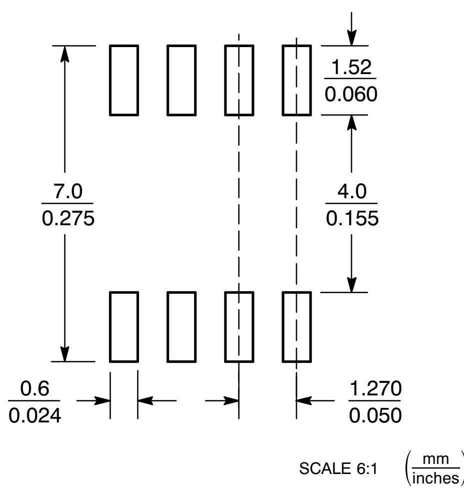




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

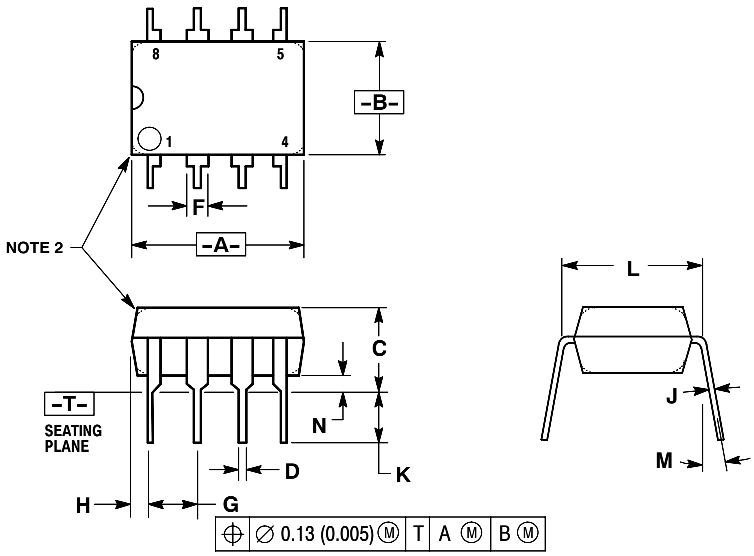
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

8 LEAD PDIP
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

The product described herein is covered by U.S. patents: 6,097,075; 7,176,723; 6,362,067. There may be some other patents pending.

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