Data Sheet | February 14, 2008 | FN7490.4

Micropower, Single Supply, Rail-to-Rail Input-Output Instrumentation Amplifiers

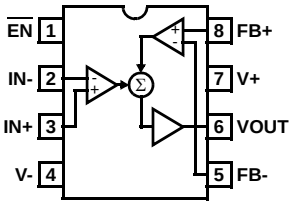
The EL8170 and EL8173 are micropower instrumentation amplifiers optimized for single supply operation over the +2.4V to +5.5V range. Inputs and outputs can operate rail-to-rail. As with all instrumentation amplifiers, a pair of inputs provide very high common-mode rejection and are completely independent from a pair of feedback terminals. The feedback terminals allow zero input to be translated to any output offset, including ground. A feedback divider controls the overall gain of the amplifier.

The EL8170 is compensated for a gain of 100 or more, and the EL8173 is compensated for a gain of 10 or more. The EL8170 and EL8173 have bipolar input devices for best offset and 1/f noise performance.

The amplifiers can be operated from one lithium cell or two Ni-Cd batteries. The EL8170 and EL8173 input range includes ground to slightly above positive rail. The output stage swings to ground and positive supply (no pull-up or pull-down resistors are needed).

Pinout

EL8170, EL8173
(8 LD SOIC)
TOP VIEW



Features

- 95µA maximum supply current
- Maximum offset voltage
  - 200µV (EL8170)
  - 1000µV (EL8173)
- Maximum 3nA input bias current
- 396kHz -3dB bandwidth (G = 10)
- 192kHz -3dB bandwidth (G = 100)
- Single supply operation
  - Input voltage range is rail-to-rail
  - Output swings rail-to-rail
- Pb-free (RoHS compliant)

Applications

- Battery- or solar-powered systems
- Strain gauges
- Current monitors
- Thermocouple amplifiers

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE	PKG. DWG. #
EL8170FSZ*	8170FSZ	8 Ld SOIC	MDP0027
EL8173FSZ*	8173FSZ	8 Ld SOIC	MDP0027

*Add “-T7” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage, V_+ 5.5V
Differential Input Current 5mA
Differential Input Voltage (EL8170) 0.5V
Differential Input Voltage (EL8173) 1.0V
V_{EN} . . . . . .0.5V to V+ + 0.5V
ESD Rating
Human Body Model 3kV

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Ld SOIC Package	110

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature . . . . . .-40°C to +125°C
Storage Temperature . . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = +5V, V_- = GND, VCM = 1/2V_+, V_{EN} = V-, R_L = Open, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

PARAMETER	DESCRIPTION	CONDITIONS		MIN (Note 2)	TYP	MAX (Note 2)	UNIT
DC SPECIFICATIONS							
V_{OS}	Input Offset Voltage	EL8170		-200 **-300**	±50	200 **300**	µV
		EL8173		-1000 **-1500**	±200	1000 **1500**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	EL8170			0.24		µV/°C
		EL8173			2.5		µV/°C
I_{OS}	Input Offset Current between IN+, and IN- and between FB+ and FB-			-2 **-3**	±0.2	2 **3**	nA
I_B	Input Bias Current (IN+, IN-, FB+, and FB- terminals)			-3 **-4**	±0.7	3 **4**	nA
V_{IN}	Input Voltage Range	Guaranteed by CMRR test		0		5	V
CMRR	Common Mode Rejection Ratio	EL8170	V_{CM} = 0V to +5V	90 **85**	114		dB
		EL8173		85 **80**	106		dB
PSRR	Power Supply Rejection Ratio	EL8170	V_+ = +2.4V to +5V	85 **80**	106		dB
		EL8173		75 **70**	90		dB
E_G	Gain Error	EL8170	R_L = 100kΩ to +2.5V	-1.5 **2**	+0.35	1.5 **2**	%
		EL8173		-0.4 **-0.8**	+0.1	0.4 **0.8**	%
V_{OUT}	Maximum Voltage Swing	Output low, R_L = 100kΩ to +2.5V			4	**10**	mV
		Output low, R_L = 1kΩ to +2.5V			0.13	0.2 **0.25**	V
		Output high, R_L = 100kΩ to +2.5V		4.985 **4.980**	4.996		V
		Output high, R_L = 1kΩ to +2.5V		**4.75**	4.887		V
$I_{S,EN}$	Supply Current, Enabled			45 **38**	65	95 **110**	µA

Electrical Specifications V_+ = +5V, V_- = GND, VCM = 1/2V_+, V_{EN} = V-, R_L = Open, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS		MIN (Note 2)	TYP	MAX (Note 2)	UNIT
$I_{S,DIS}$	Supply Current, Disabled	$\overline{EN}$ = V_+		1.8 **1.3**	2.6	4 **5**	µA
V_{ENH}	$\overline{EN}$ Pin for Shut-down			2			V
V_{ENL}	$\overline{EN}$ Pin for Power-on					0.8	V
V_{SUPPLY}	Supply Operating Range	V+ to V- (Note 3)		2.4		5.5	V
I_{O+}	Output Source Current into 10Ω to V_+/2	V_+ = +5V		23 **19**	32		mA
		V_+ = +2.4V		6 **4.5**	8		mA
I_{O-}	Output Sink Current into 10Ω to V_+/2	V_+ = +5V		19 **15**	26		mA
		V_+ = +2.4V		5 **4**	7		mA
AC SPECIFICATIONS							
-3dB BW	-3dB Bandwidth	EL8170	Gain = 100		192		kHz
			Gain = 200		93		kHz
			Gain = 500		30		kHz
			Gain = 1000		13		kHz
		EL8173	Gain = 10		396		kHz
			Gain = 20		221		kHz
			Gain = 50		69		kHz
			Gain = 100		30		kHz
e_N	Input Noise Voltage	EL8170	f = 0.1Hz to 10Hz		3.5		$µV_{P-P}$
		EL8173			3.6		$µV_{P-P}$
	Input Noise Voltage Density	EL8170	f_0 = 1kHz		58		nV/√Hz
		EL8173			220		nV/√Hz
i_N	Input Noise Current Density	EL8170, f_0 = 1kHz			0.38		pA/√Hz
		EL8173, f_0 = 1kHz			0.8		pA/√Hz
CMRR @ 60Hz	Input Common Mode Rejection Ratio	EL8170	V_{CM} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		100		dB
		EL8173			84		dB
PSRR+ @ 120Hz	Power Supply Rejection Ratio (V_+)	EL8170	V_+, V_- = ±2.5V, V_{SOURCE} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		98		dB
		EL8173			78		dB
PSRR- @ 120Hz	Power Supply Rejection Ratio (V_-)	EL8170	V_+, V_- = ±2.5V, V_{SOURCE} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		106		dB
		EL8173			82		dB
TRANSIENT RESPONSE							
SR	Slew Rate	R_L = 1kΩ to GND		0.4 **0.35**	0.55	0.7 **0.7**	V/µs

NOTES:

2. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.
3. V_{SUPPLY} = +5.25V max when V_{ENL} = +V (device in disable state).

Typical Performance Curves

V+ = +5V, V- = 0V, V_{CM} = +2.5V, V_{EN} = V-, R_L = Open, unless otherwise specified.

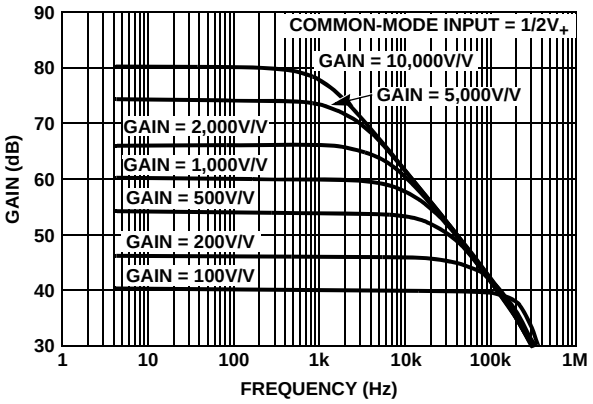


FIGURE 1. EL8170 FREQUENCY RESPONSE vs CLOSED LOOP GAIN

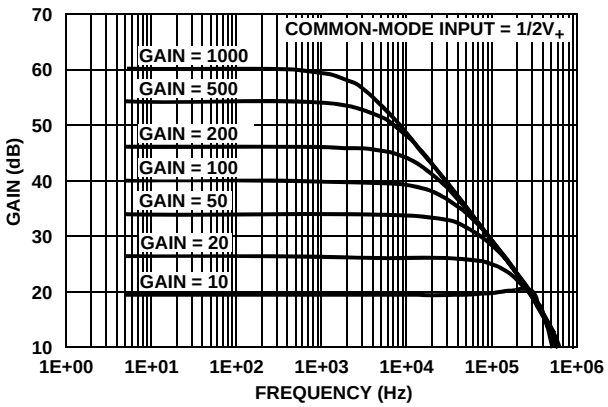


FIGURE 2. EL8173 FREQUENCY RESPONSE vs CLOSED LOOP GAIN

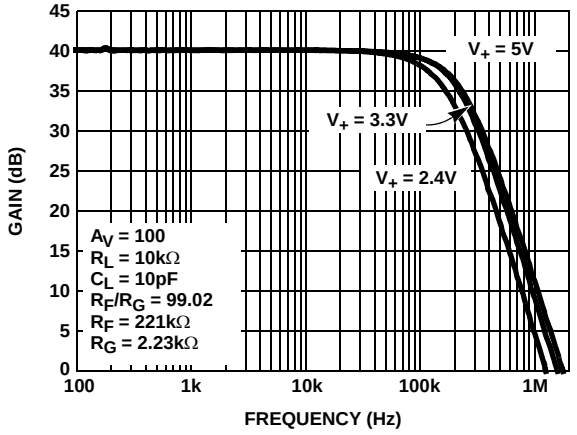


FIGURE 3. EL8170 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

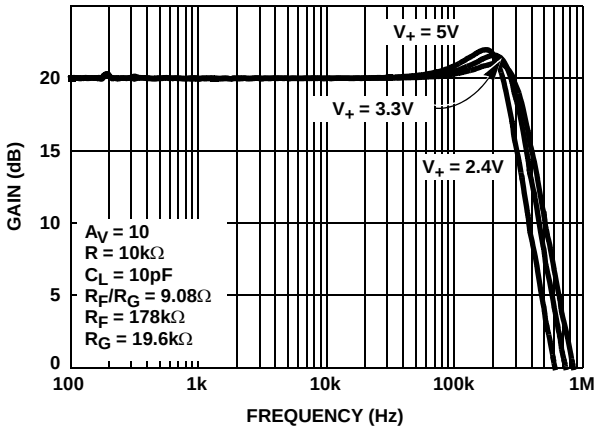


FIGURE 4. EL8173 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

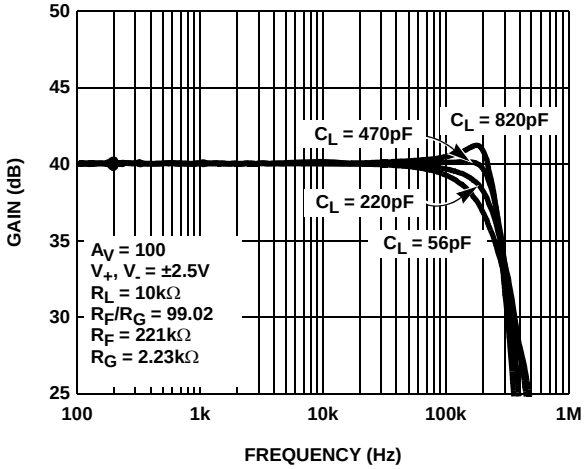


FIGURE 5. EL8170 FREQUENCY RESPONSE vs C_{LOAD}

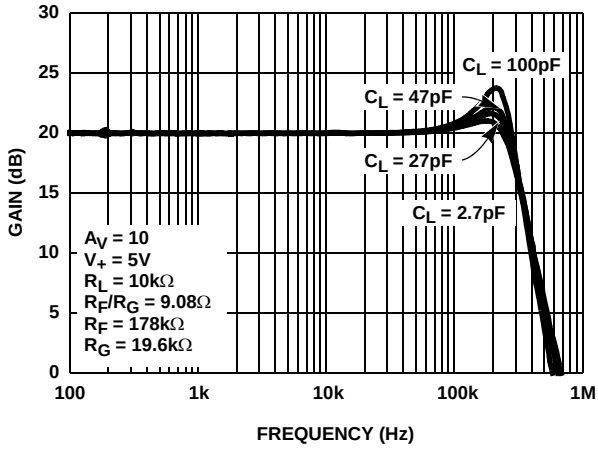


FIGURE 6. EL8173 FREQUENCY RESPONSE vs C_{LOAD}

Typical Performance Curves V+ = +5V, V- = 0V, V_{CM} = +2.5V, V_{EN} = V-, R_L = Open, unless otherwise specified. **(Continued)**

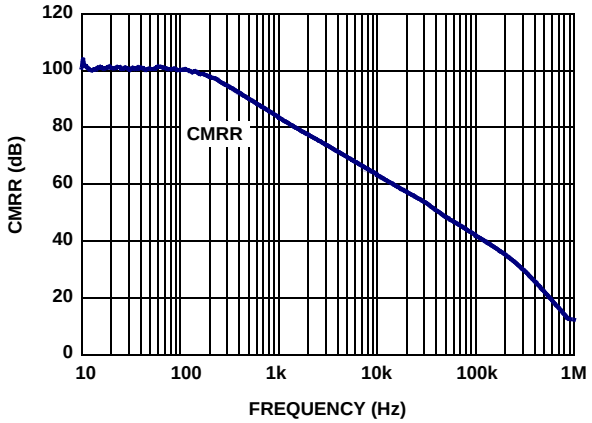


FIGURE 7. EL8170 CMRR vs FREQUENCY

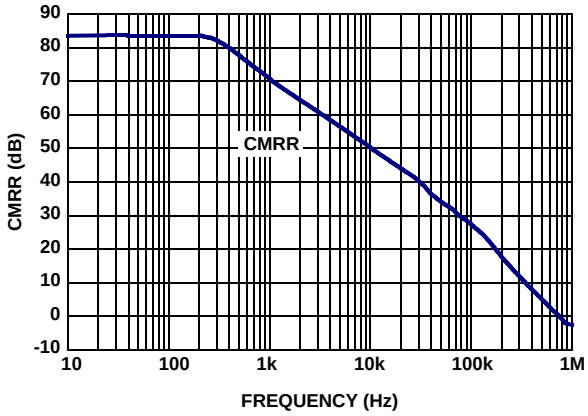


FIGURE 8. EL8173 CMRR vs FREQUENCY

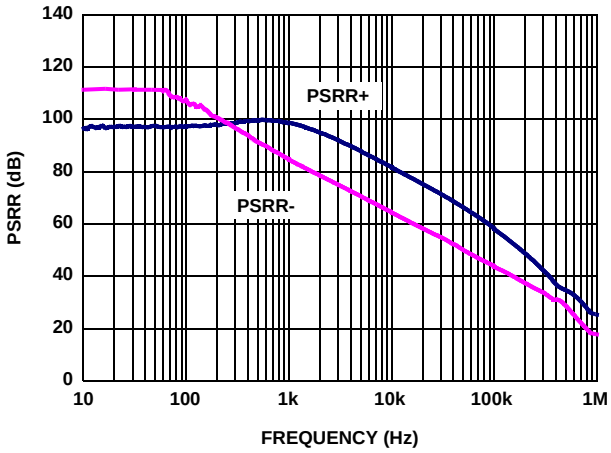


FIGURE 9. EL8170 PSRR vs FREQUENCY

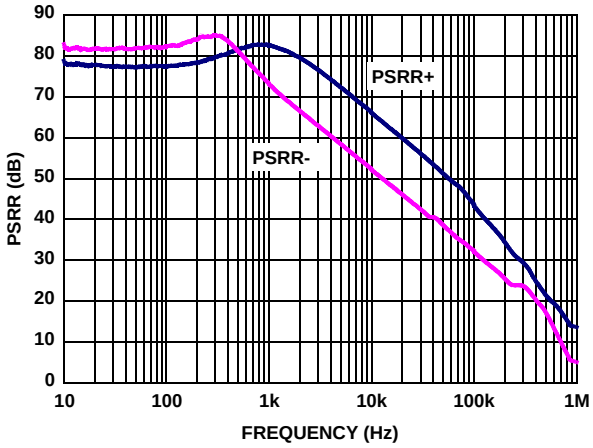


FIGURE 10. EL8173 PSRR vs FREQUENCY

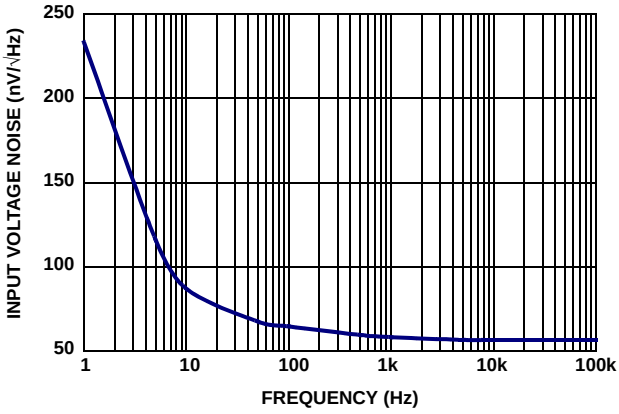


FIGURE 11. EL8170 VOLTAGE NOISE DENSITY

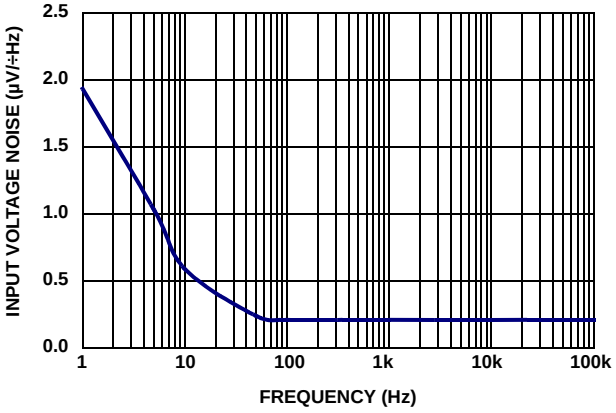


FIGURE 12. EL8173 VOLTAGE NOISE DENSITY

Typical Performance Curves $V+ = +5V, V- = 0V, V_{CM} = +2.5V, V_{EN} = V-, R_L$ = Open, unless otherwise specified. **(Continued)**

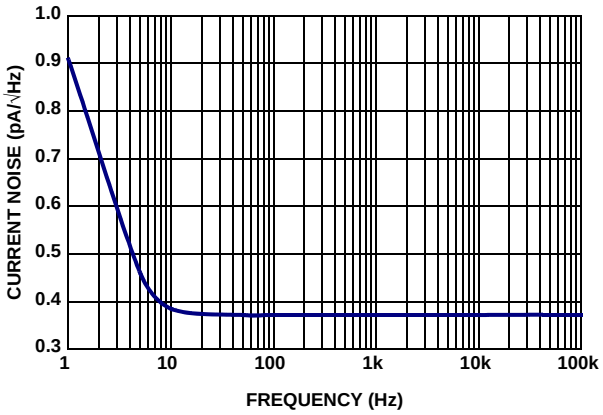


FIGURE 13. EL8170 CURRENT NOISE DENSITY

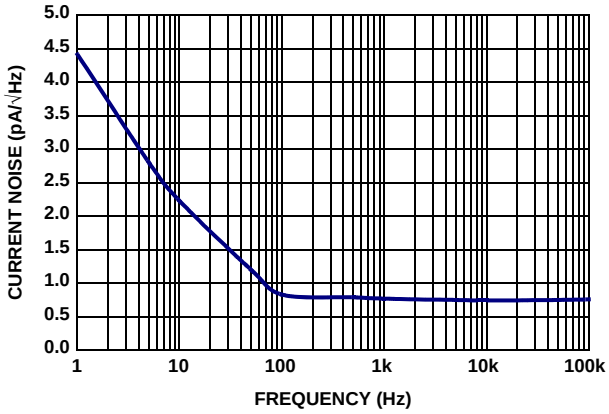


FIGURE 14. EL8173 CURRENT NOISE DENSITY

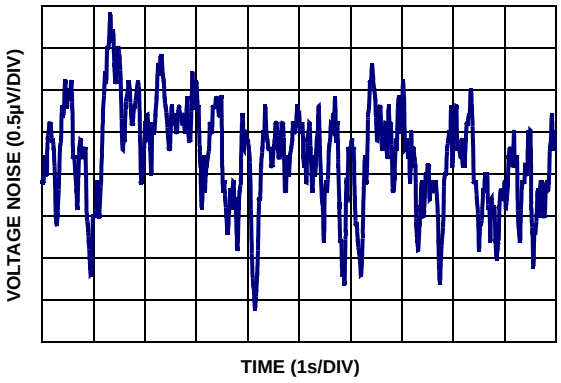


FIGURE 15. EL8170 0.1Hz TO 10Hz INPUT VOLTAGE NOISE (GAIN = 100)

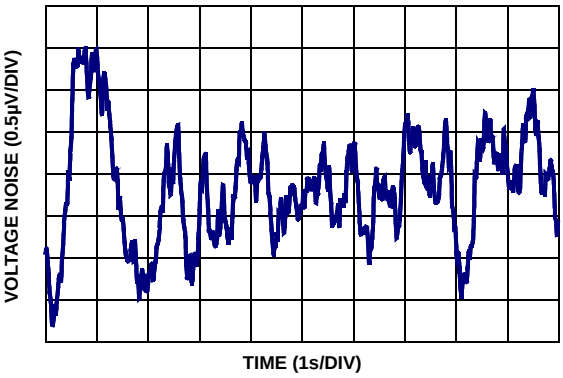


FIGURE 16. EL8173 0.1Hz TO 10Hz INPUT VOLTAGE NOISE (GAIN = 10)

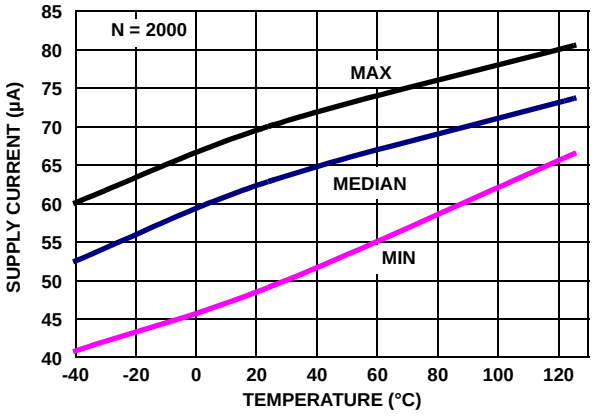


FIGURE 17. EL8170 SUPPLY CURRENT ENABLED vs TEMPERATURE, V_+, V_- = ±2.5V, V_{IN} = 0V

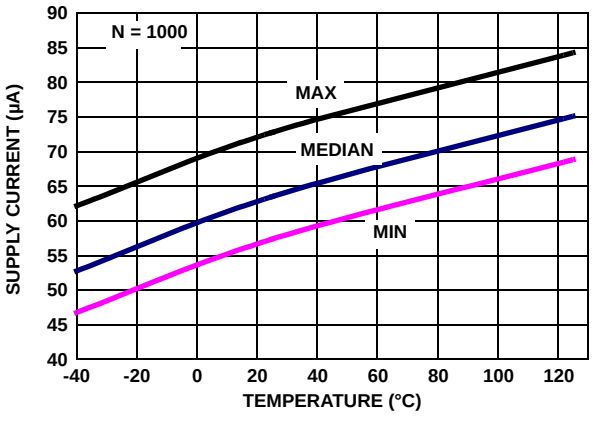


FIGURE 18. EL8173 SUPPLY CURRENT ENABLED vs TEMPERATURE, V_+, V_- = ±2.5V, V_{IN} = 0V

Typical Performance Curves V+ = +5V, V- = 0V, V_{CM} = +2.5V, V_{EN} = V-, R_L = Open, unless otherwise specified. **(Continued)**

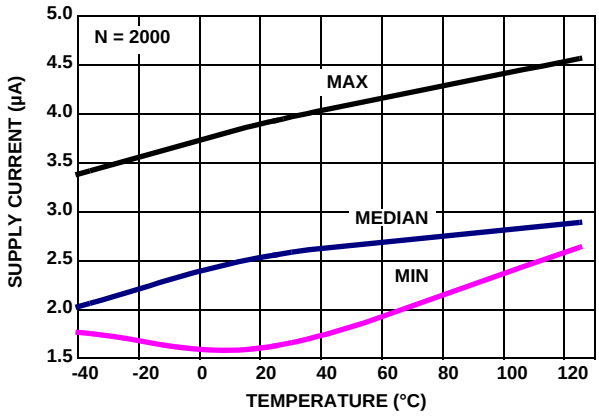


FIGURE 19. EL8170 SUPPLY CURRENT DISABLED vs TEMPERATURE, V_+, V_- = ±2.5V, V_{EN} = V_+, V_{IN} = 0V

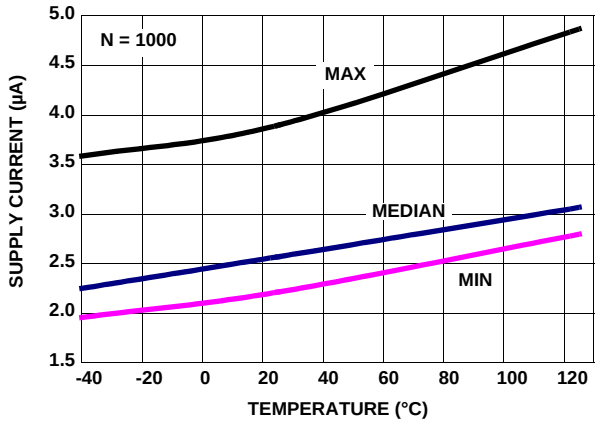


FIGURE 20. EL8173 SUPPLY CURRENT DISABLED vs TEMPERATURE, V_+, V_- = ±2.5V, V_{EN} = V_+, V_{IN} = 0V

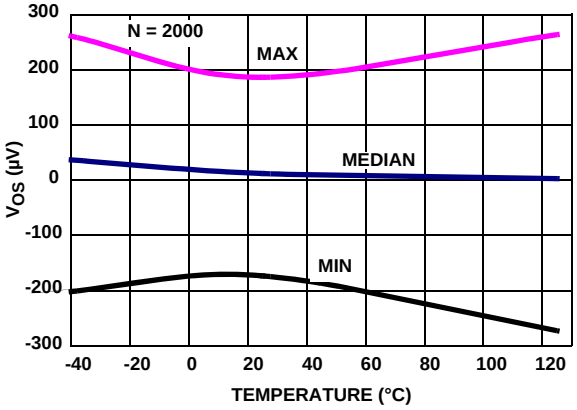


FIGURE 21. EL8170 V_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V, V_{IN} = 0V

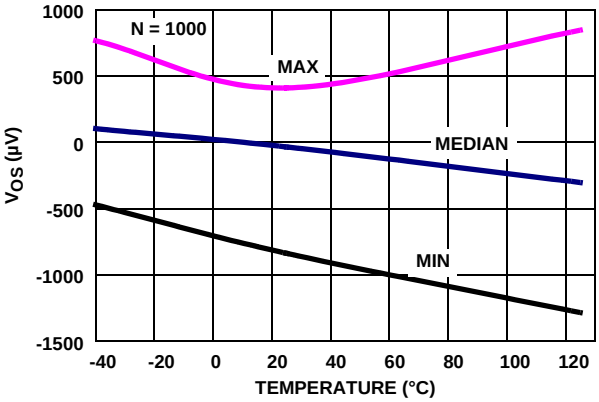


FIGURE 22. EL8173 V_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V, V_{IN} = 0V

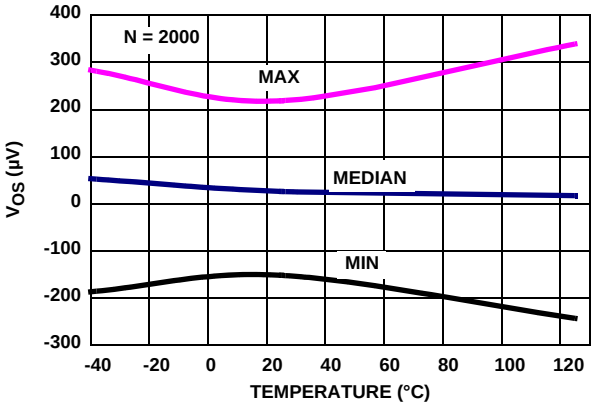


FIGURE 23. EL8170 V_{OS} vs TEMPERATURE, V_+, V_- = ±1.2V, V_{IN} = 0V

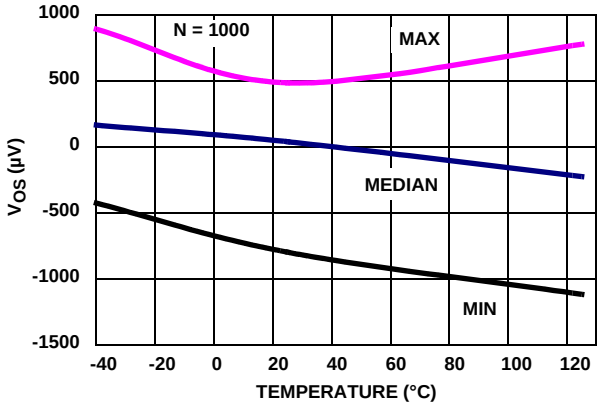


FIGURE 24. EL8173 V_{OS} vs TEMPERATURE, V_+, V_- = ±1.2V, V_{IN} = 0V

Typical Performance Curves $V+ = +5V, V- = 0V, V_{CM} = +2.5V, V_{EN} = V-, R_L$ = Open, unless otherwise specified. **(Continued)**

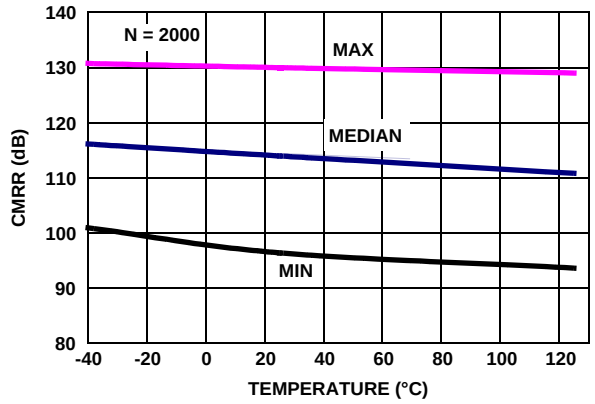


FIGURE 25. EL8170 CMRR vs TEMPERATURE, V_{CM} = +2.5V TO -2.5V, V_+, V_- = ±2.5V

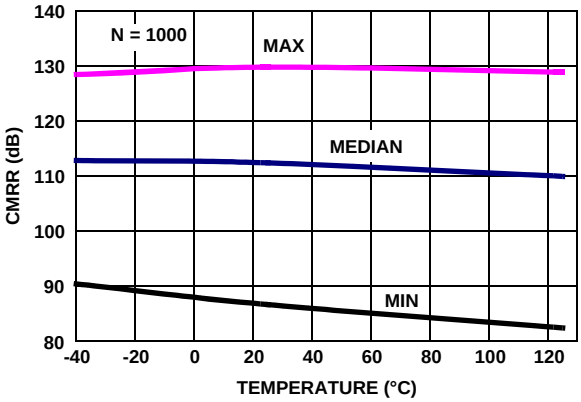


FIGURE 26. EL8173 CMRR vs TEMPERATURE, V_{CM} = +2.5V TO -2.5V, V_+, V_- = ±2.5V

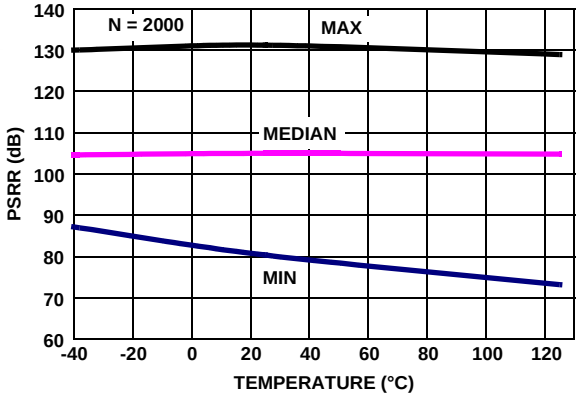


FIGURE 27. EL8170 PSRR vs TEMPERATURE, V_+, V_- = ±1.2V TO ±2.5V

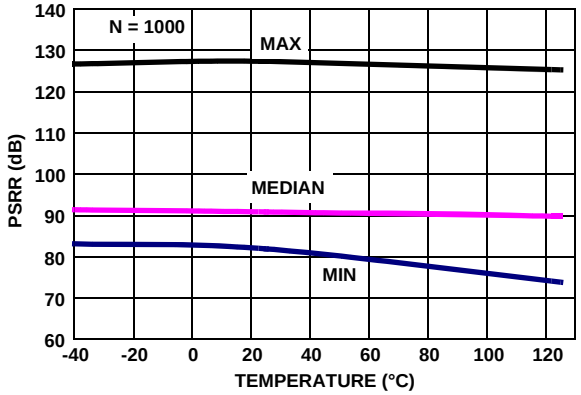


FIGURE 28. EL8173 PSRR vs TEMPERATURE, V_+, V_- = ±1.2V TO ±2.5V

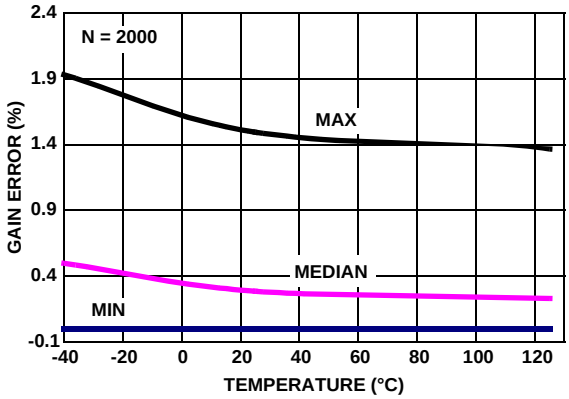


FIGURE 29. EL8170 %GAIN ERROR vs TEMPERATURE, R_L = 100k

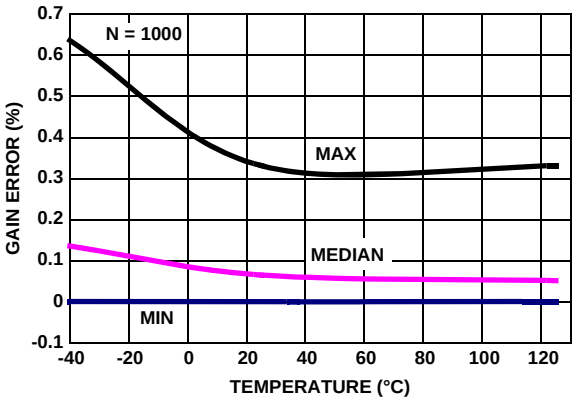


FIGURE 30. EL8173 %GAIN ERROR vs TEMPERATURE, R_L = 100k

Typical Performance Curves V+ = +5V, V- = 0V, V_{CM} = +2.5V, V_{EN} = V-, R_L = Open, unless otherwise specified. **(Continued)**

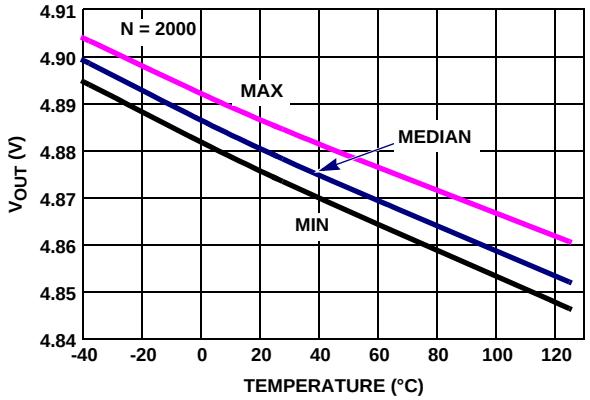


FIGURE 31. EL8170 V_{OUT} HIGH vs TEMPERATURE, R_L = 1k, V_+, V_- = ±2.5V

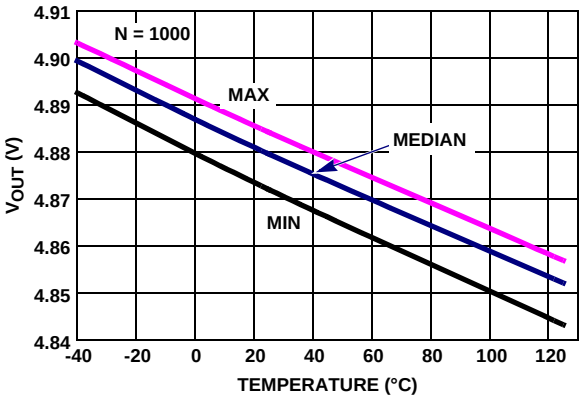


FIGURE 32. EL8173 V_{OUT} HIGH vs TEMPERATURE, R_L = 1k, V_+, V_- = ±2.5V

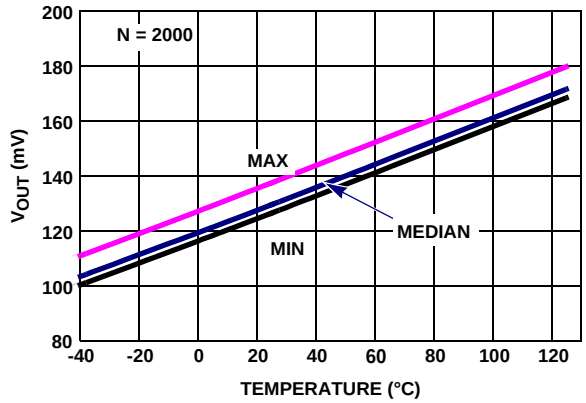


FIGURE 33. EL8170 V_{OUT} LOW vs TEMPERATURE, R_L = 1k, V_+, V_- = ±2.5V

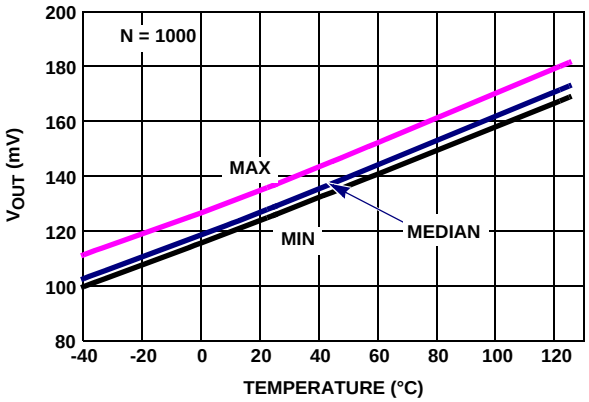


FIGURE 34. EL8173 V_{OUT} LOW vs TEMPERATURE, R_L = 1k, V_+, V_- = ±2.5V

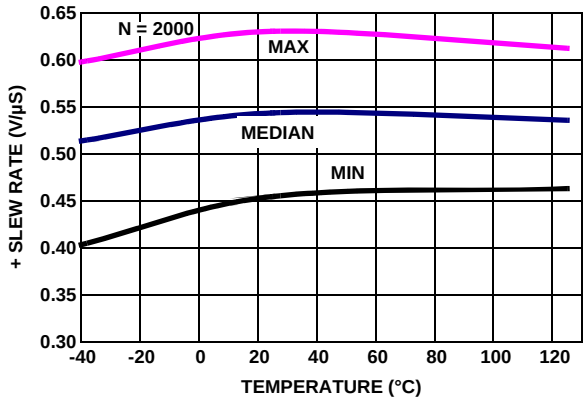


FIGURE 35. EL8170 + SLEW RATE vs TEMPERATURE, INPUT ±0.015V @ GAIN + 100

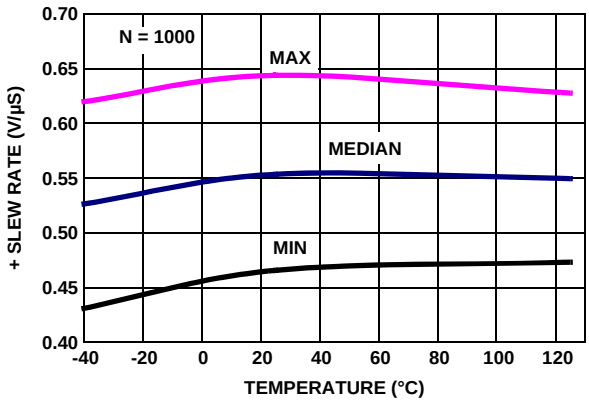


FIGURE 36. EL8173 + SLEW RATE vs TEMPERATURE, INPUT ±0.015V @ GAIN + 100

Typical Performance Curves $V+ = +5V, V- = 0V, V_{CM} = +2.5V, V_{EN} = V-, R_L$ = Open, unless otherwise specified. **(Continued)**

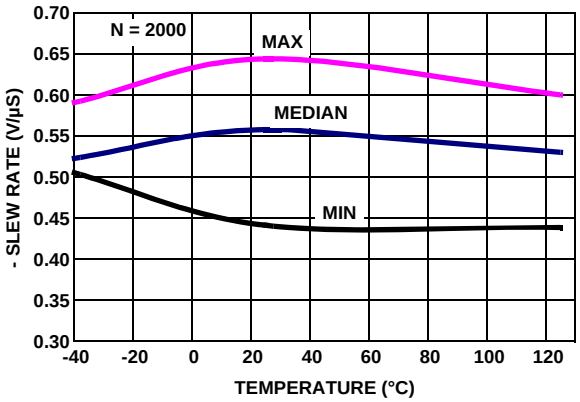


FIGURE 37. EL8170 - SLEW RATE vs TEMPERATURE, INPUT ±0.015V @ GAIN + 100

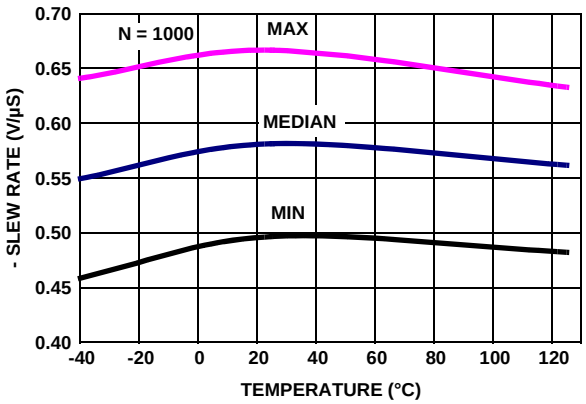
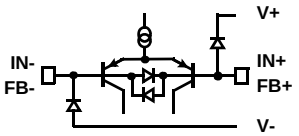


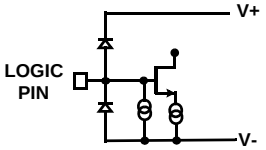
FIGURE 38. EL8173 - SLEW RATE vs TEMPERATURE, INPUT ±0.015V @ GAIN + 100

Pin Descriptions

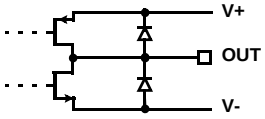
EL8170, EL8173	PIN NAME	EQUIVALENT CIRCUIT	PIN FUNCTION
1	$\overline{EN}$	Circuit 2	Active LOW logic pins. When pulled above 2V, the corresponding channel turns off and OUT is high impedance. A channel is enabled when pulled below 0.8V. Built-in pull downs define each $\overline{EN}$ pin LOW when left floating.
2	IN-	Circuit 1A, Circuit 1B	High impedance input terminals. EL8170 input circuit is shown in Circuit 1A, and the EL8173 input circuit is shown in Circuit 1B. EL8173: to avoid offset drift, it is recommended that the terminals are not overdriven beyond 1V and the input current must never exceed 5mA.
3	IN+	Circuit 1A, Circuit 1B	
4	V-	Circuit 4	Negative supply terminal.
5	FB-	Circuit 1A, Circuit 1B	High impedance feedback terminals. EL8170 input circuit is shown in Circuit 1A, and the EL8173 input circuit is shown in Circuit 1B. EL8173: to avoid offset drift, it is recommended that the terminals are not overdriven beyond 1V and the input current must never exceed 5mA.
8	FB+	Circuit 1A, Circuit 1B	
7	V+	Circuit 4	Positive supply terminal.
6	VOUT	Circuit 3	Output Voltage.



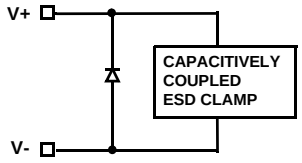
CIRCUIT 1A



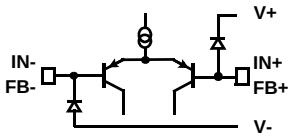
CIRCUIT 2



CIRCUIT 3



CIRCUIT 4



CIRCUIT 1B

Description of Operation and Applications Information

Product Description

The EL8170 and EL8173 are micropower instrumentation amplifiers (in-amps) which deliver rail-to-rail input amplification and rail-to-rail output swing on a single +2.4V to +5.5V supply. The EL8170 and EL8173 also deliver excellent DC and AC specifications while consuming only 65µA typical supply current. Because the EL8170 and EL8173 provide an independent pair of feedback terminals to set the gain and to adjust output level, these in-amps achieve high common-mode rejection ratio regardless of the tolerance of the gain setting resistors. The EL8173 is internally compensated for a minimum closed loop gain of 10 or greater, well suited for moderate to high gains. For higher gains, the EL8170 is internally compensated for a minimum gain of 100. An $\overline{EN}$ pin is used to reduce power consumption, typically 2.6µA, while the instrumentation amplifier is disabled.

Input Protection

All input and feedback terminals of the EL8170 and EL8173 have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode drop beyond the supply rails. The inverting inputs and FB- inputs have ESD diodes to the V-rail, and the non-inverting inputs and FB+ terminals have ESD diodes to the V+ rail. The EL8170 has additional back-to-back diodes across the input terminals and also across the feedback terminals. If overdriving the inputs is necessary, the external input current must never exceed 5mA. On the other hand, the EL8173 has no clamps to limit the differential voltage on the input terminals allowing higher differential input voltages at lower gain applications. It is recommended however, that the input terminals of the EL8173 are not overdriven beyond 1V to avoid offset drift. An external series resistor may be used as an external protection to limit excessive external voltage and current from damaging the inputs.

Input Stage and Input Voltage Range

The input terminals (IN+ and IN-) of the EL8170 and EL8173 are single differential pair bipolar PNP devices aided by an Input Range Enhancement Circuit to increase the headroom of operation of the common-mode input voltage. The feedback terminals (FB+ and FB-) also have a similar topology. As a result, the input common-mode voltage range of both the EL8170 and EL8173 is rail-to-rail. These in-amps are able to handle input voltages that are at or slightly beyond the supply and ground making these in-amps well suited for single +5V or +3.3V low voltage supply systems. There is no need to move the common-mode input of the in-amps to achieve symmetrical input voltage.

Input Bias Cancellation, Input Bias Compensation

Both EL8170 and EL8173 feature an Input Bias Cancellation/Compensation Circuit for both the input and feedback terminals (IN+, IN-, FB+ and FB-), achieving a low input bias current all throughout the input common-mode range and the operating temperature range. While the PNP bipolar input stages are biased with an adequate amount of biasing current for speed and increased noise performance, the Input Bias Cancellation/Compensation Circuit sinks most of the base current of the input transistor leaving a small portion as input bias current, typically 500pA. In addition, the Input Bias Cancellation/Compensation Circuit maintains a smooth and flat behavior of input bias current over the common mode range and over the operating temperature range. The Input Bias Cancellation, Input Bias Compensation Circuit operates from input voltages of 10mV above the negative supply to input voltages slightly above the positive supply. See “Average Input Bias Current vs Common-Mode Input Voltage” in the “Typical Performance Curves” beginning on page 4.

Output Stage and Output Voltage Range

A pair of complementary MOSFET devices drives the output V_{OUT} to within a few millivolts of the supply rails. At a 100kΩ load, the PMOS sources current and pulls the output up to 4mV below the positive supply, while the NMOS sinks current and pulls the output down to 4mV above the negative supply, or ground in the case of a single supply operation. The current sinking and sourcing capability of the EL8170 and EL8173 are internally limited to 26mA.

Gain Setting

V_{IN}, the potential difference across IN+ and IN-, is replicated (less the input offset voltage) across FB+ and FB-. The objective of the EL8170 and EL8173 in-amp is to maintain the differential voltage across FB+ and FB- equal to IN+ and IN-; (FB+ - FB-) = (IN+ - IN-). Consequently, the transfer function can be derived. The gain of the EL8170 and EL8173 is set by two external resistors, the feedback resistor R_F, and the gain resistor R_G.

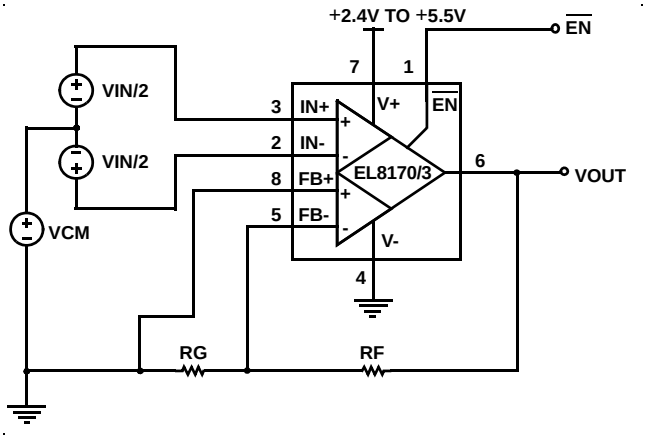


FIGURE 39. GAIN IS SET BY TWO EXTERNAL RESISTORS, R_F AND R_G

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right)V_{IN} \quad \text{(EQ. 1)}$$

In Figure 39, the FB+ pin and one end of resistor R_G are connected to GND. With this configuration, Equation 1 is only true for a positive swing in VIN; negative input swings will be ignored and the output will be at ground.

Reference Connection

Unlike a three op amp instrumentation amplifier, a finite series resistance seen at the REF terminal does not degrade the EL8170 and EL8173's high CMRR performance, eliminating the need for an additional external buffer amplifier. The circuit shown in Figure 40 uses the FB+ pin as a REF terminal to center or to adjust the output. Because the FB+ pin is a high impedance input, an economical resistor divider can be used to set the voltage at the REF terminal. The reference voltage error due to the input bias current is minimized by keeping the values of the voltage divider resistors, R_1 and R_2, as low as possible. Any voltage applied to the REF terminal will shift V_{OUT} by VREF times the closed loop gain, which is set by resistors R_F and R_G according to Equation 2. Note that any noise or unwanted signals on the reference supply will be amplified at the output according to Equation 2.

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right)(V_{IN}) + \left(1 + \frac{R_F}{R_G}\right)(V_{REF}) \quad \text{(EQ. 2)}$$

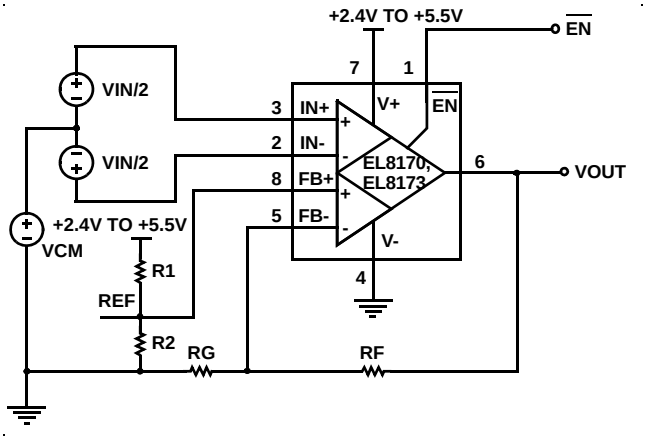


FIGURE 40. GAIN SETTING AND REFERENCE CONNECTION

The FB+ pin can also be connected to the other end of resistor, R_G. See Figure 41. Keeping the basic concept that the EL8170 and EL8173 in-amps maintain constant differential voltage across the input terminals and feedback terminals (IN+ - IN- = FB+ - FB-), the transfer function of Figure 41 can be derived (Equation 3). Note that the V_{REF} gain term is eliminated, and susceptibility to external noise is reduced.

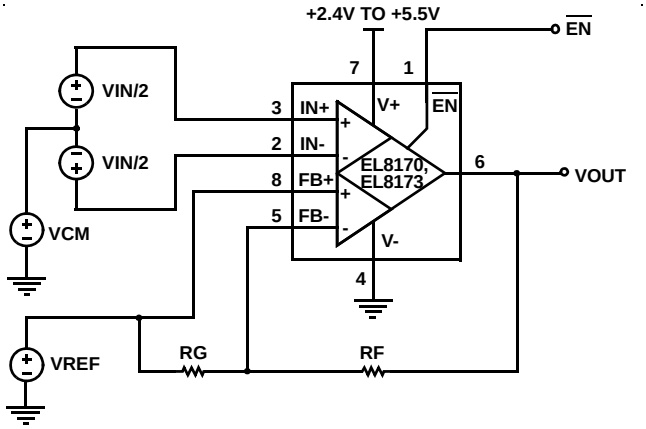


FIGURE 41. REFERENCE CONNECTION WITH AN AVAILABLE V_{REF}

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right)(V_{IN}) + (V_{REF}) \quad \text{(EQ. 3)}$$

External Resistor Mismatches

Because of the independent pair of feedback terminals provided by the EL8170 and EL8173, the CMRR is not degraded by any resistor mismatches. Hence, unlike a three op amp and especially a two op amp in-amp, the EL8170 and EL8173 reduce the cost of external components by allowing the use of 1% or more tolerance resistors without sacrificing CMRR performance. The EL8170 and EL8173 CMRR is maintained regardless of the tolerance of the resistors used.

Gain Error and Accuracy

The EL8173 has a Gain Error, E_G, of 0.2% typical. The EL8170 has an E_G of 0.3% typical. The gain error indicated in the “Electrical Specifications” table on page 2 is the inherent gain error of the EL8170 and EL8173 and does not include the gain error contributed by the resistors. There is an additional gain error due to the tolerance of the resistors used. The resulting non-ideal transfer function effectively becomes Equation 4:

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right) \times [1 - (E_{RG} + E_{RF} + E_G)] \times V_{IN} \quad \text{(EQ. 4)}$$

Where:

E_{RG}= Tolerance of R_G

E_{RF}= Tolerance of R_F

E_G= Gain Error of the EL8170 or EL8173

The term [1 - (E_{RG} + E_{RF} + E_G)] is the deviation from the theoretical gain. Thus, (E_{RG} + E_{RF} + E_G) is the total gain error. For example, if 1% resistors are used for the EL8170, the total gain error would be:

$$\begin{aligned} &= \pm(E_{RG} + E_{RF} + E_G(\text{typical})) \\ &= \pm(0.01 + 0.01 + 0.003) \\ &= \pm 2.3\% \end{aligned} \quad \text{(EQ. 5)}$$

Disable/Power-Down

The EL8170 and EL8173 can be powered down reducing the supply current to typically 2.9µA. When disabled, the output is in a high impedance state. The active low $\overline{EN}$ bar pin has an internal pull-down and hence can be left floating and the in-amp enabled by default. When the $\overline{EN}$ bar is connected to an external logic, the in-amp will power down when the $\overline{EN}$ bar is pulled above 2V, and will power-on when the $\overline{EN}$ bar is pulled below 0.8V.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 6:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 6)}$$

where:

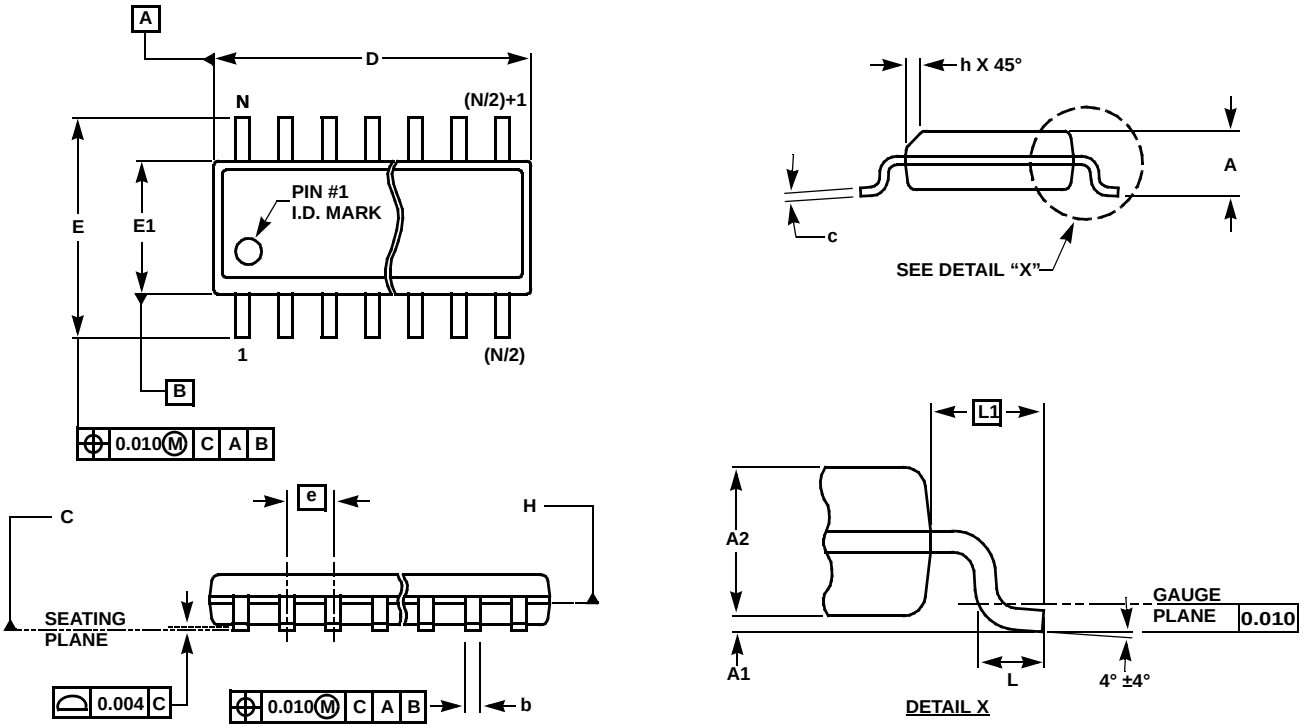
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as shown in Equation 7:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 7)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage (Magnitude of V_+ and V_-)
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994