TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM2323

20V P-Channel MOSFET

SOT-23

Pin Definition:
1. Gate
2. Source
3. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
-20	39 @ V_{GS} = -4.5V	-4.7
	52 @ V_{GS} = -2.5V	-4.1
	68 @ V_{GS} = -1.8V	-2.0

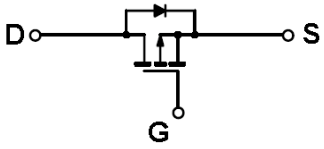
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



P-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM2323CX RF	SOT-23	3Kpcs / 7" Reel

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current, V_{GS} @4.5V.		I_D	-4.7	A
Pulsed Drain Current, V_{GS} @4.5V		I_{DM}	-20	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	-1.0	A
Maximum Power Dissipation	Ta = 25°C	P_D	1.25	W
	Ta = 70°C		0.8	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JC}$	75	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	250	°C/W

Notes:

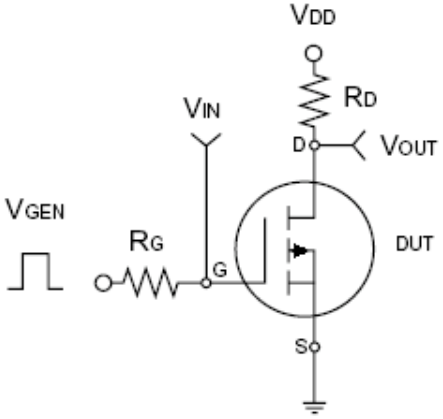
a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

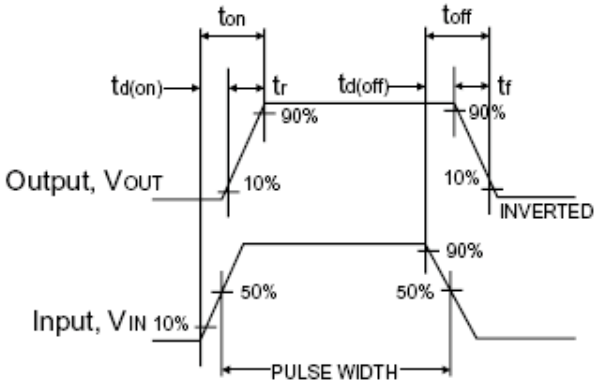
Electrical Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = - 250uA	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = - 250uA	$V_{GS(TH)}$	-0.4	--	-1.0	V
Zero Gate Voltage Drain Current	V_{DS} = -16V, V_{GS} = 0V	I_{DSS}	--	--	-1.0	uA
Gate Body Leakage	V_{GS} = ±8V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
On-State Drain Current	V_{DS} ≤-5V, V_{GS} = -4.5V	$I_{D(ON)}$	-20	--	--	A
Drain-Source On-State Resistance	V_{GS} = -4.5V, I_D = -4.7A	$R_{DS(ON)}$	--	31	39	mΩ
	V_{GS} = -2.5V, I_D = -4.1A		--	41	52	
	V_{GS} = -1.8V, I_D = -2.0A		--	54	68	
Forward Transconductance	V_{DS} = - 5V, I_D = - 4.7A	g_{fs}	--	16	--	S
Diode Forward Voltage	I_S = - 1.0A, V_{GS} = 0V	V_{SD}	--	- 0.7	-1.2	V
Dynamic[b]						
Total Gate Charge	V_{DS} = -10V, I_D = -4.7A, V_{GS} = -4.5V	Q_g	--	12.5	19	nC
Gate-Source Charge		Q_{gs}	--	1.7	--	
Gate-Drain Charge		Q_{gd}	--	3.3	--	
Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1020	--	pF
Output Capacitance		C_{oss}	--	191	--	
Reverse Transfer Capacitance		C_{rss}	--	140	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = -10V, R_L = 10Ω, I_D = -1A, V_{GEN} = -4.5V, R_G = 6Ω	$t_{d(on)}$	--	25	40	nS
Turn-On Rise Time		t_r	--	43	65	
Turn-Off Delay Time		$t_{d(off)}$	--	71	110	
Turn-Off Fall Time		t_f	--	48	75	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



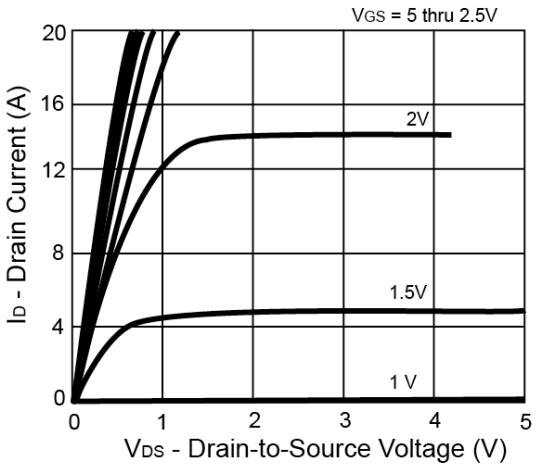
Switching Test Circuit



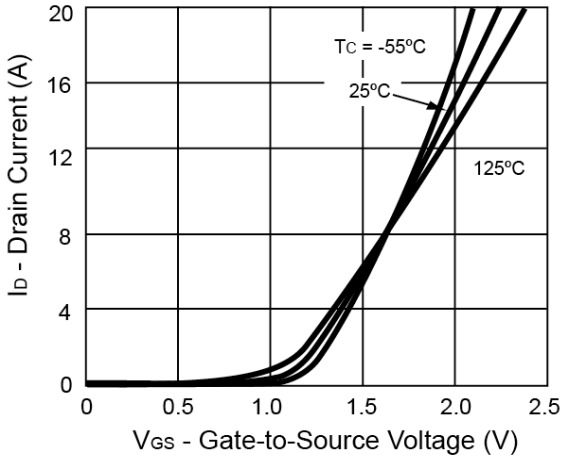
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

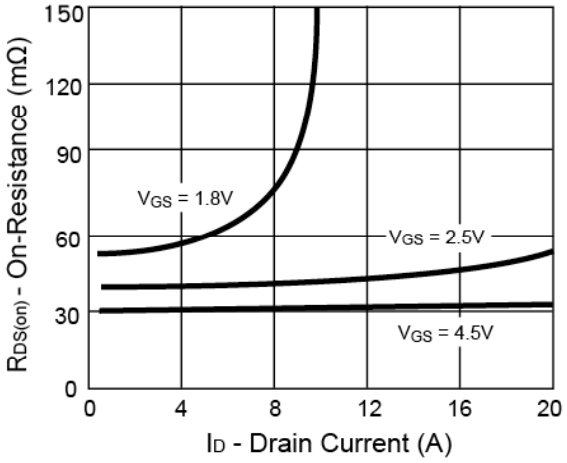
Output Characteristics



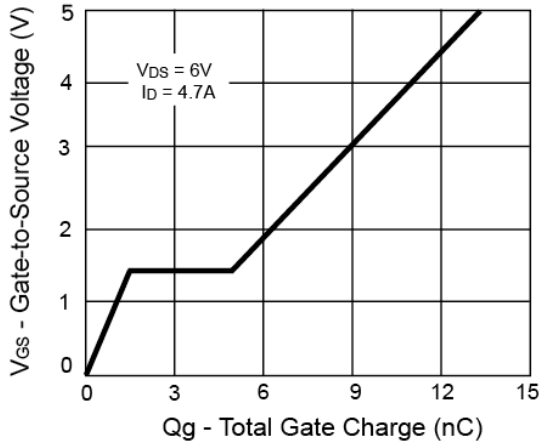
Transfer Characteristics



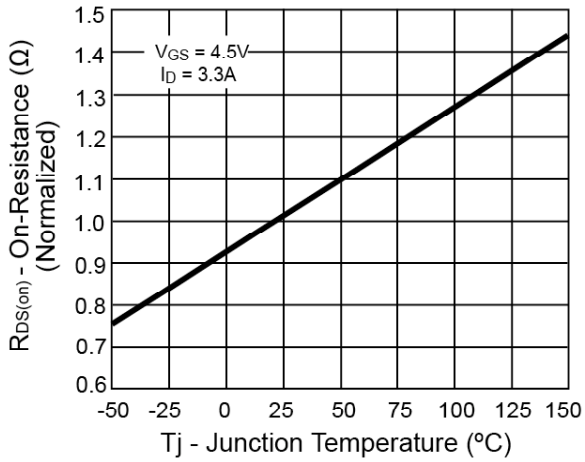
On-Resistance vs. Drain Current



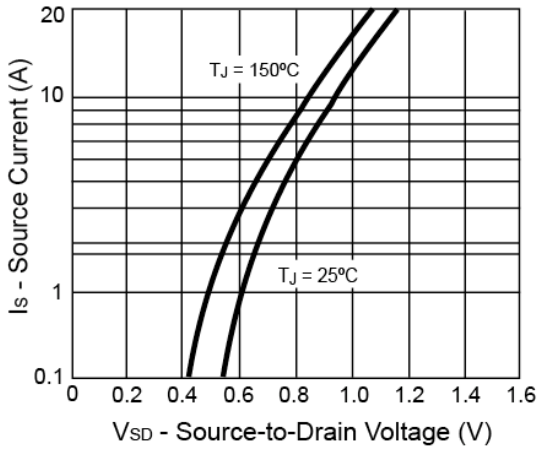
Gate Charge



On-Resistance vs. Junction Temperature

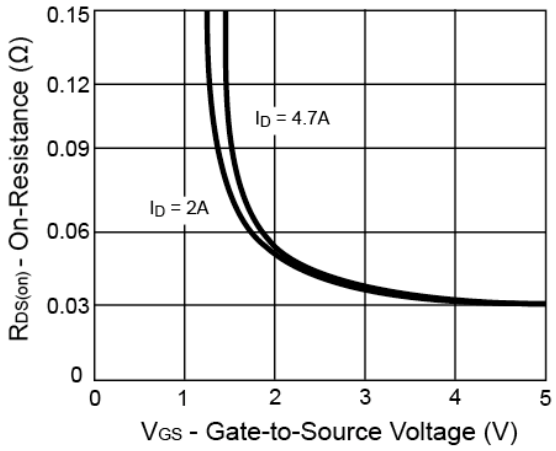


Source-Drain Diode Forward Voltage

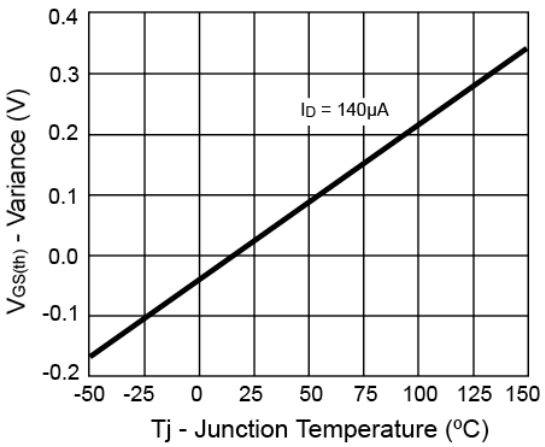


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

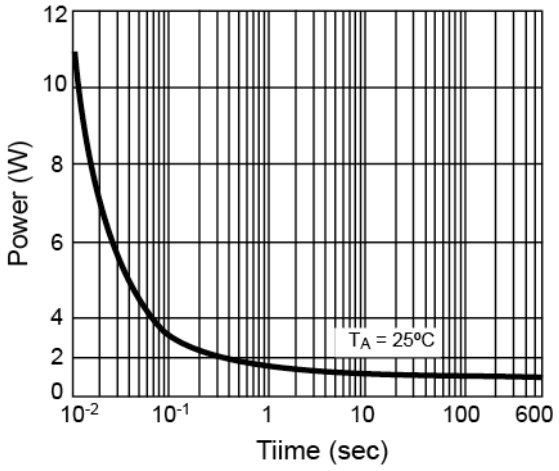
On-Resistance vs. Gate-Source Voltage



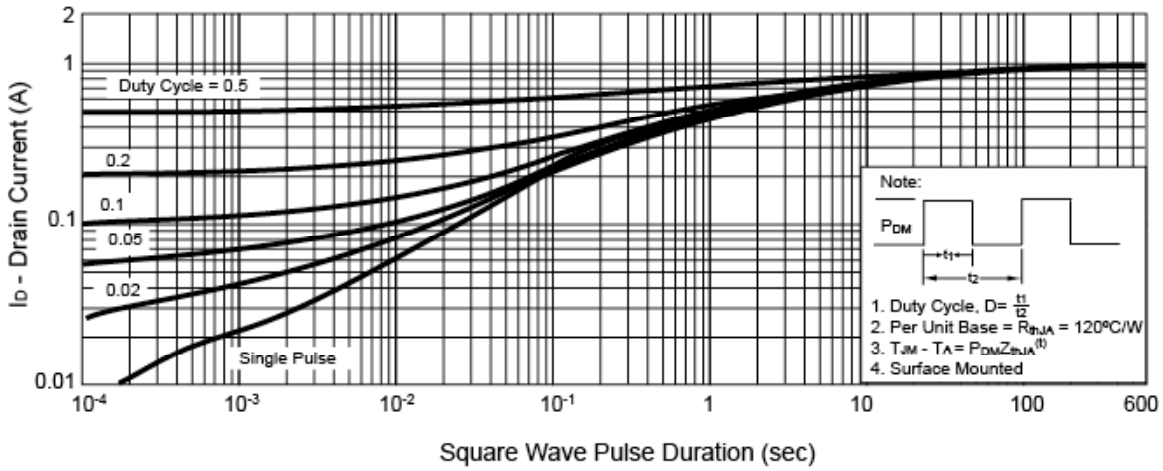
Threshold Voltage



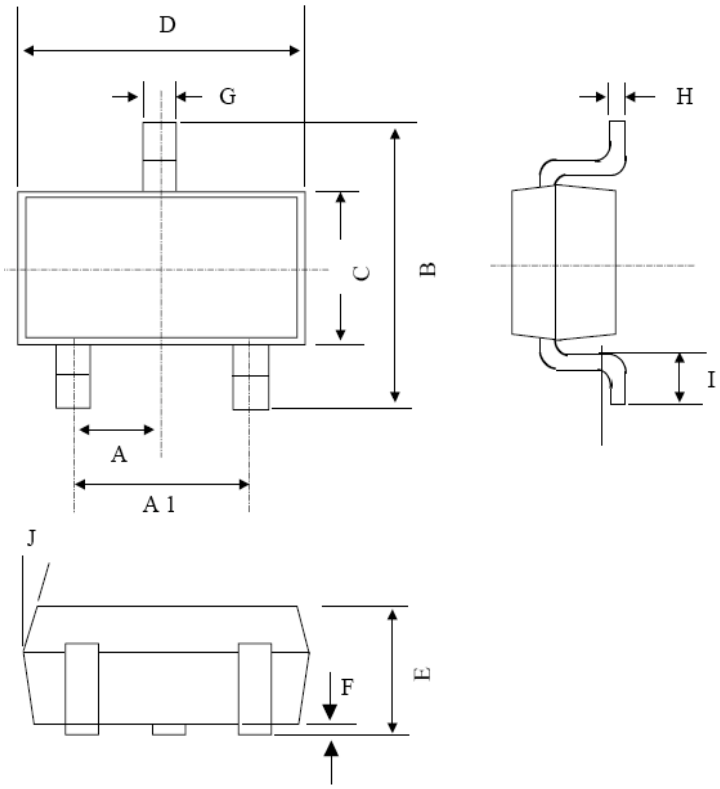
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

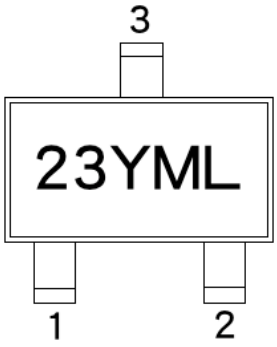


SOT-23 Mechanical Drawing



SOT-23 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	2.88	2.91	0.113	0.115
B	0.39	0.42	0.015	0.017
C	1.78	2.03	0.070	0.080
D	0.51	0.61	0.020	0.024
E	1.59	1.66	0.063	0.065
F	1.04	1.08	0.041	0.043
G	0.07	0.09	0.003	0.004

Marking Diagram



23 = Device Code
Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
L = Lot Code

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