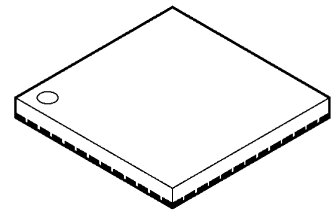
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB2173FTG

2-Source Stereo Headphone Amplifier

The TB2173FTG is a stereo headphone amplifier IC that can accept two sources, developed for portable audio systems.

It is particularly ideal for digital portable audio systems having built-in tuners.


VQON44-P-0606-0.4

Weight: 0.05 g (typ.)

Product indication: B2173G

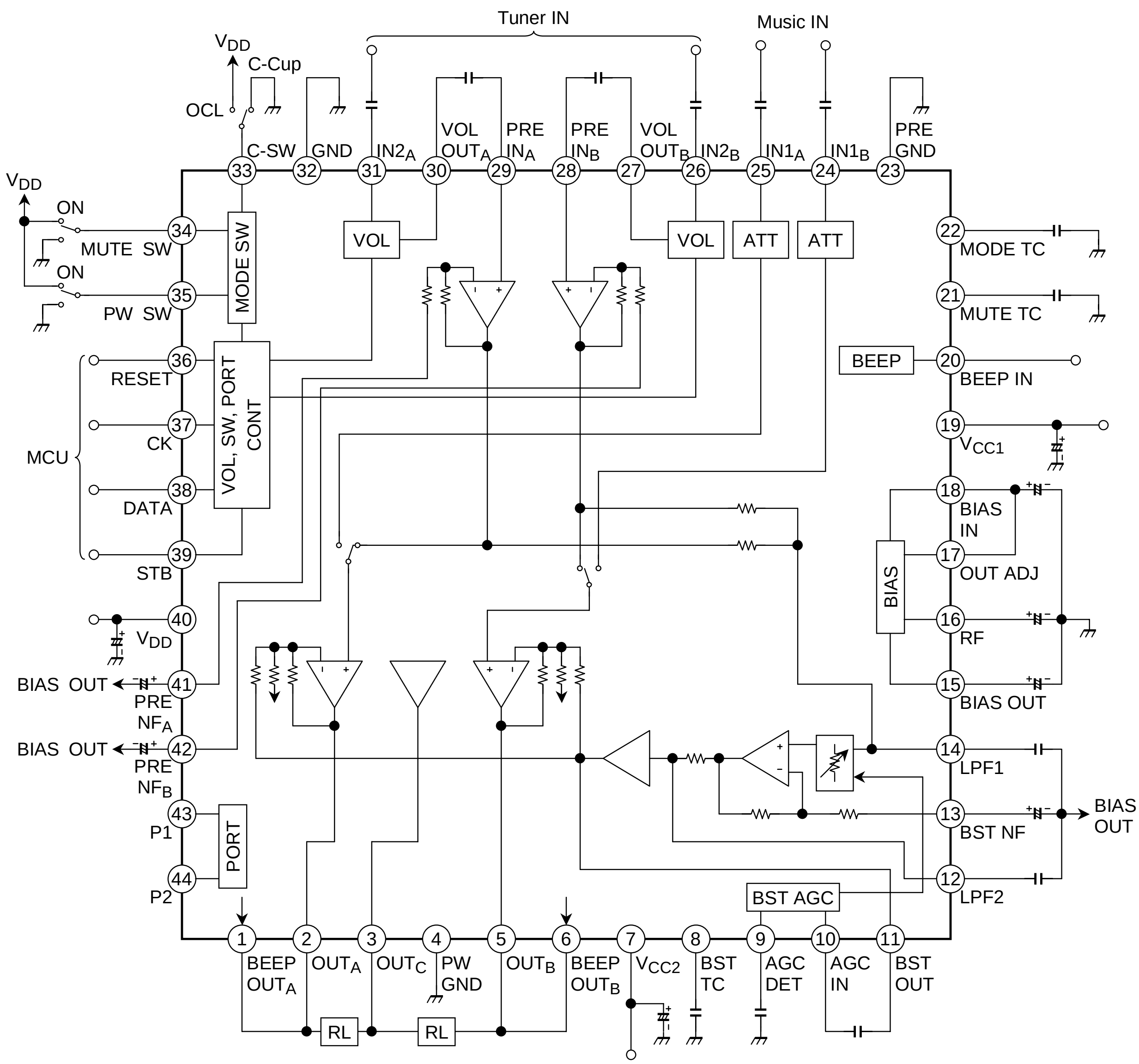
Features

- Accepts headphone amplifier inputs from two sources
- Selectable headphone amplifier output: Output coupling or OCL
- Incorporates beep circuit
- Incorporates power switch (controlled using port or command)
- Supports power muting (controlled using port or command)
- Features with single source only (tuner mode):
  - Electronic volume
    Provides logic reset feature
  - Low-frequency boost (with AGC)
- Two port expansion circuits
- Operating supply voltage range: Ta = 25°C
  V_{DD} (opr) = 1.8 to 4.5 V
  V_{CC1} (opr) = 1.8 to 4.5 V
  V_{CC2} (opr) = 0.9 to 4.5 V

Note: Use the device with V_{CC1} greater than or equal to V_{CC2}.

- Handle the product with great care because its surge resistance is low.
- Ensure that the product is mounted correctly.
  Otherwise, the product or connected equipment may get damaged or degrade.

Block Diagram (OCL Type)

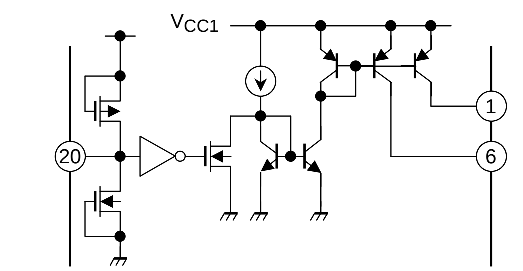
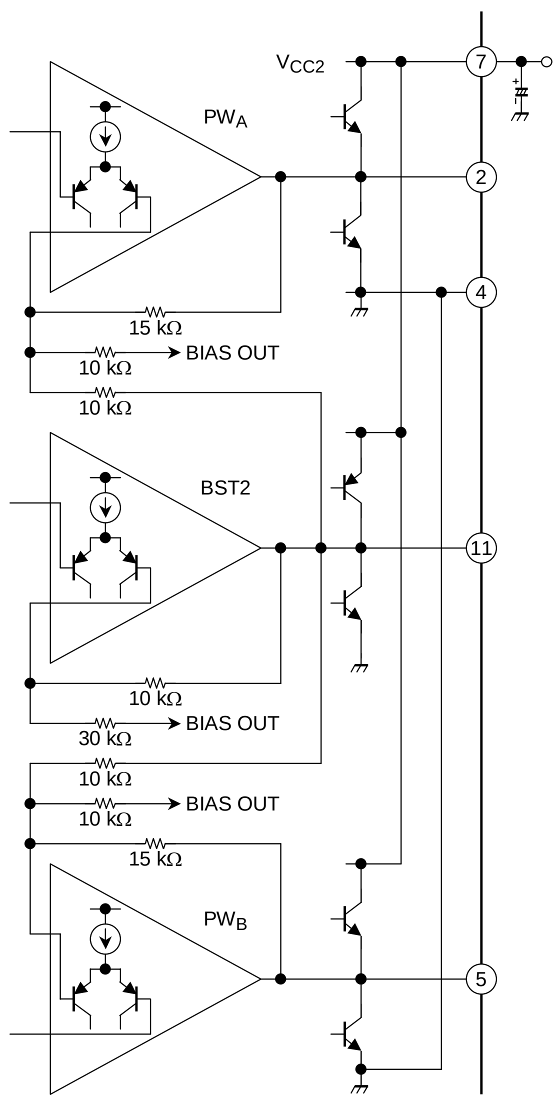


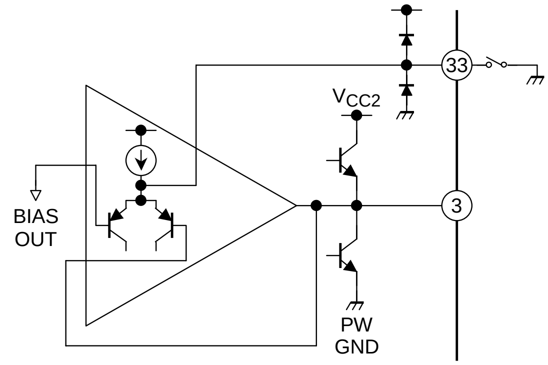
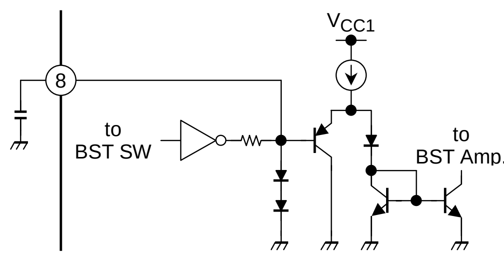
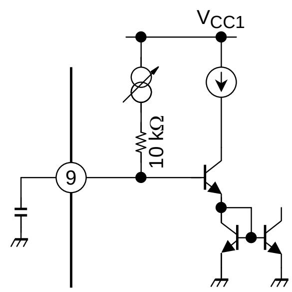
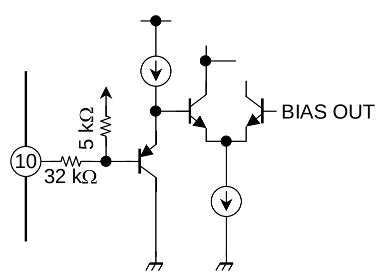
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

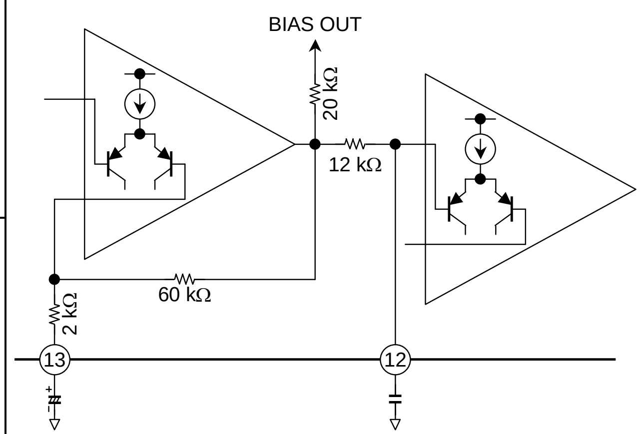
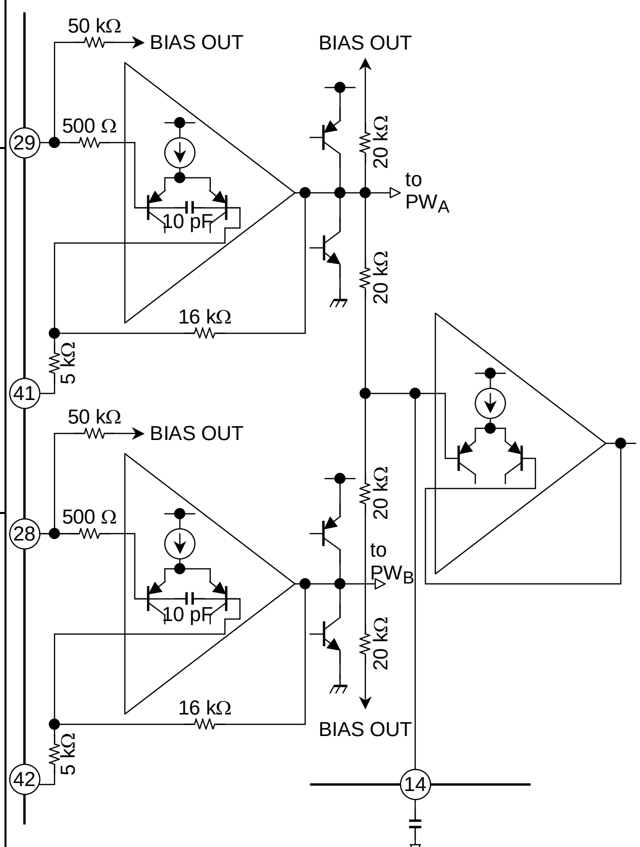
Pin Functions

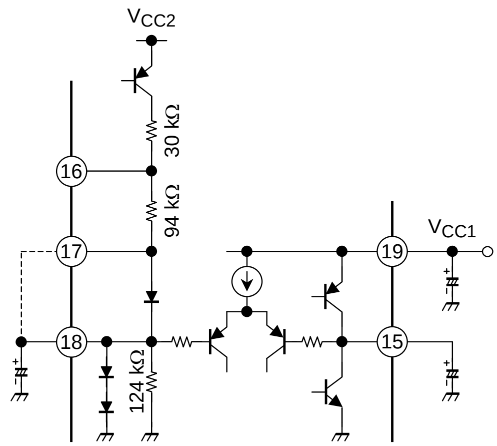
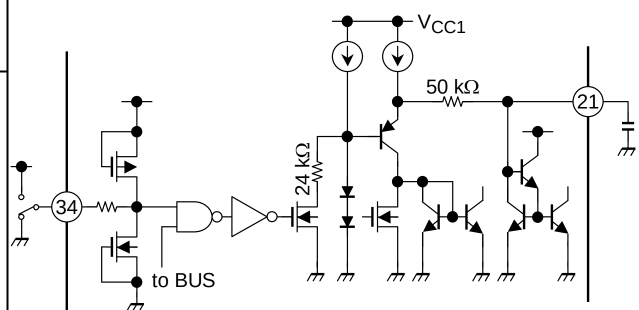
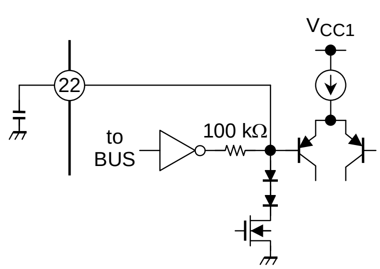
Pin voltages: Typical quiescent pin voltages in test circuit, $V_{DD} = V_{CC1} = 2.1$ V, $V_{CC2} = 1.2$ V, Ta = 25°C

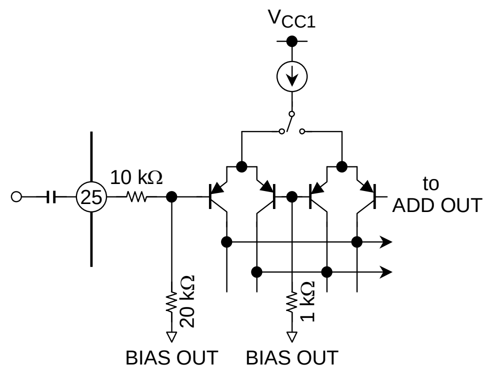
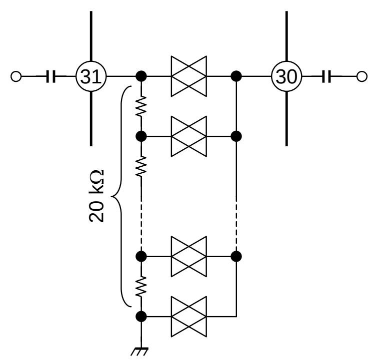
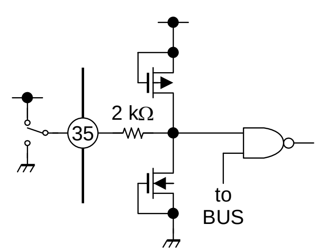
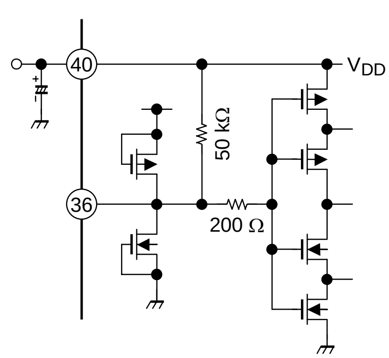
The equivalent circuit diagrams are intended as an aid for describing circuits; they may be shown in abbreviated or simplified format.

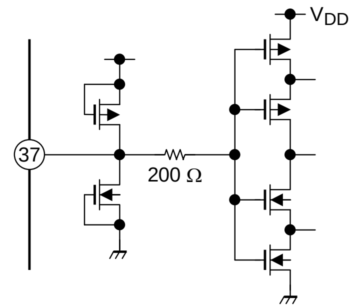
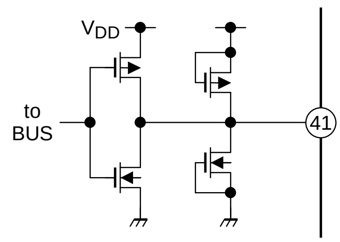
Pin No. and Name		Function	Internal Equivalent Circuit	Pin Voltage (V)
1	BEEP OUT_A	Beep signal output		—
6	BEEP OUT_B			
20	BEEP IN	Beep signal input		—
2	OUT_A	Power amplifier output		0.6
5	OUT_B			
4	PW GND	Power drive stage ground		0
7	V_{CC2}	Power drive stage V_{CC}		1.2
11	BST OUT	Boost amplifier output		0.6

<table>
<tr><th colspan="2">Pin No. and Name</th><th>Function</th><th>Internal Equivalent Circuit</th><th>Pin Voltage (V)</th></tr>
<tr><td>3</td><td>OUT_C</td><td>Center amplifier output</td><td rowspan="2">
</td><td>0.6</td></tr>
<tr><td>33</td><td>C-SW</td><td>Output application select switch
(V_{DD} : OCL
GND : Output coupling)</td><td>0.6</td></tr>
<tr><td>8</td><td>BST TC</td><td>Pin for reducing boost ON/OFF pop noise</td><td>
</td><td>—</td></tr>
<tr><td>9</td><td>AGC DET</td><td>Boost AGC detection</td><td>
</td><td>—</td></tr>
<tr><td>10</td><td>AGC IN</td><td>Boost AGC input
The level of the input signal to the BST amplifier is varied according to the input level at this pin.
Input impedance: 37 kΩ (typ.)</td><td>
</td><td>0.6</td></tr>
</table>

Pin No.	and Name	Function	Internal Equivalent Circuit	Pin Voltage (V)
12	LPF2	Boost filter pin 2 Cutoff frequency setting 2 for low-frequency boost		0.6
13	BST NF	Boost amplifier NF		0.6
14	LPF1	Boost filter pin 1 Cutoff frequency setting 1 for low-frequency boost		0.6
28	PRE IN_B	Tuner mode: Power amplifier input		0.6
29	PRE IN_A			
41	PRE NF_A	Tuner mode: Power amplifier NF		0.6
42	PRE NF_B			

Pin No.	and Name	Function	Internal Equivalent Circuit	Pin Voltage (V)
15	BIAS OUT	Bias circuit output		0.6
16	RF	Ripple filter pin		1.1
17	OUT ADJ	Output DC voltage adjustment The output bias voltage is set to an optimum value according to the voltage applied to V_{CC2}.		0.6
18	BIAS IN	Bias circuit input		0.6
19	V_{CC1}	V_{CC} other 2 than V_{DD} and V_{CC2}		2.1
21	MUTE TC	Mute smoothing		—
34	MUTE SW	Power mute switch Mute switch for power amplifier. When controlling MUTE SW using a port, specify "0" in a command. In that case, the IC operates as follows according to the port state: High: Mute ON Low: Mute OFF When controlling MUTE SW using a command, drive the port low.		—
22	MODE TC	Pin for reducing mode change pop noise		—
23	PRE GND	Ground for circuits other than logic and power drive stage	—	0

Pin No. and Name		Function	Internal Equivalent Circuit	Pin Voltage (V)
24	IN_{1B}	Input pin 1 Input pin with G_V = 8dB		0.6
25	IN_{1A}			
26	IN_{2B}	Input pin 2 The input signal is supplied to the power amplifier through the electronic volume circuit and preamplifier.		0
31	IN_{2A}			
27	VOL OUT_B	Volume output IN_2 electronic volume output		0
30	VOL OUT_A			
32	GND	Logic ground	—	0
35	PW SW	Power switch IC ON/OFF switch. The switch does not, however, control the electronic volume circuit. When controlling PW SW using a port, specify "1" in a command. In that case, the IC operates as follows according to the port state: High: IC ON Low: IC OFF When controlling PW SW using a command, drive the port high.		—
36	RESET	Command reset This pin resets the bus data. High: No reset Low: Reset		2.1
40	V_{DD}	Logic power supply		2.1

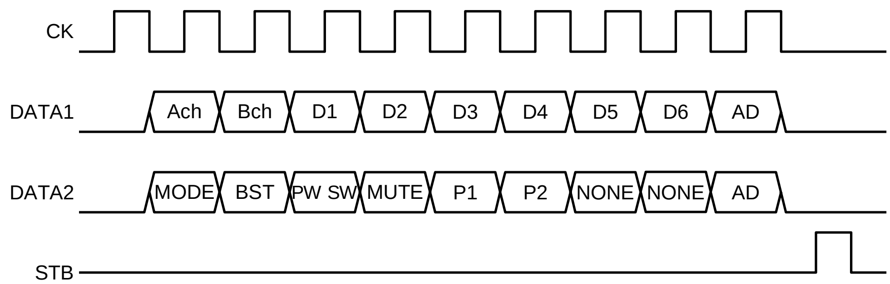
Pin No. and Name		Function	Internal Equivalent Circuit	Pin Voltage (V)
37	CK	Clock input		—
38	DATA	Data input		—
39	STB	Strobe input		—
43	P1	Port expansion		—
44	P2			

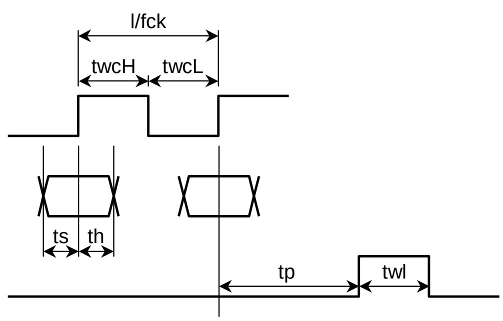
Functional Description

Bus Data

Timing Charts

1. Serial Data Specification (initial data is not set.)





Characteristics	Symbol	Min	Typ.	Max	Unit
Clock frequency	fck	—	—	1.0	MHz
High-level pulse width	twcH	500	—	—	nSec
Low-level pulse width	twcL	500	—	—	nSec
Data setup time	ts	100	—	—	nSec
Data hold time	th	100	—	—	nSec
STB setup time	tp	150	—	—	nSec
STB pulse width	twl1	0.80	—	—	μSec

(1) Ach/Bch control data: 2 bits (Ach, Bch)

Ach	Bch	Operation
0	0	No volume data set
1	0	Volume data set for Ach only
0	1	Volume data set for Bch only
1	1	Volume data sets for both channels

(2) Volume data: 6 bits (D1 to D6)

Volume Value		D1	D2	D3	D4	D5	D6	Volume Value		D1	D2	D3	D4	D5	D6
1	–0.1dB	0	0	0	0	0	0	33	–34.3	0	0	0	0	0	1
2	–2.1	1	0	0	0	0	0	34	–34.7	1	0	0	0	0	1
3	–4.0	0	1	0	0	0	0	35	–35.1	0	1	0	0	0	1
4	–5.5	1	1	0	0	0	0	36	–35.5	1	1	0	0	0	1
5	–6.9	0	0	1	0	0	0	37	–36.0	0	0	1	0	0	1
6	–8.2	1	0	1	0	0	0	38	–36.5	1	0	1	0	0	1
7	–9.6	0	1	1	0	0	0	39	–37.0	0	1	1	0	0	1
8	–10.9	1	1	1	0	0	0	40	–37.6	1	1	1	0	0	1
9	–12.3	0	0	0	1	0	0	41	–38.2	0	0	0	1	0	1
10	–13.6	1	0	0	1	0	0	42	–38.9	1	0	0	1	0	1
11	–14.9	0	1	0	1	0	0	43	–39.6	0	1	0	1	0	1
12	–16.3	1	1	0	1	0	0	44	–40.4	1	1	0	1	0	1
13	–17.6	0	0	1	1	0	0	45	–41.5	0	0	1	1	0	1
14	–19.0	1	0	1	1	0	0	46	–42.7	1	0	1	1	0	1
15	–20.3	0	1	1	1	0	0	47	–43.3	0	1	1	1	0	1
16	–22.1	1	1	1	1	0	0	48	–43.9	1	1	1	1	0	1
17	–23.7	0	0	0	0	1	0	49	–44.7	0	0	0	0	1	1
18	–25.1	1	0	0	0	1	0	50	–45.3	1	0	0	0	1	1
19	–26.6	0	1	0	0	1	0	51	–46.1	0	1	0	0	1	1
20	–27.9	1	1	0	0	1	0	52	–46.9	1	1	0	0	1	1
21	–28.5	0	0	1	0	1	0	53	–47.7	0	0	1	0	1	1
22	–29.1	1	0	1	0	1	0	54	–48.7	1	0	1	0	1	1
23	–29.3	0	1	1	0	1	0	55	–49.9	0	1	1	0	1	1
24	–29.8	1	1	1	0	1	0	56	–51.1	1	1	1	0	1	1
25	–30.5	0	0	0	1	1	0	57	–52.5	0	0	0	1	1	1
26	–30.8	1	0	0	1	1	0	58	–54.4	1	0	0	1	1	1
27	–31.3	0	1	0	1	1	0	59	–56.1	0	1	0	1	1	1
28	–31.7	1	1	0	1	1	0	60	–57.8	1	1	0	1	1	1
29	–32.2	0	0	1	1	1	0	61	–60.0	0	0	1	1	1	1
30	–32.8	1	0	1	1	1	0	62	–63.5	1	0	1	1	1	1
31	–33.2	0	1	1	1	1	0	63	–68.9	0	1	1	1	1	1
32	–33.9	1	1	1	1	1	0	64	–90.0	1	1	1	1	1	1

(3) Identification data: 1 bit (AD)

AD	Operation
0	Recognized as DATA1
1	Recognized as DATA2

(4) MODE SW data: 1 bit (MODE)

MODE	Operation
0	Outputs the input signal components for IN2 (tuner mode).
1	Outputs the input signal components for IN1 (music mode).

(5) BST SW data: 1 bit (BST)

BST	Operation
0	Boost OFF
1	Boost ON

(6) PW SW: 1 bit (PW SW)
PW SW can be controlled using either a command or port, with the following truth table:

Port	Command	Operation
0 (OFF)	0 (OFF)	0 (IC OFF)
0 (OFF)	1 (ON)	0 (IC OFF)
1 (ON)	0 (OFF)	0 (IC OFF)
1 (ON)	1 (ON)	1 (IC ON)

(7) MUTE SW: 1 bit (MUTE)
MUTE SW can be controlled using either a command or port, with the following truth table:

Port	Command	Operation
0 (OFF)	0 (OFF)	0 (MUTE OFF)
0 (OFF)	1 (ON)	1 (MUTE ON)
1 (ON)	0 (OFF)	1 (MUTE ON)
1 (ON)	1 (ON)	1 (MUTE ON)

(8) Power expansion: 1 bit (P1/P2)

P1/P2	Operation
0	Port Low
1	Port High

(9) NONE
An invalid bit

(10) Strobe data (STB)

STB	Operation
0	No data write
1	Data write

(11) Initial command upon command reset

DATA1	Ach	Bch	D1	D2	D3	D4	D5	D6	AD
Initial value	1	1	1	1	1	1	1	1	0
DATA2	MODE	BST	PW SW	MUTE	P1	P2	Invalid	Invalid	AD
Initial value	0	0	0	1	1	0			

Bit 9 specifies the address.

The initial address selected upon a reset is DATA1.

Command data is maintained over a power cycle.

2. IC Settings According to Supply Voltage

(1) Connecting power supplies
The TB2173FTG supports an end product that uses either one or two batteries. Connect the power supply pins according to the number of batteries, as follows:

	Microcontroller power supply	Battery power supply
Single battery	V_{DD}, V_{CC1}	V_{CC2}
Two batteries	V_{DD}	V_{CC1}, V_{CC2}

Note: Use the device with V_{CC1} greater than or equal to V_{CC2}.

(2) Handling the OUT ADJ pin (pin 17)
When using a single battery: Jumper OUT ADJ (pin 17) and BIAS IN (pin 18).
When using two batteries: Leave OUT ADJ (pin 17) open.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol		Rating	Unit
DC supply voltage	V_{DD}		5.0	V
	V_{CC}			
Operating supply voltage	V_{DD}		4.5	V
	V_{CC}			
Power block output current	I_O		100	mA
Power dissipation	P_D	(Note 1)	350	mW
		(Note 2)	1200	
Operating temperature	T_{opr}		−25 to 75	°C
Storage temperature	T_{stg}		−55 to 150	°C

Note 1: IC alone: When the IC is used at 25°C or higher, reduce 2.8 mW per 1°C.

Note 2: When mounted on Toshiba standard board: When the IC is used at 25°C or higher, reduce 9.6 mW per 1°C.

The absolute maximum ratings of a semiconductor device are a set of specified parameter values which must not be exceeded during operation, even for an instant.
Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blowup and/or burning.
The equipment manufacturer should design so that no absolute maximum rating value is exceeded with respect to current, voltage, power dissipation, temperature, etc.
Ensuring that the parameter values remain within these specified ranges during device operation will help to ensure that the integrity of the device is not compromised.

Electrical Characteristics

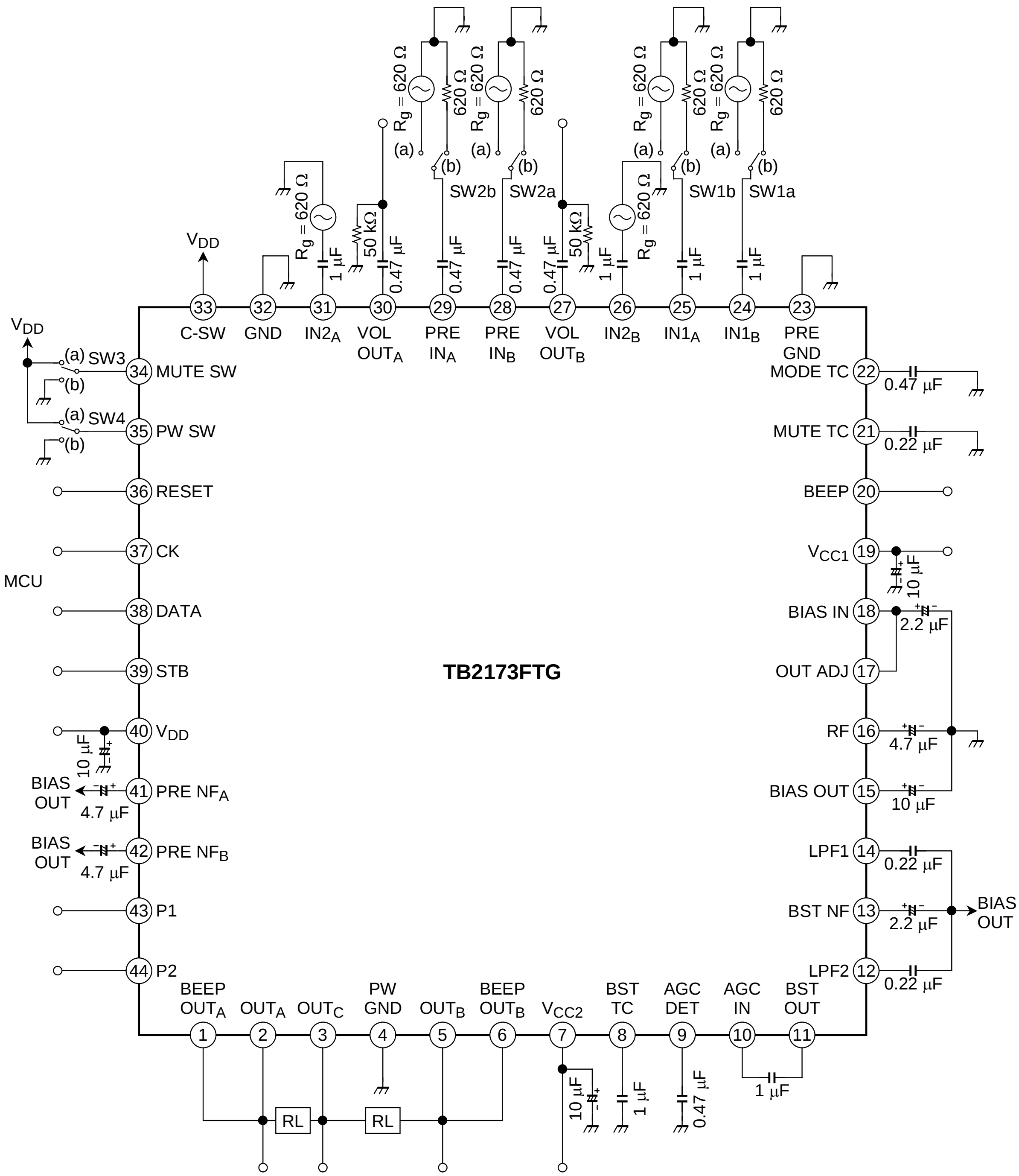
($V_{DD} = V_{CC1} = 2.1$ V, $V_{CC2} = 1.2$ V, $R_g = 600\ \Omega$, $R_L = 16\ \Omega$, f = 1 kHz, OCL mode, Ta = 25°C, SW3: b, SW4: a, unless otherwise specified)

Music mode — **Input: IN1, Output: OUT, SW1: a**
Tuner mode — **Input: PRE IN, Output: OUT, SW2: a**
Electronic volume — **Input: IN2, Output: VOL OUT**

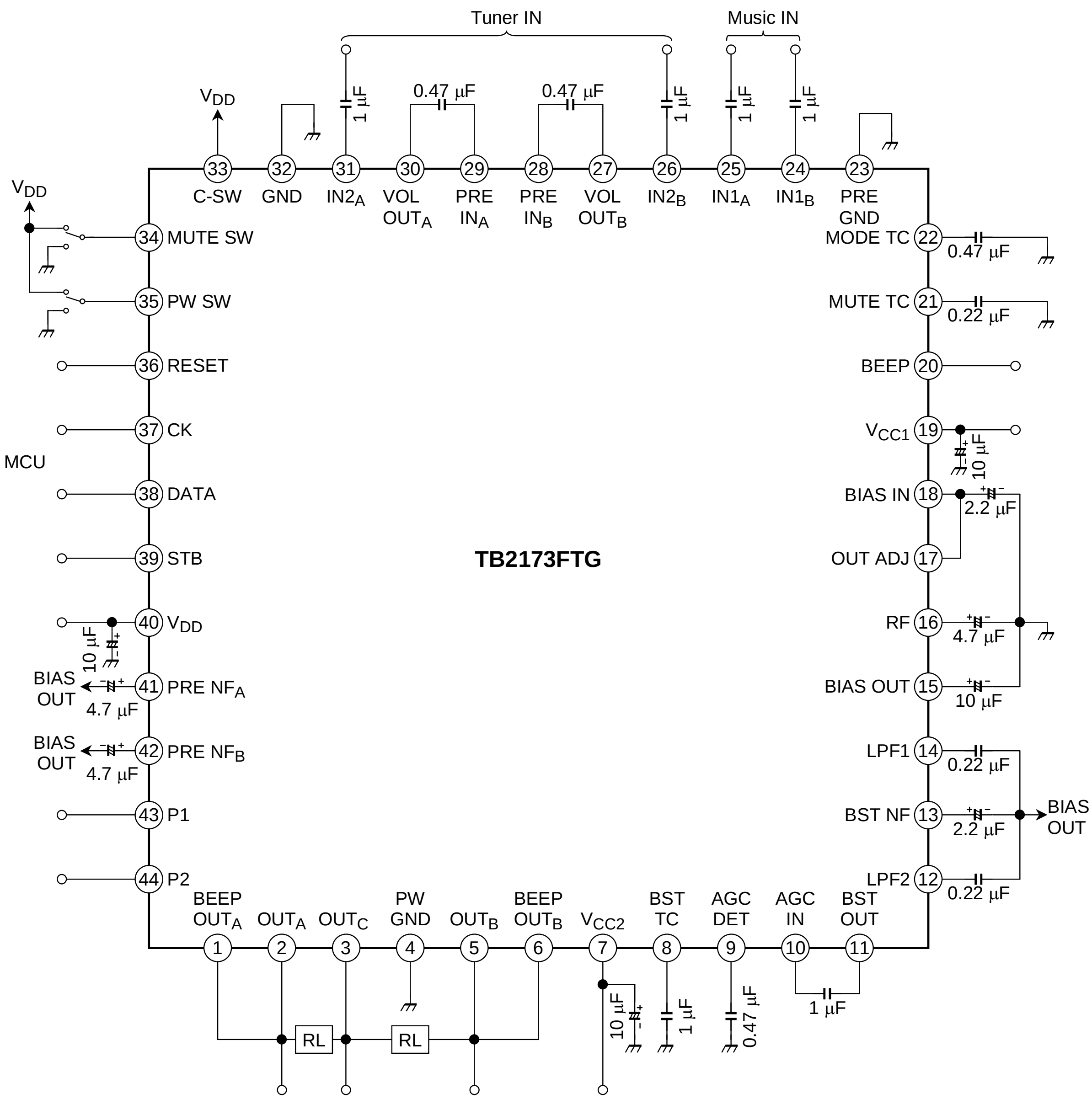
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Quiescent current		I_{CCQ1}	Standby (V_{DD}), SW4: b	—	—	5	μA
		I_{CCQ2}	Standby (V_{CC1}, V_{CC2})	—	—	5	μA
		I_{CCQ3}	Mute ON: Music mode (V_{CC1}), SW3: a	—	0.6	1.0	mA
		I_{CCQ4}	Mute ON: Music mode (V_{CC2}), SW3: a	—	0.3	0.6	mA
		I_{CCQ5}	Mute ON: Music mode (V_{CC1}), SW3: a	—	0.6	1.0	mA
		I_{CCQ6}	Mute ON: Music mode (V_{CC2}), SW3: a	—	0.3	0.6	mA
		I_{CCQ7}	No signal: Music mode (V_{CC1})	—	0.9	1.4	mA
		I_{CCQ8}	No signal: Music mode (V_{CC2})	—	0.7	1.4	mA
		I_{CCQ9}	No signal: Music mode (V_{CC1})	—	0.9	1.4	mA
		I_{CCQ10}	No signal: Music mode (V_{CC2})	—	0.8	1.6	mA
Driving current		I_{CCD1}	0.1 mW∗2ch/16 Ω (V_{CC1})	—	1.0	—	mA
		I_{CCD2}	0.1 mW∗2ch/16 Ω (V_{CC2})	—	4.5	—	mA
Music mode	Voltage gain	G_{V1}	$V_o = -20$dBV	6.5	8	9.5	dB
	Channel balance	CB1	$V_o = -20$dBV	−1.5	0	+1.5	dB
	Output power	P_{o1}	THD = 10%	7	9.5	—	mW
	Total harmonics distortion	THD1	$P_o = 1$ mW	—	0.2	0.5	%
	Output noise voltage	V_{no1}	$R_g = 600\ \Omega$, IHF-A, SW1: b	—	−98	−92	dBV
	Interchannel crosstalk	CT1	$V_o = -20$dBV	−32	−38	—	dB
	Intermode crosstalk	CT2	$V_o = -20$dBV, monitor: music	−45	−51	—	dB
	Ripple rejection ratio	RR1	$f_r = 100$Hz, $V_r = -20$dBV, injected to V_{CC1}	−70	−85	—	dB
		RR2	$f_r = 100$Hz, $V_r = -20$dBV, injected to V_{CC2}	−60	−75	—	dB
	Mute attenuation	ATT1	$V_o = -20$dBV, SW3: b → a	−100	−120	—	dB
Tuner mode	Voltage gain	G_{V2}	$V_o = -20$dBV	22.5	24	25.5	dB
	Channel balance	CB2	$V_o = -20$dBV	−1.5	0	+1.5	dB
	Output power	P_{o2}	THD = 10%	7	9.5	—	mW
	Total harmonics distortion	THD2	$P_o = 1$ mW	—	0.2	0.5	%
	Output noise voltage	V_{no2}	$R_g = 600\ \Omega$, IHF-A, SW2: b	—	−90	−84	dBV
	Interchannel crosstalk	CT3	$V_o = -20$dBV	−27	−33	—	dB
	Intermode crosstalk	CT4	$V_o = -20$dBV, monitor: tuner	−39	−45	—	dB
	Ripple rejection ratio	RR3	$f_r = 100$ Hz, $V_r = -20$dBV, injected to V_{CC1}	−58	−73	—	dB
		RR4	$f_r = 100$ Hz, $V_r = -20$dBV, injected to V_{CC2}	−43	−58	—	dB
	Mute attenuation	ATT2	$V_o = -20$dBV	−95	−115	—	dB
	Boost	BST1	f = 100 Hz, $V_o = -20$dBV	1.5	4.5	7.5	dB
		BST2	f = 100 Hz, $V_o = -30$dBV	8.5	11.5	14.5	dB
		BST3	f = 100 Hz, $V_o = -50$dBV	9.5	12.5	15.5	dB

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Electronic volume	Maximum input level	V_{im}	THD = 1%	250	320	—	mVrms
	Attenuation error	Δ ATT	V_o = −10dBV	−3.0	0	+3.0	dB
	Channel balance	CB3	V_o = −10dBV	−1.5	0	+1.5	dB
	Maximum attenuation	ATT	V_o = −10dBV	−80	−90	—	dB
Logic	Bus operating frequency	f_{opr}		—	—	1	MHz
	Input voltage, High level	V_{IH}	CK, DATA, STB, and RESET input pins	V_{DD} × 0.75	—	V_{DD}	V
	Input voltage, Low level	V_{IL}	CK, DATA, STB, and RESET input pins	0	—	V_{DD} × 0.25	V
	Input leakage current	I_{LI}	V_{IH}: V_{DD}, V_{IL}: 0 V	—	—	±1	μA
	Port expansion driving current	I_{OL}	V_{OL}: 0.3 V	1.0	—	—	mA
		I_{OH}	V_{OH}: V_{DD}-0.3 V	−1.0	—	—	mA
Beep output level		V_{BEEP}	SW3: a	−55	−50	−45	dBV
PW SW pin ON voltage		V35 (ON)		V_{DD} × 0.8	—	V_{DD}	V
PW SW pin OFF voltage		V35 (OFF)		0	—	V_{DD} × 0.2	V
MUTE SW pin ON voltage		V34(ON)		V_{DD} × 0.8	—	V_{DD}	V
MUTE SW pin OFF voltage		V34 (OFF)		0	—	V_{DD} × 0.2	V

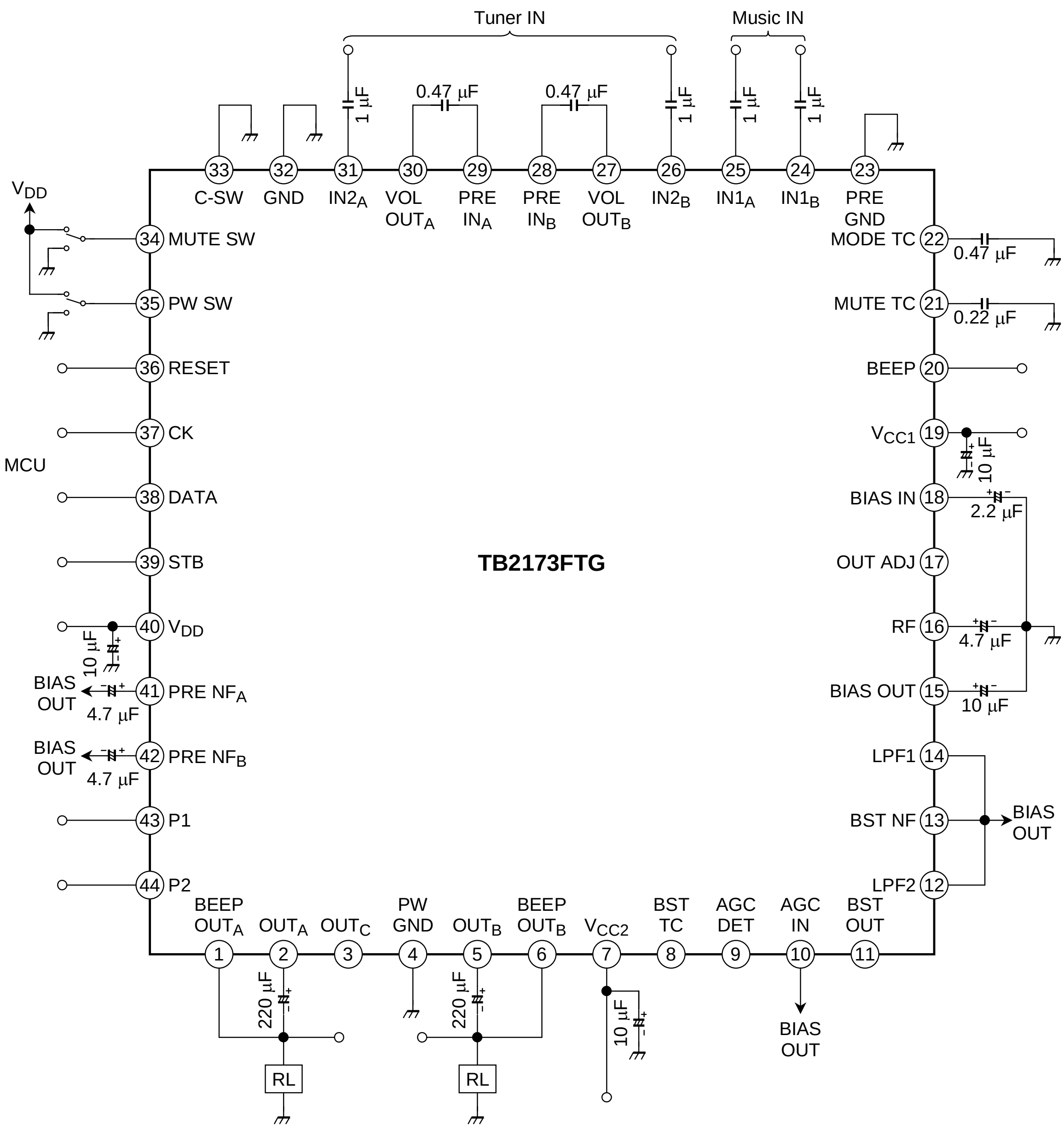
Test Circuit Diagram



Example Application Circuit 1 (1.5-V OCL)

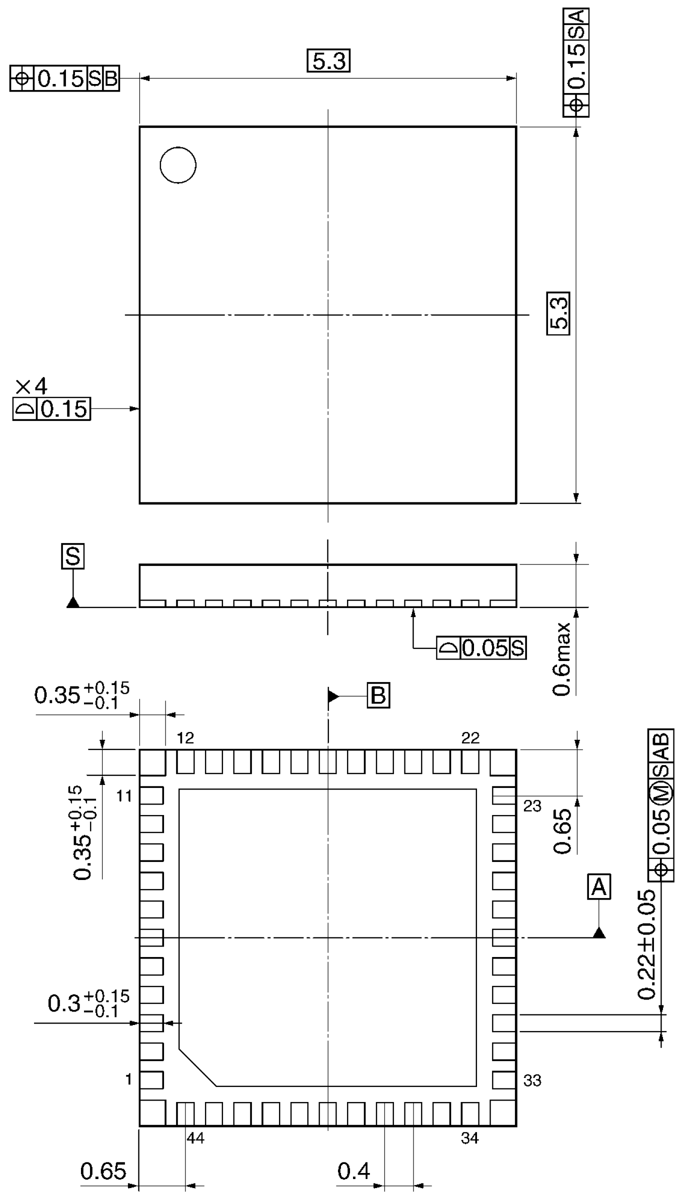


Example Application Circuit 2 (3-V output coupling, without low-frequency boost)



Package Dimensions

VQON44-P-0606-0.4 Unit: mm



Weight: 0.05 g (typ.)

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060116EBA

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About solderability, following conditions were confirmed

- Solderability

(1) Use of Sn-37Pb solder Bath
- solder bath temperature = 230°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- solder bath temperature = 245°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux