DFPAU-DP

Floating Point Arithmetic Coprocessor

Double Precision

ver 3.02

OVERVIEW

DFPAU-DP is a Floating Point Arithmetic Coprocessor, designed to assist CPU in performing the floating point arithmetic computations. DFPAU-DP directly replaces C software functions, by equivalent, very fast hardware operations, which significantly accelerate system performance. It doesn't require any programming, so it also doesn't require any modifications made in the main software. Everything is done automatically during software compilation by the DFPAU-DP C driver.

DFPAU-DP was designed to operate with DCD's DP8051, but can also operate with any other 8-, 16- and 32-bit processor. Drivers for all popular 8051 C compilers are delivered together with the DFPAU-DP package.

DFPAU-DP uses the specialized algorithms to compute math functions. It supports **addition, subtraction, multiplication, division, square root**, and comparison. It has built-in conversion instructions from integer type to floating point type and vice versa. The input numbers format is according to IEEE-754 standard. DFPAU-DP supports double and single precision real numbers, 8-bit, 16-bit and 32-bit integers. DFPAU-DP is prepared to use with 8-, 16- and 32-bit processors. **Each floating point function can be turned on/off** at configuration level providing the flexible scalability of DFPAU-DP module. It allows save silicon space and provides exact configuration required by certain application.

DFPAU-DP is a technology independent design that can be implemented in a variety of process technologies.

APPLICATIONS

- Math coprocessors
- DSP algorithms
- Embedded arithmetic coprocessor
- Fast data processing & control

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KEY FEATURES

- **Direct replacement** for C double, float software functions such as: +, -, *, /,==, !=,>=, <=, <, >
- Configurability of all available functions
- C interface supplied for all popular compilers: GNU C/C++, 8051 compilers
- **No programming required**
- IEEE-754 Double precision real format support – **double type**
- IEEE-754 Single precision real format support – **float type**
- 8-bit, 16-bit 32-bit and 52-bit integers format supported – **integer types**
- Flexible arguments and result registers location
- Performs the following functions:
  - *FADD, FSUB – addition, subtraction*
  - *FMUL, FDIV – multiplication, division*
  - *FSQRT – square root*
  - *FXAM – examine input data*
  - *FUCOM – comparison*
  - *FCLD, FILD – 8-bit, 16-bit integer to double*
  - *FLLD, FELD – 32-bit, 52-bit integer to double*
  - *FCST, FIST – double to 8-bit, 16-bi integer*
  - *FLST, FEST – double to 32-bit, 52-bit integer*
  - *FFLD – float to double*
  - *FFST – double to float*
- Exceptions built-in routines
- Masks each exception indicator:
  - *Precision lack PE*
  - *Underflow result UE*
  - *Overflow result OE*
  - *Invalid operand IE*
  - *Division by zero ZE*
  - *Denormal operand DE*
- Fully configurable
- Fully synthesizable, static synchronous design with no internal tri-states

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted Netlist or/and
  - plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - NCSim automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

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LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

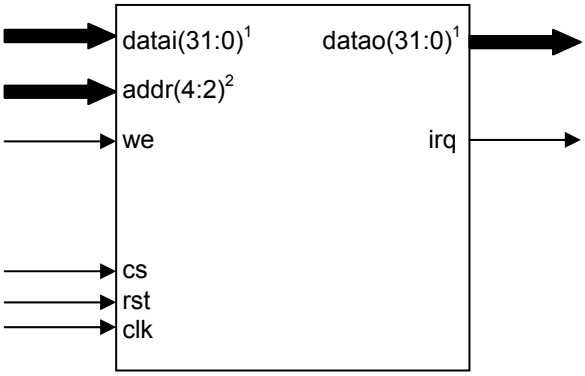
Single Design license allows using IP Core in single FPGA bitstream and ASIC implementation. It also permits FPGA prototyping before ASIC production.

Unlimited Designs license allows using IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time of use limitations.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *Netlist to HDL Source*
  - *Single Design to Unlimited Designs*

SYMBOL



PINS DESCRIPTION

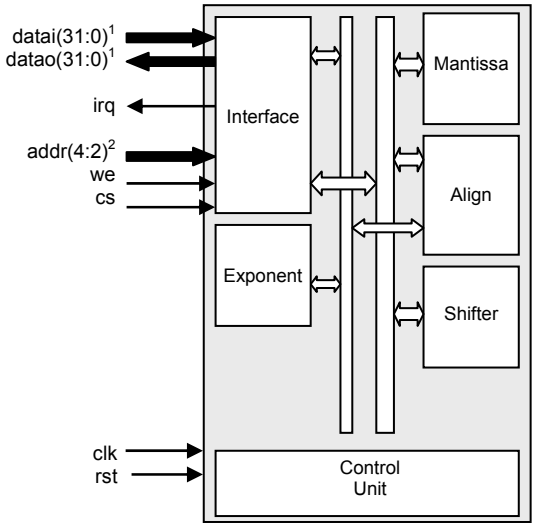
PIN	TYPE	DESCRIPTION
clk	Input	Global system clock
rst	Input	Global system reset
cs	Input	Chip select for read/write
datai[31:0][1]	Input	Data bus input
addr[4:2][2]	Input	Register address to read/write
we	Input	Data write enable
datao[31:0][1]	Output	Data bus output
irq	Output	Interrupt request indicator

1 – data bus can be configured as 8-, 16- or 32- bit depends on processor's bus size

2 – address bus is aligned to work with 8- (3:0), 16- (3:1) or 32- (4:2) bit processors

BLOCK DIAGRAM

Mantissa – performs operations on mantissa part of number. The addition, subtraction, multiplication, division, square root, comparison and conversion operations are executed in this module. It contains mantissas and work registers.



Exponent – performs operations on exponent part of number. The addition, subtraction, shifting, comparison and conversion operations are executed in this module. It contains exponents and work registers.

Align – performs the numbers analyze against IEEE-754 standard compliance. Information about the data classes are passed as result to appropriate internal module.

Shifter – performs mantissa shifting during normalization, denormalization operations.

Information about shifted-out bits are stored for rounding process.

Control Coprocessor – manages execution of all instructions and internal operation required to execute particular function.

Interface – makes interface between external device and DFPAU-DP internal 32-bit modules. It contains data, control and status registers. It can be configured to work with 8-, 16- and 32-bit processors.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	3660	79 MHz
CYCLONE-II	-6	3630	71 MHz
STRATIX	-5	3660	84 MHz
STRATIX-II	-3	2800	110 MHz

Core performance in ALTERA® devices

DFPAU-DP floating point instructions performance has been compared to standard C library functions delivered with every commercial C compiler. Each program was executed in the same system environments. Number of clock periods were measured between input data loading into work registers and output result storing after operation.

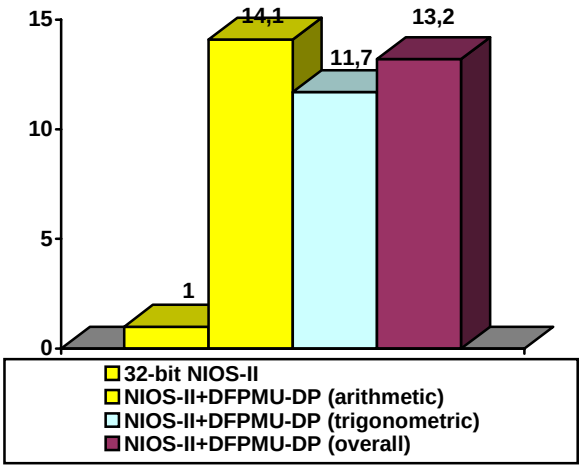
The results are placed in table below. Improvement has been computed as number of: (NIOS-II CLK) divided by (NIOS-II+DFPAU-DP CLK), required to execute particular instruction.

IEEE-754 FP Instruction	Improvement
Addition	12.0
Subtraction	11.7
Multiplication	10.6
Division	15.0
Square Root	21.5
Sine	11.8
Cosine	10.3
Tangent	10.1
Arcs Tangent	14.7
Average speed improvement:	**13.1**

More details are available in core documentation.

The following table gives a survey about the 32-bit NIOS-II+DFPAU-DP performance compared to 32-bit NIOS-II.

Device	Improvement
NIOS-II	1.0
NIOS-II+DFPAU (arithmetic)	14.1
NIOS-II+DFPAU (trigonometric)	11.7
NIOS-II+DFPAU (overall)	**13.1**



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