10-Channel Serial-Input Latched Display Driver

Features

- High output voltage 80V
- High speed 5MHz @ 5.0V_{DD}
- Low power I_{BB} ≤ 0.1mA (all high)
- Active pull down 100µA min
- Output source current 100mA at 60V V_{PP}
- Each device drives 10 lines
- High-speed serially-shifted data input
- 5.0V CMOS-compatible inputs
- Latches on all driver outputs
- Pin-compatible replacement for UCN5810A and TL4810A, TL4810B

Applications

- High speed dot matrix print head driver
- VFD (vacuum fluorescent display) driver

Ordering Information

Device	Package Options	
	20-J Lead PLCC	20-Lead SOW
HV6810	HV6810PJ-G	HV6810WG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
Logic supply voltage, V_{DD} (1)	7.5V
Driver supply voltage, V_{BB} (1)	90V
Output voltage(1)	90V
Input voltage(1)	-0.3V to V_{DD}+ 0.3V
Continuous total power dissipation at 25°C free-air temperature 20-J Lead PLCC (PJ) 20-Lead SOW (WG)	 1000mW(2) 1000mW(2)
Operating temperature range	-45°C +85°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

(1) All voltages are referenced to V_{SS}.

(2) For operation above 25°C ambient derate linearly to 85°C at 16.7mW/°C.

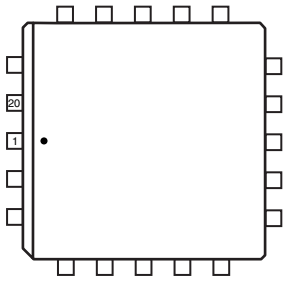
General Description

The HV6810 is a monolithic integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large displays.

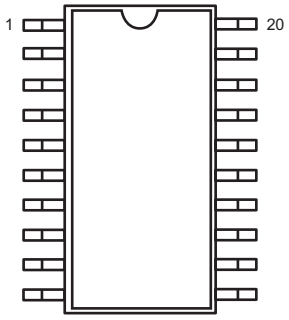
A 10-bit data word is serially loaded into the shift register on the positive-going transition of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high, and is latched when the latch enable is low. When the blanking input is high, all of the outputs are low.

Outputs are structures formed by double-diffused MOS (DMOS) transistors with output voltage ratings of 80V and 25mA source-current capability. All inputs are compatible with CMOS levels.

Pin Configurations



20-J Lead PLCC (PJ)
(top view)

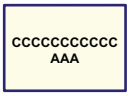


20-Lead SOW (WG)
(top view)

Product Marking

Top Marking

Bottom Marking

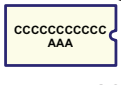


YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
——— = "Green" Packaging
**May be part of top marking*

20-J Lead PLCC (PJ)

Top Marking

Bottom Marking



YY = Year Sealed
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20-Lead SOW (WG)

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	4.5	-	5.5	V	---
V_{BB}	Supply voltage	20	-	80	V	---
V_{SS}	Supply voltage	-	0	-	V	---
V_{IH}	High-level input voltage (for V_{DD} = 5.0V)	3.5	-	5.3	V	---
V_{IL}	Low-level input voltage	-0.3	-	0.8	V	---
I_{OH}	Continuous high-level Q output current	-25	-	-	mA	---
f_{CLK}	Clock frequency	-	-	5.0	MHz	---
T_A	Operating ambient temperature	-40	-	+85	°C	---

Power-Up / Power-Down Sequence

Step	Description
1	Connect ground V_{SS}
2	Apply V_{DD}
3	Set all inputs (Data, CLK, Enable, etc.) to a known state
4	Apply V_{BB}
5	The V_{BB} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics

(V_{DD} = 5V±10%, V_{BB} = 60V, V_{SS} = 0, T_A = 25°C unless otherwise noted)

Sym	Parameter		Min	Typ	Max	Units	Conditions
V_{OH}	High level output voltage	Q outputs	57.5	58	-	V	I_{OH} = 25mA
		Serial output	4.0	4.5	-		V_{DD} = 4.5V, I_{OL} = -100µA
V_{OL}	Low level output voltage	Q outputs	-	0.15	1.0	V	I_{OH} = 100µA, blanking input at V_{DD}
		Serial output	-	0.05	0.1		V_{DD} = 4.5V, I_{OL} = 100µA
I_{OL}	Low level Q output current (pull-down current)		60	80	-	µA	T_A = Max, V_{OL} = 0.7V
$I_{O(OFF)}$	Off-state output current		-	-1.0	-15	µA	V_O = 0, Blanking input T_A = Max at V_{DD}
I_H	High level input current		-		1.0	µA	V_I = V_{DD}
I_{DD}	Supply current from V_{DD} (standby)		-	10	50	µA	All inputs at 0V, one Q output high
			-	10	50		All inputs at 0V, all Q outputs low
I_{BB}	Supply current from V_{BB}		-	0.05	0.1	mA	All outputs low, all Q outputs open
			-	0.05	0.1		All outputs high, all Q outputs open

* *All typical values are at T_A = 25°C except for I_O.*

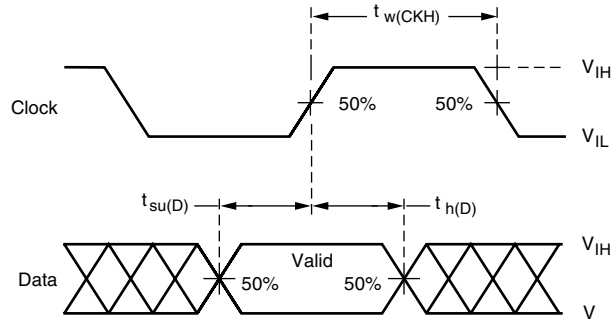
AC Electrical Characteristics

(Timing requirements over recommended operating conditions)

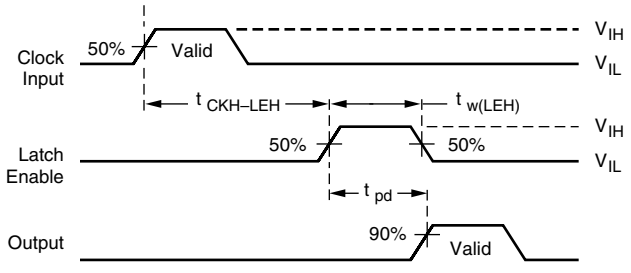
Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{W(CKH)}$	Pulse duration, clock high	100	-	-	ns	---
$t_{W(LEH)}$	Pulse duration, latch enable high	100	-	-	ns	---
$t_{SU(D)}$	Setup time, data before clock	50	-	-	ns	---
$t_{H(D)}$	Hold time, data after clock	50	-	-	ns	---
$t_{CKH-LEH}$	Delay time, clock to latch enable high	50	-	-	ns	---
t_{PD} *	Propagation delay time, latch enable to output	-	0.3	-	ns	---

* *Switching characteristics, V_{BB} = 60V, T_A = 25°C*

Switching Waveforms

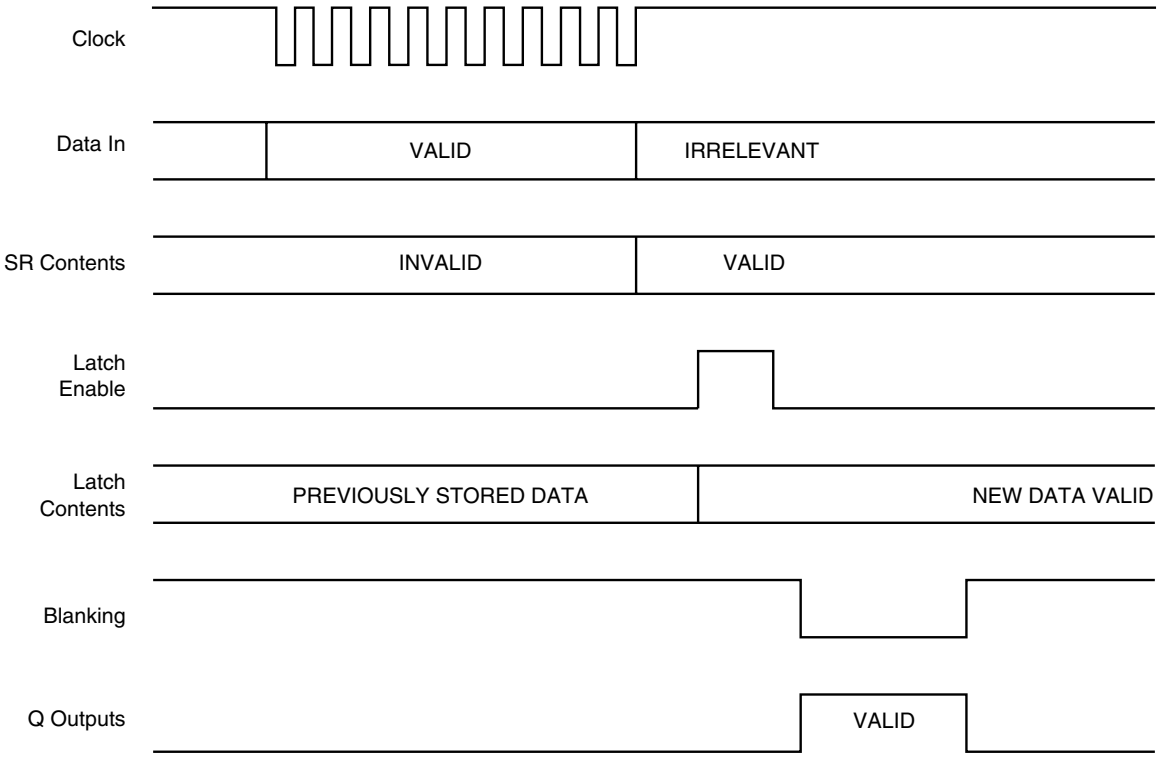


Input Timing

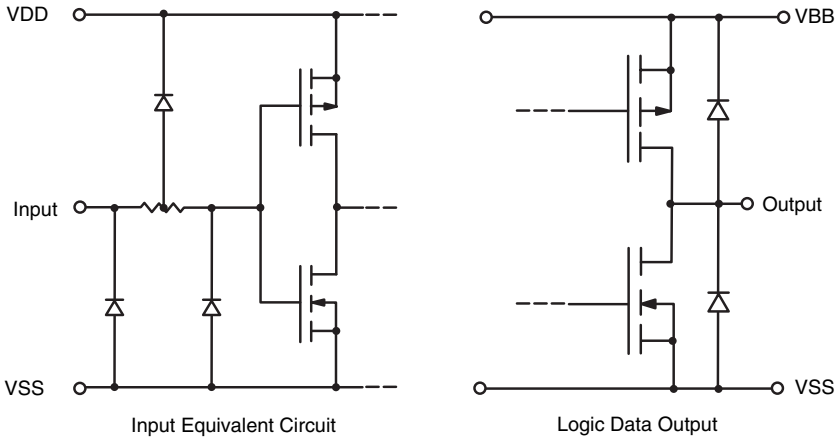


Output Switching Times

Timing Diagram



Input and Output Equivalent Circuits

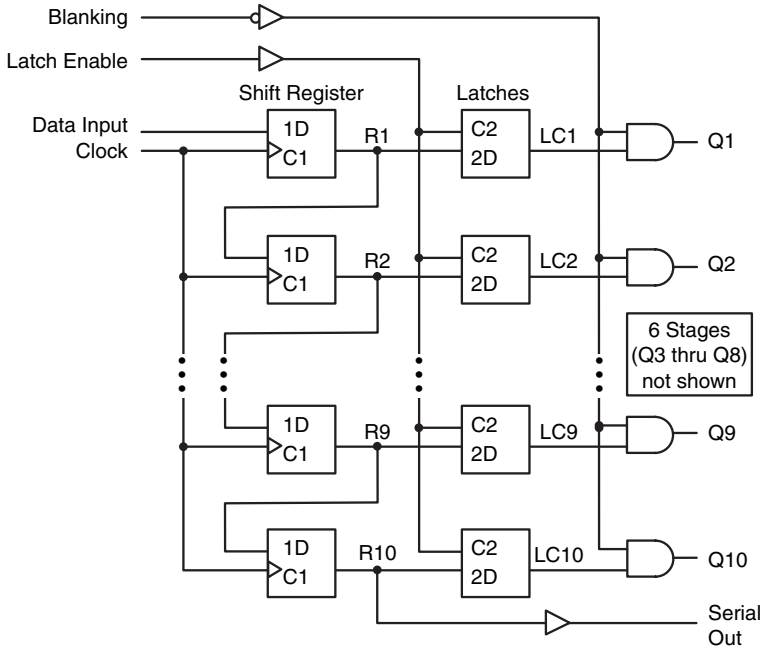


Input Equivalent Circuit

Logic Data Output

Functional Block Diagram

Logic Diagram (positive logic)



Function Table

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots\ I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots\ I_{N-1}\ I_N$	Blanking Input	Output Contents $I_1\ I_2\ I_3\ \ldots\ I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2 \ldots R_{N-2}\ R_{N-1}$	R_{N-1}	---	---	---	---
L	⎍	$L\ R_1\ R_2 \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	⎎	$R_1\ R_2\ R_3 \ldots R_{N-1}\ R_N$	R_N				
---	---	X X X ... X X	X	L	$R_1\ R_2\ R_3 \ldots R_{N-1}\ R_N$	---	
		$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$
		---	---	---	X X X ... X X	H	L L L ... L L

Pin Descriptions

HV6810 20-J Lead PLCC (PJ)

Pin	Function	Description
1	Q8	High voltage output.
2	Q7	
3	Q6	
4	CLOCK	Input data are shifted into the data shift register on the thepostive edge of the clock.
5	N/C	No connection.
6	VSS	Usually V_{SS} = 0, ground connection.
7	VDD	Low voltage power supply.
8	LE (STROBE)	When LE is high, data is transferred from data shift register to the Q output latch. When LE is low, data is latched into data latches and new data can be clocked into the shift register.
9	Q5	High voltage output.
10	Q4	
11	Q3	
12	Q2	
13	Q1	
14	BLANKING	When blanking is low, all Q's are forced to a high state, regardless of data in each channel. When OL is low, all Q's are forced to a low state, regardless of data in each channel.
15	DATA IN	Input data for the input shift register.
16	N/C	No connection.
17	VBB	High voltage power supply.
18	SERIAL DATA OUT	Output data from the shift register.
19	Q10	High voltage output.
20	Q9	

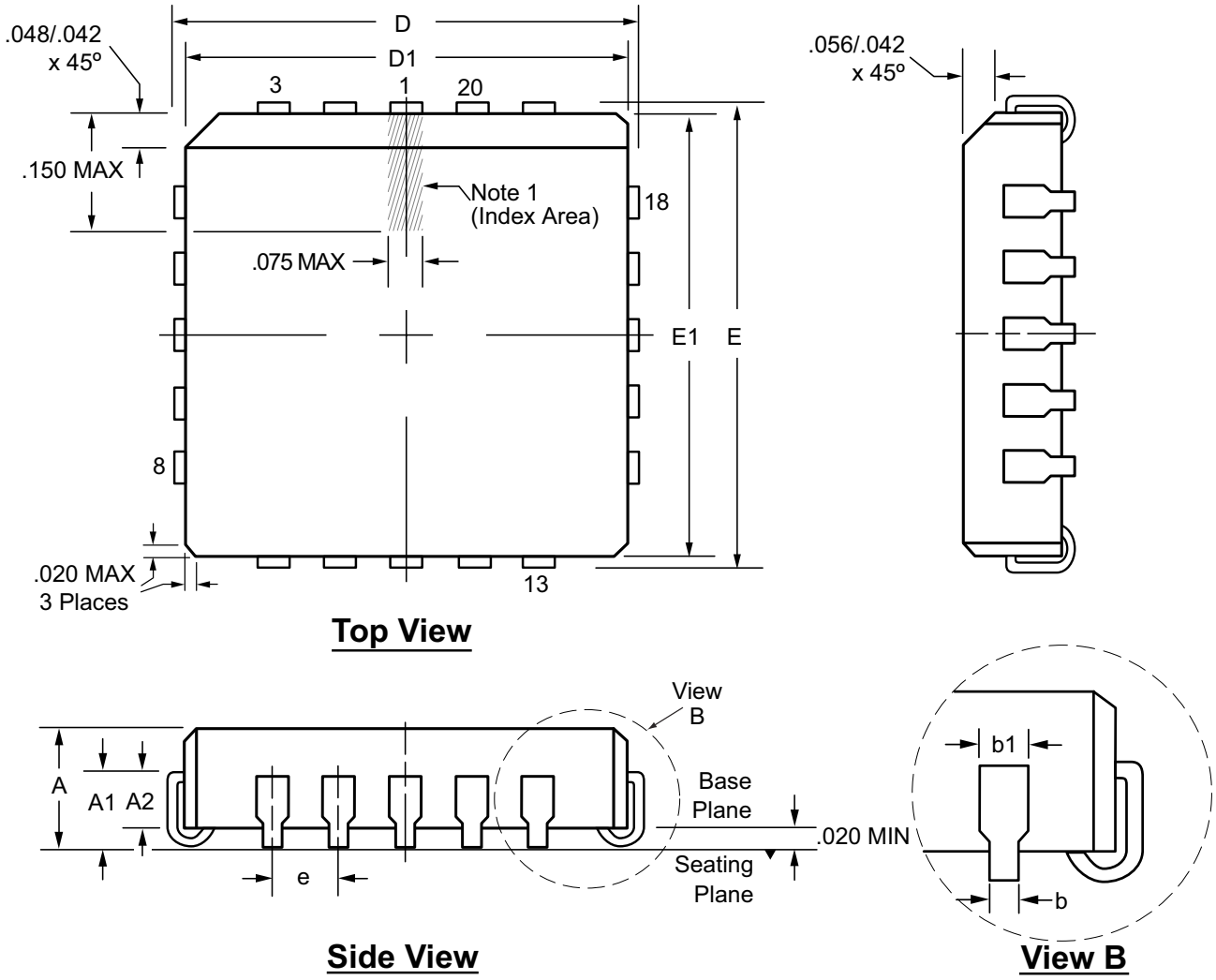
Pin Descriptions

HV6810 20-Lead SOW (WG)

Pin	Function	
1	Q8	High voltage output.
2	Q7	
3	Q6	
4	CLOCK	Input data are shifted into the data shift register on the thepostive edge of the clock.
5	VSS	Usually V_{SS} = 0, ground connection.
6	N/C	No connection.
7	VDD	Low voltage power supply.
8	LE (STROBE)	When LE is high, data is transferred from data shift register to the Q output latch. When LE is low, data is latched into data latches and new data can be clocked into the shift register
9	Q5	High voltage output.
10	Q4	
11	Q3	
12	Q2	
13	Q1	
14	BLANKING	When blanking is low, all Q's are forced to a high state, regardless of data in each channel. When OL is low, all Q's are forced to a low state, regardless of data in each channel.
15	DATA IN	Input data for the input shift register.
16	VBB	High voltage power supply.
17	SERIAL DATA OUT	Output data from the shift register.
18	N/C	No connection.
19	Q10	High voltage output.
20	Q9	

20-J Lead PLCC Package Outline (PJ)

.353x.353in body, .180in height (max.), .050in pitch



Note 1:

A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

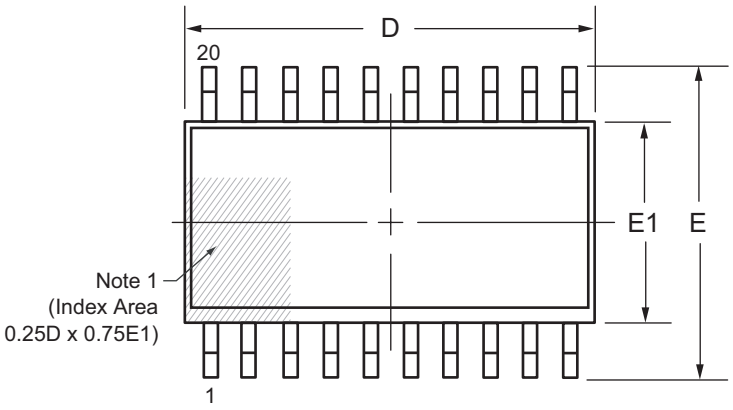
Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.385	.350	.385	.350	.050 BSC
	NOM	.172	.105	-	-	-	.390	.353	.390	.353	
	MAX	.180	.120	.083	.021	.032	.395	.356	.395	.356	

JEDEC Registration MS-018, Variation AA, Issue A, June, 1993.

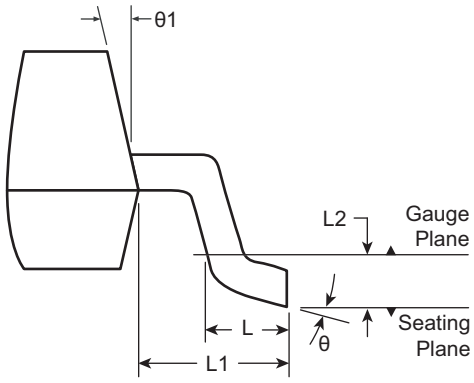
Drawings not to scale.

20-Lead SOW (Wide Body) Package Outline (WG)

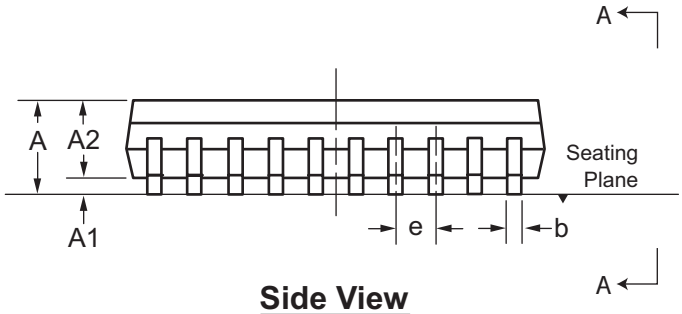
12.80x7.50mm body, 2.65mm height (max), 1.27mm pitch



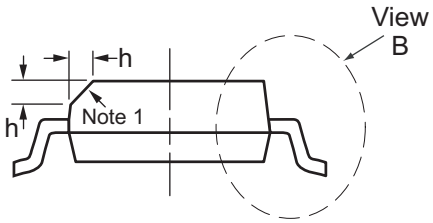
Top View



View B



Side View



View A-A

Note 1:

This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15	0.10	2.05	0.31	12.60	9.97	7.40	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	12.80	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55	0.51	13.00	10.63	7.60		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AC, Issue E, Sep. 2005.
Drawings not to scale.

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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