Genesys Logic, Inc.

GL800HT25

USB 2.0 UTMI
Compliant Transceiver IP Core

Datasheet

Revision 1.30

Nov. 28, 2002

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Revision History

Revision	Date	Description
1.0	02/22/2002	First draft release
1.1	06/21/2002	1. Remove Optional Output Signals in Sec.VII. 2. Add Testing Circuit in Sec.IX. 3. Add IX.6 application circuit for tester.
1.2	07/10/2002	Modify VII.2 Interface port description. (1) Pad descriptions are separated from interface signals. (2) Use the same pad names and pad order as layout. (3) Add description for bonding options.
1.21	07/16/2002	1. Insert table for operation mode in Sec IX.2 2. Add some description on analogue test.
1.22	07/29/2002	1. Insert table for pin description while in testing. 2. Add some description on analogue test. 3. More description on layout guide.
1.23	08/02/2002	1. Revert Figure 7.3 horizontally. 2. CLKOUT -> CLK30.
1.24	08/12/2002	Re-organize layout recommendation
1.30	11/28/2002	Modify pin description of DVDD1 of test sample.

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CHAPTER 1 GENERAL DESCRIPTION

GL800HT25 is a high performance USB 2.0 Transceiver compliant with the UTMI (USB 2.0 Transceiver Macrocell Interface) Specification proposed by Intel. The UTMI specification defines a standard interface to USB 2.0 high-speed transceivers that enables common design across prototype and production implementations.

The GL800HT25 integrates high-speed, mixed-signal circuitry to serve as the interface between the high performance USB serial bus and the 16-bit SIE bus. The transceiver is controlled by input signals from the SIE bus, which is synchronized with the 30MHz clock output. The UTMI transceiver handles the low level USB protocol and signaling. This includes features such as: data serialization and deserialization, bit stuffing and clock recovery and synchronization. The primary focus of the UTMI transceiver is to shift the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

To eliminate the difficult high-speed, mixed-signal USB 2.0 logic design for system and peripheral developers, the GL800HT25 with standard UTMI and 40X improvement in data rate can be easily adapted for implementation of USB 2.0 high speed compliant design of widely applications, including scanners, printers, portable storage, external CD-ROM / CD-RW / DVD-ROM, flash card readers, and PC cameras. The IP block now is certified and available on the 0.35μm UMC standard CMOS process; and it is also scheduled for 0.25μm TSMC standard CMOS process in 3Q'02.

CHAPTER 2 FEATURES

- Complies with Universal Serial Bus Specification Rev. 2.0.
- Complies with USB 2.0 Transceiver Macrocell Interface (UTMI) Specification.
- Supports 480 Mbit/s "High Speed" (HS) / 12 Mbit/s “Full Speed” (FS), FS Only serial data transmission rates.
- 16 bit Bi-directional Serial Interface Engine (SIE) bus.
- SYNC/EOP generation and checking.
- Supports “Chirp” for High Speed recognition.
- Data and clock recovery from serial stream on the USB.
- Bit-stuffing / unstuffing; Bit stuff error detection.
- Holding registers to stage transmit and receive data.
- Supports Reset and Suspend.
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks.
- Available in 48 pin LQFP package or IP macrocell on the 0.35µm UMC / 0.25µm TSMC standard CMOS processes.

CHAPTER 3 BLOCK DIAGRAM

3.1 System Configuration

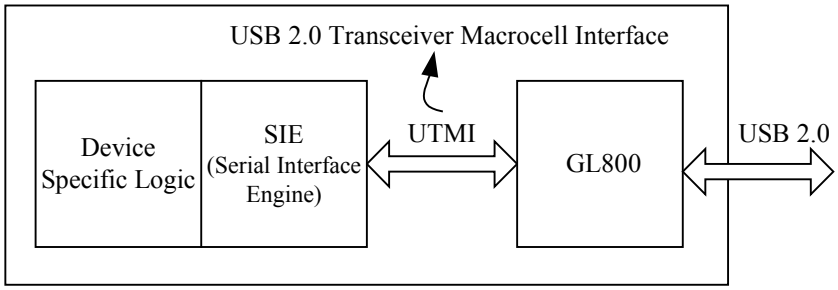


Figure 3.1 - System Diagram

1. GL800HT25

The USB 2.0 UTMI Transceiver, which handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

2. Serial Interface Engine

The Serial Interface Engine can be further sub-divided into 2 types of sub-blocks; the SIE control logic and the Endpoint logic. The SIE control logic contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions. The Endpoint logic contains the endpoint specific logic: endpoint number recognition, FIFOs and FIFO control, etc.

SIE logic module can be developed by peripheral vendors or purchased from IP vendors. The standardization of the UTMI allows multiple sources of SIE logic to connect with GL800HT25 to implement the USB 2.0 High-Speed design.

3. Device Specific Logic

This block is the glue that ties the USB interface to the specific application of the device.

3.2 Block Diagram

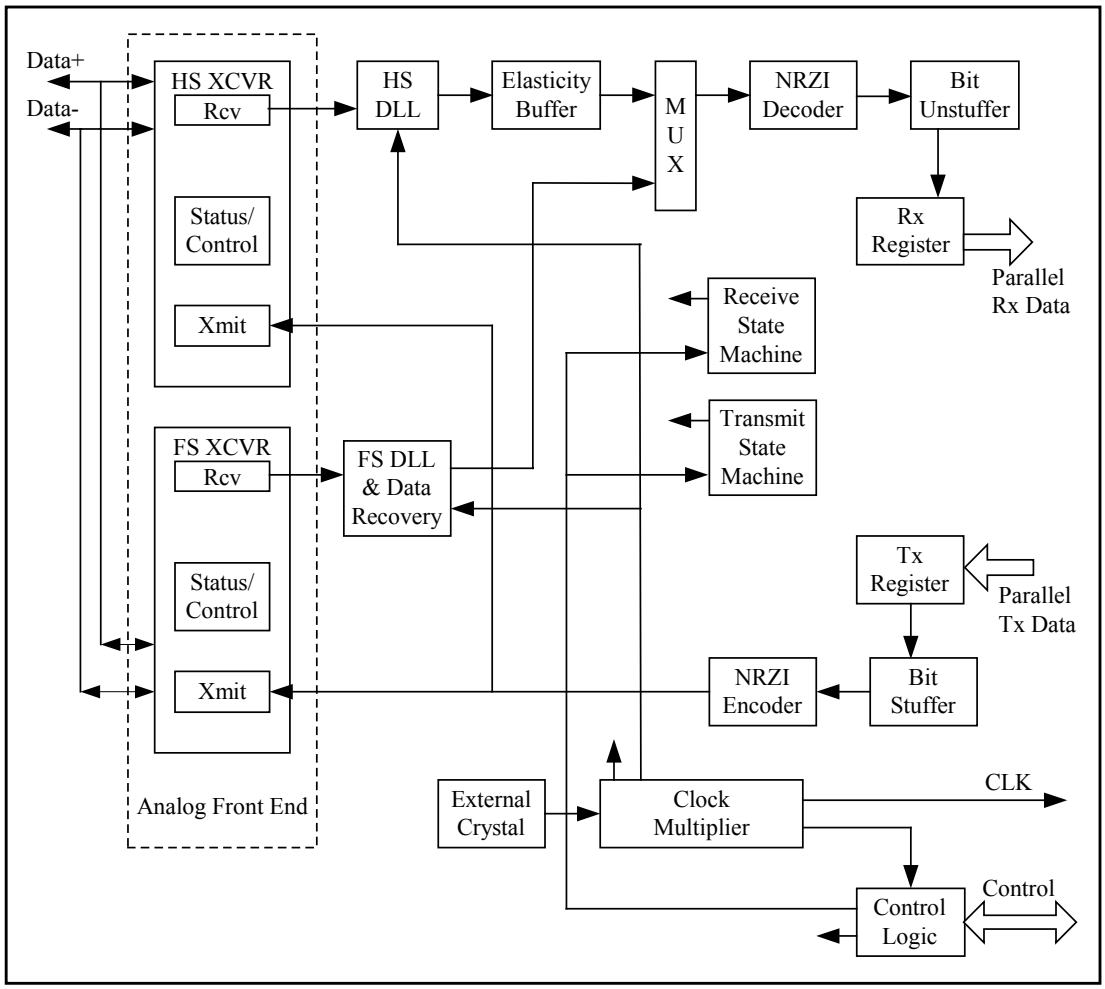


Figure 3.2 - Block Diagram

1. HS XCVR

HS XCVR contains the low-level analog circuitry required to physically interface USB 2.0 signaling to the USB DP/DM signal lines.

2. FS XCVR

FS XCVR includes the logic necessary to send and receive the FS data on USB.

3. Clock Multiplier

Clock Multiplier generates the internal clocks for the GL800HT25 USB 2.0 Transceiver and the CLK30 signal. All data transfer signals are synchronized with the CLK30 signal.

In HS mode there is one clock cycle per byte time. The frequency of clock does not change when the UTMI is switched between HS to FS modes. In FS mode there are 5 clock cycles per FS bit time, typically 40 clock cycles per FS byte time. If a received byte contains a stuffed bit then the byte boundary can be stretched to 45 clock cycles, and two stuffed bits would result in a 50 clock delay between bytes.

4. HS DLL (High Speed Delay Line PLL)

DLL extracts clock and data from the data received over the USB 2.0 interface for reception by the Receive Deserializer. The data output from the DLL is synchronous with the local clock.

5. Elasticity Buffer

Elasticity Buffer is used to compensate for difference between transmitting and receiving clocks. The USB specification defines a maximum clock error of +/- 500 ppm. When the error is calculated over the maximum packet size up to +/- 12 bits of drift can occur. The elasticity buffer is filled to a threshold prior to enabling the remainder of the down stream receive logic.

Overview and underflow conditions detected in the elasticity buffer can be reported with the **RXERR** signal.

6. Mux

The MUX block allows the data from the HS or FS receivers to be routed to the shared receive logic. The state of the Mux is determined by the **FSPEED** input.

7. NRZI Decoder

The NRZI Decoder is compliant to standard USB 1.X specification, and it can operate at FS and HS data rates.

8. Bit Unstuffer

The Bit Unstuffer is compliant to standard USB 1.X specification, and it can operate at FS and HS data rates. The bit unstuffer is a state machine, which strips a stuffed 0 bit from the data stream and detects bit stuff errors. In FS mode bit stuff errors asserts the **RXERR** signal. In HS mode bit stuff errors are used to generate the EOP signal so the **RXERR** signal is not asserted.

9. Rx Register

Rx Register is in charge of converting serial data received from the USB to parallel data.

10. Receive State Machine

The behavior of the Receive State Machine is described at Chapter 6, Function Description.

11. NRZI Encoder

The NRZI Encoder is compliant to standard USB 1.X specification, and it can operate at FS and HS data rates.

12. Bit Stuffer

Bit Stuffer is used by insert a zero after every six consecutive ones in the data stream before the data is NRZI encoded in order to ensure adequate signal transitions. Bit stuffing is enabled beginning with the SYNC Pattern and through the entire transmission. The data “one” that ends the SYNC Pattern is counted as the first one in a sequence.

In FS mode bit stuffing by the transmitter is always enforced, without exception. If required by the bit stuffing rules, a zero bit is inserted even after the last bit before the TXVLD signal is negated.

After 8 bits are stuffed into the USB data stream TXRDY is negated for one byte time to hold up the data stream on the Data bus.

13. Tx Register

Tx Register is in charge of reading parallel data from the parallel application bus interface upon command and serializing for transmission over USB.

14. Transmit State Machine

The behavior of the Transmit State Machine is described at Chapter 6, Function Description.

CHAPTER 4 PIN ASSIGNMENT

4.1 Pinouts

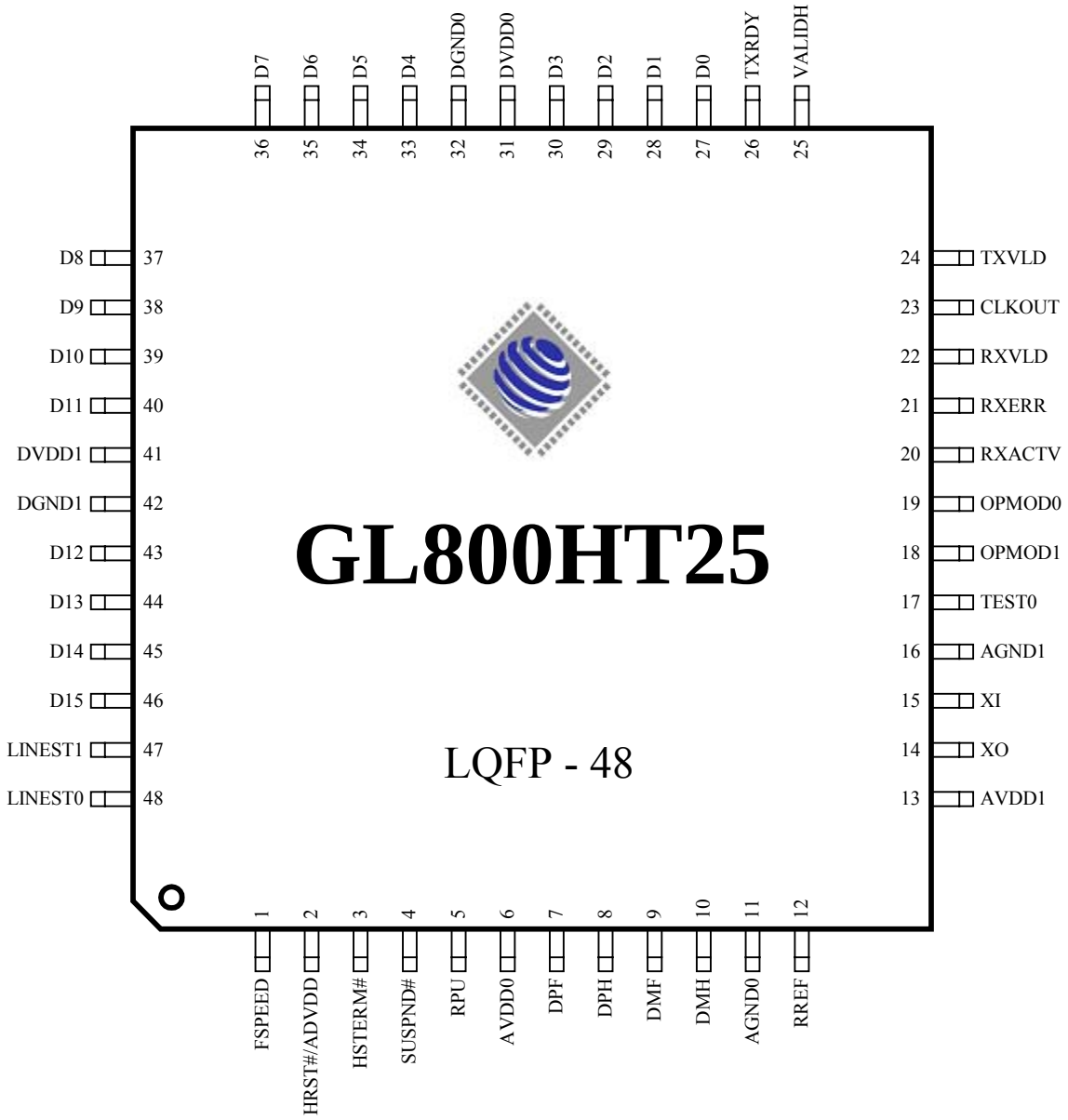


Figure 4.1 - Pinout Diagram

4.2 Pin List

Table 4.1 - Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	FSPEED	I	13	AVDD1	P	25	VALIDH	B	37	D8	B
2	HRST#	I	148	XO	B	26	TXRDY	O	38	D9	B
3	HSTERM#	I	15	XI	I	27	D0	B	39	D10	B
4	SUSPND#	I	16	AGND1	P	28	D1	B	40	D11	B
5	RPU	-	17	TEST0	I	29	D2	B	41	DVDD1	P
6	AVDD0	P	18	OPMOD1	I	30	D3	B	42	DGND1	P
7	DPF	B	19	OPMOD0	I	31	DVDD0	P	43	D12	B
8	DPH	B	20	RXACTV	O	32	DGND0	P	44	D13	B
9	DMF	B	21	RXERR	O	33	D4	B	45	D14	B
10	DMH	B	22	RXVLD	O	34	D5	B	46	D15	B
11	AGND0	P	23	CLKOUT	O	35	D6	B	47	LINEST1	O
12	RREF	-	24	TXVLD	I	36	D7	B	48	LINEST2	O

4.3 Pin Descriptions

Table 4.2 - Pin Descriptions

Pin Name	Pin#	Type	Description
FSPEED	1	I (pu)	Transceiver Select. This signal selects between the FS and HS transceivers: 0: High Speed transceiver enabled 1: Full Speed transceiver enabled
HRST# / ADVDD	2	I (pu)	UMC 0.35um sample: Reset. Chip reset Input, active low. This signal is used to reset all state machines in the GL800HT25. TSMC 0.25um sample: this pin should be digital 2.5V power for transceiver.
HSTERM#	3	I (pu)	Termination Select. HS termination enable, active low
SUSPND#	4	I (pd)	Suspend mode enable, active low. This signal places the GL800HT25 in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation. While suspended, HSTERM# must always be disabled (FS Mode) to ensure that the 1.5K pull-up on DP remains powered.
RPU	5	-	3.3V Pull up control for DPF
AVDD0~1	6,13	P	Positive analog supply (3.3V)
DPF	7	B	Positive USB differential data (Full Speed)
DPH	8	B	Positive USB differential data (High Speed)
DMF	9	B	Negative USB Differential Data (Full Speed)

DMH	10	B	Negative USB Differential Data (High Speed)
AGND0~1	11,16	P	Analog ground (0V)
RREF	12	-	510 Ω reference resistor input
XO	14	B	Crystal output
XI	15	I	12MHz crystal/oscillator input
TEST0	17	I (pd)	Test mode enable
OPMOD1	18	I (pu)	Operational mode. These signals select between various operational modes: [1] [0] Description 0 0 0: Normal Operation 0 1 1: Non-Driving 1 0 2: Disable Bit Stuffing and NRZI encoding 1 1 3: Reserved
OPMOD0	19	I (pd)	
RXACTV	20	O	Receive Active, active high. Indicates that the receive state machine has detected SYNC and is active. RXACTV is negated after a Bit Stuff Error or an EOP is detected. In HS mode, RXACTV must be negated no less than 3 and no more than 8 CLKs after an Idle state is detected on the USB. And RXACTV must be negated for at least 1 CLK between consecutive received packets. In FS/FS only modes, RXACTV must be negated no more than 2 CLKs after a FS Idle state is detected on the USB. And RXACTV must be negated for at least 4 CLKs between consecutive received packets.
RXERR	21	O	Receive Error, active high. 0: Indicates no error. 1: Indicates that a receive error has been detected. This output is clocked with the same timing as the Data lines and can occur at anytime during a transfer. If asserted, it will force the negation of RXVLD on the next rising edge of CLK30.
RXVLD	22	O	Receive Data Valid, active high. Indicates that the Data bus has valid data. The Rx Register is full and ready to be unloaded. The SIE is expected to latch the Data bus on the clock edge.
CLKOUT	23	O	Clock. This 30MHz clock output is used for clocking receive and transmit HS/FS 16-bit parallel data.
TXVLD	24	I	Transmit Valid, active high. Indicates that the Data bus is valid. The assertion of Transmit Valid initiates SYNC on the USB. The negation of Transmit Valid initiates EOP on the USB. In HS mode, the SYNC pattern must be asserted on the USB between 8 and 16 bit times after the assertion of TXVLD is detected by the Transmit State Machine. In FS/ FS only Modes, the SYNC pattern must be asserted on the USB no less than 1 CLK and no more than 5 CLKs after the assertion of TXVLD is detected by the Transmit State Machine.
VALIDH	25	B	Transmit/Receive Valid High, active high.
TXRDY	26	O	Transmit data ready, active high. If TXVLD is asserted, the SIE must always have data available for clocking in to the TX Register on the rising edge of CLK30. If TXVLD is true and TXRDY is asserted at the rising edge of CLK30, the GL800HT25 will load the data on the Data bus into the TX Register on the next rising edge of CLK30, at that time, SIE should immediately present the

			data for next transfer on the Data bus. If TXVLD is asserted and TXRDY is negated, the SIE must hold the previously asserted data on the Data bus. From the time TXVLD is negated, TXRDY is a don't care for the SIE.
D0~D15	27~30, 33~40, 43~46	B	Data bus 0~15
DVDD0	31	P	Positive digital supply (3.3V)
DVDD1	41	P	Positive digital supply UMC 0.35um sample : 3.3V TSMC 0.25um sample : 2.5V
DGND0~1	32,42	P	Digital ground (0V)
LINEST1	47	O	Line State. These signals reflect the current state of the single ended receivers. They are combinatorial until a "usable" CLK30 is available then they are synchronized to CLK30. They directly reflect the current state of the DP (LineState[0]) and DM (LineState[1]) signals: DM DP Description 0 1 0: SE0 0 1 1: 'J' State 1 0 2: 'K' State 1 1 3: SE1
LINEST0	48	O	

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 5 FUNCTIONAL DESCRIPTION

5.1 Transmit Operation

5.1.1 Transmit State Diagram

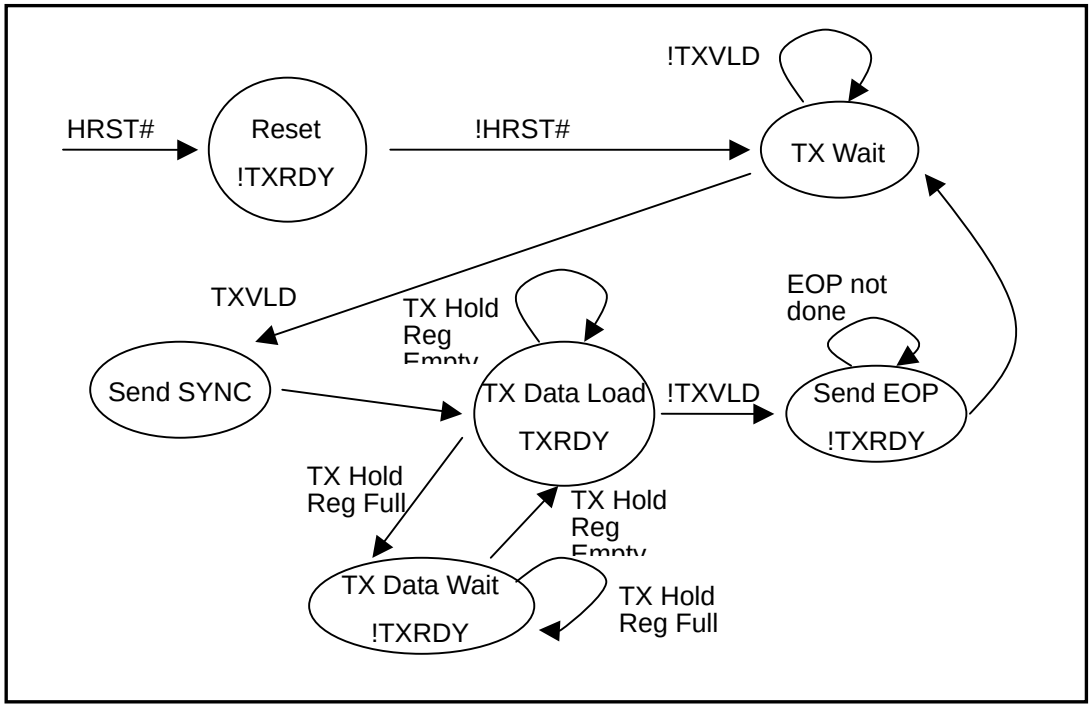


Figure 5.1 - Transmit State Diagram

- Transmit must be asserted to enable any transmissions.
- The SIE asserts TXVLD to begin a transmission.
- The SIE negates TXVLD to end a transmission.
- After the SIE asserts TXVLD it can assume that the transmission has started when it detects TXRDY asserted.
- The SIE assumes that the UTM has consumed a data byte if TXRDY and TXVLD are asserted.
- The SIE must have valid packet information (PID) asserted on the Data bus coincident with the assertion of TXVLD. Depending on the UTM implementation, TXRDY may be asserted by the Transmit State Machine as soon as one CLK after the assertion of TXVLD.
- TXVLD and TXRDY are sampled on the rising edge of CLK30.
- The Transmit State Machine does not automatically generate Packet ID's (PIDs) or CRC.
  When transmitting, the SIE is always expected to present a PID as the first byte of the data stream and if appropriate, CRC as the last bytes of the data stream.
- The SIE must use LINEST0/1 to verify a Bus Idle condition before asserting TXVLD in the TX Wait state.

5.1.2 Transmit Timing for Data Packet

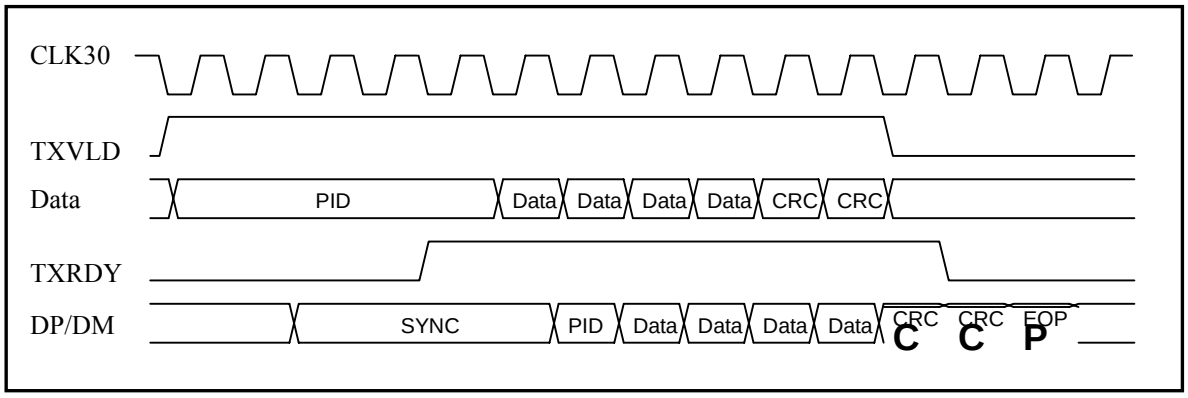


Figure 5.2 - Timing Diagram of Transmit for Data Packet

The SIE negates TXVLD to complete a packet. Once negated, the Transmit State Machine will never reassert TXRDY until after the EOP has been loaded into the Transmit Shift Register. Note that the UTM Transmit State Machine can be ready to start another package immediately, however the SIE must confirm to the minimum inter-packet delays identified in the USB 2.0 Specification.

5.2 Receive Operation

5.2.1 Receive State Diagram

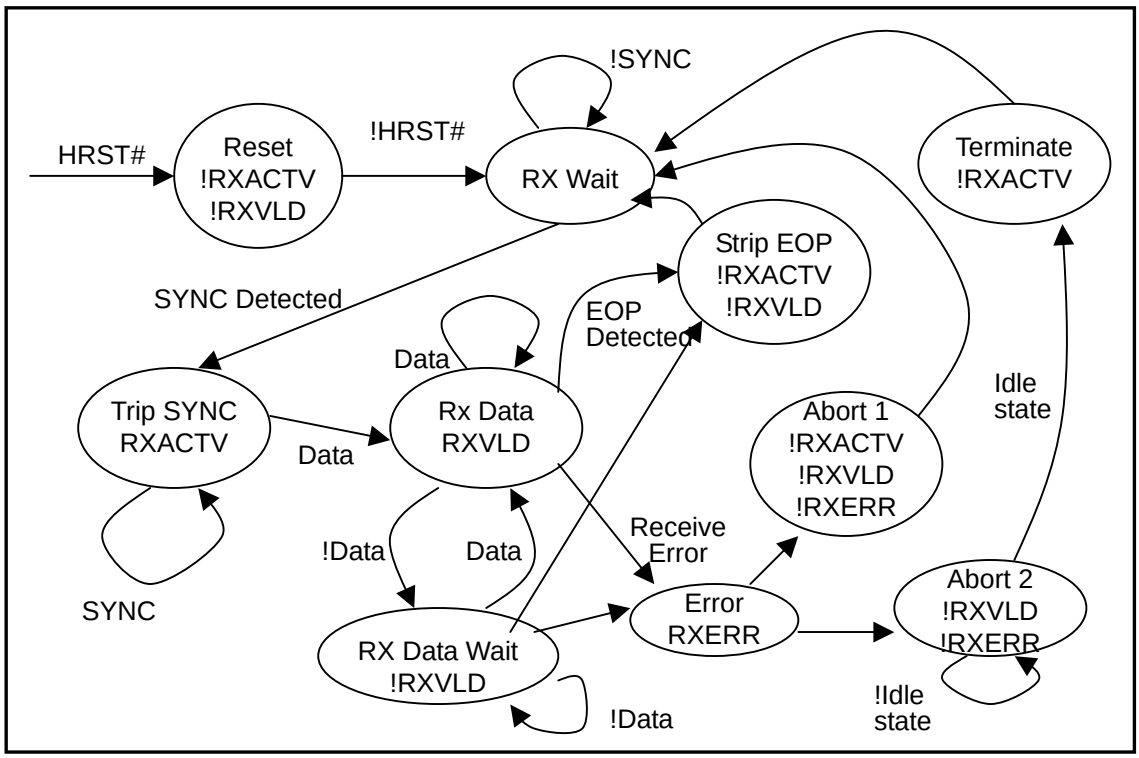


Figure 5.3 - Receive State Diagram

- RXACTV and RXVLD are sampled on the rising edge of CLK30.
- In the RX Wait state the receiver is always looking for SYNC.
- The Macrocell asserts RXACTV when SYNC is detected (Strip SYNC state).
- The Macrocell negates RXACTV when an EOP is detected (Strip EOP state).
- When RXACTV is asserted, RXVLD will be asserted if the RX Holding Register is full.
- RXVLD will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The SIE must be ready to consume a data byte if RXACTV and RXVLD are asserted (RX Data state).
- In FS mode, if a bit stuff error is detected then the Receive State Machine will negate RXACTV and RXVLD, and return to the RXWait state.

5.2.2 Receive Timing for Data Packet (with CRC-16)

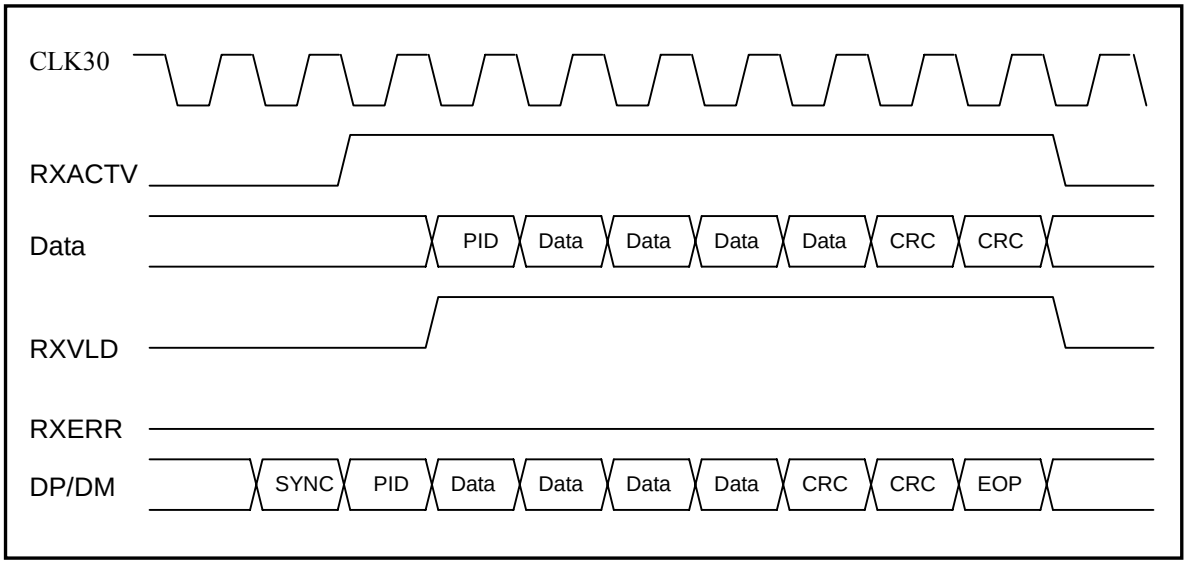


Figure 5.4 - Timing Diagram of Receive for Data Packet (with CRC-16)

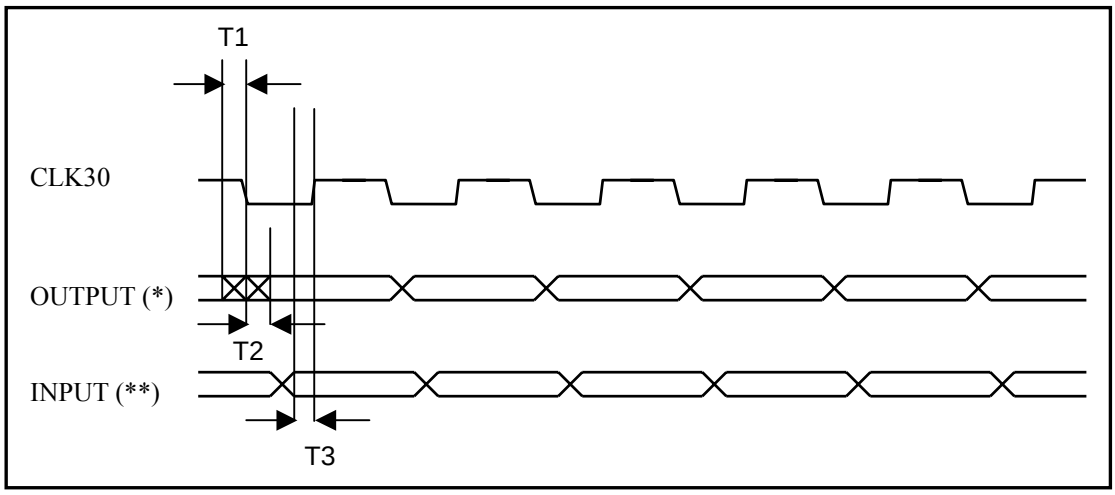
Note that the USB 2.0 transceiver does not decode Packet ID's (PIDs). They are passed to the SIE for decoding.

This timing example is in HS mode. When a HS/FS UTM is in FS mode there are approximately 40 clock cycles every byte time. The Receive State Machine assumes that the SIE captures the data on the data bus if RXACTV and RXVLD are asserted. In FS mode, RXVLD will only be asserted for one clock per byte time.

Note that the receive and transmit sections of the transceiver operate independently. The receiver will receive any packets on the USB. The transceiver does not identify whether the packet that it is receiving from the upstream or the downstream port. The SIE must ignore receive data while it is transmitting.

5.3 Timing Chart

5.3.1 CLK30 Rising and Falling Edge VS. Input/Output Signals



* Output signals includes TXRDY, RXACTV, RXERR, RXVLD, LINEST[1:0], D[15:0]
** Input signals includes TXVLD, VALIDH

Figure 5.5 - CLK30 Rising and Falling Edge VS. Input/Output Signals

	Max.	Min.	Unit
T1	8	-	ns
T2	3	-	ns
T3	-	8	ns

5.3.2 Relationship Between Mode Change and Other Input Signals

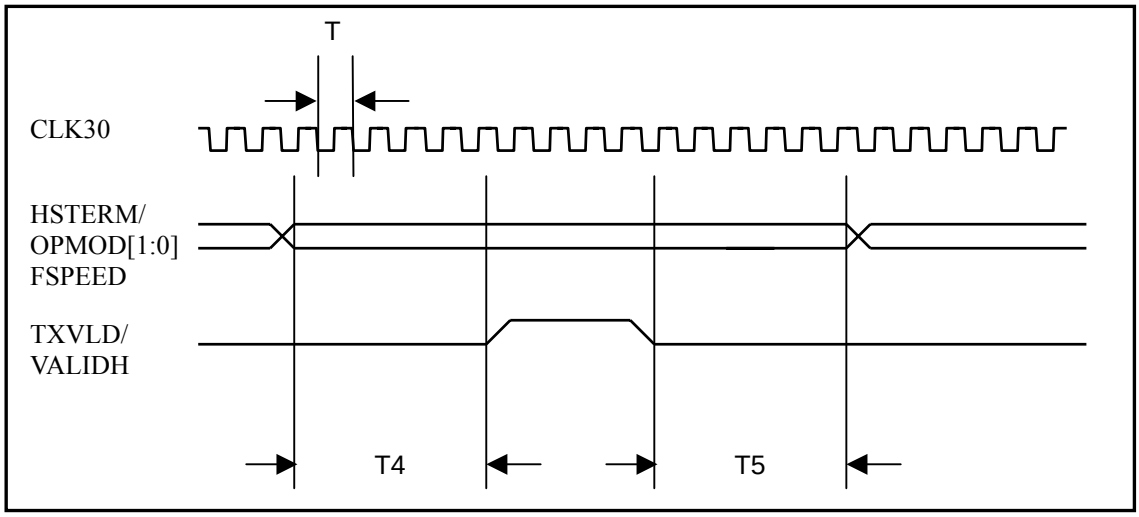
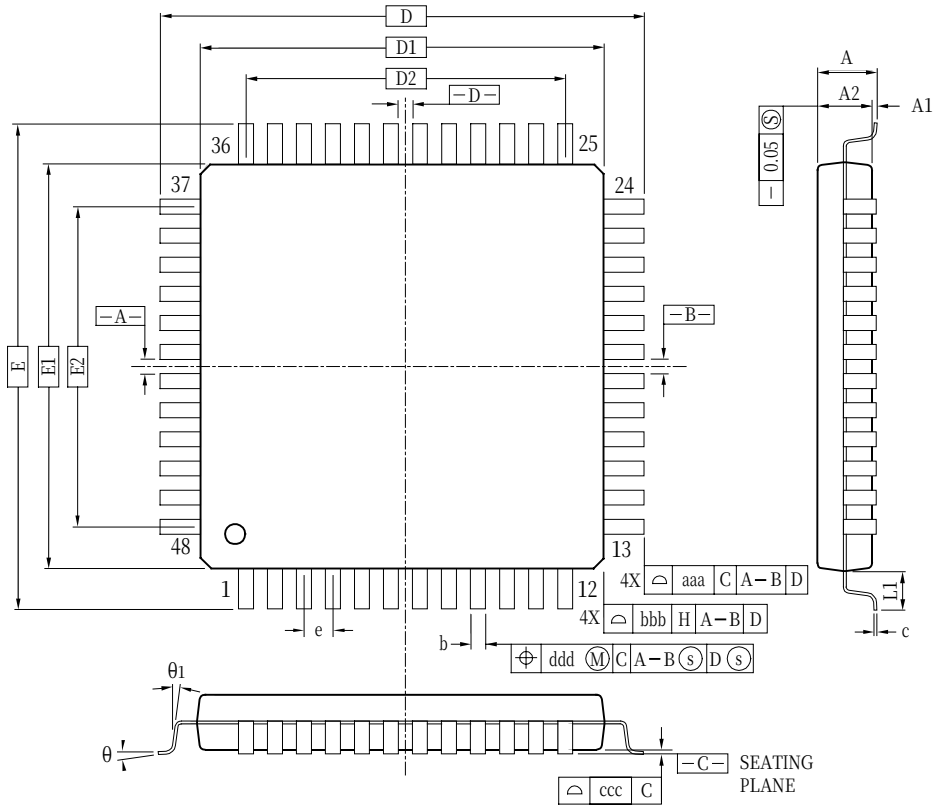
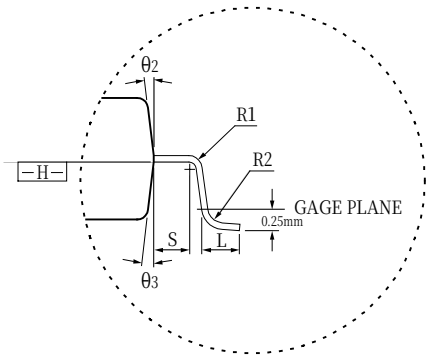


Figure 5.6 - Relationship Between Mode Change and Other Input Signals

	Max.	Min.
T4	-	4T
T5	-	4T

CHAPTER 6 PACKAGE DIMENSION





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 6.1 - GL800HT25 48 Pin LQFP Package

