ESS Technology, Inc.

ES6425
Digital Media Processor 2
Product Brief

DESCRIPTION

The ES6425 Digital Media Processor 2 (DMP2) is a high performance single-chip audio/video decoder for a wide series of applications such as networked or non-networked/flash memory media players. This second generation of Digital Media Processor has an enhanced performance engine to decode MPEG-4 video at D1 resolution with state-of-the-art progressive scan NTSC/PAL video encoder for brilliant and sharp, flicker-free output to the video display.

At the heart of the ES6425 is the ESS proprietary Programmable Multimedia Processor core consisting of 32-bit RISC and 64-bit DSP processors that enable simultaneous parallel execution of system commands and specialized multimedia decoding tasks. The ES6425 includes a memory controller which interfaces to 8-bit or 16-bit DRAM with up to 128-Mb capacity.

The ES6425 performs video processing to provide high-resolution display of MPEG-1, MPEG-2, and MPEG-4 videos and JPEG photos. The integrated NTSC/PAL TV-encoder provides composite, S-video, and YUV outputs. The ES6425 includes an On-Screen-Display (OSD) controller to provide a user friendly setup menu to enable or modify the various audio decoding and video display features. A CCIR656/601 digital video output port is also present.

The ES6425 also performs audio processing for Wave, MP3, AAC, Dolby® Digital, and WMA playback along with a 7-band graphic equalizer. The ES6425 has a multi-channel audio serial port compliant to I²S format for interfacing to an external audio DAC and ADC. An S/PDIF output port is also integrated for transmitting digital audio streams.

A 16-bit host interface present in the ES6425 connects to many different storage solutions including Compact Flash®, Smart Media™, xD-Picture Card™, and IDE hard drives. Similarly, a serial interface is built-in to interface to SD™, xD™, MultiMediaCard™, and Memory Stick™ devices.

The ES6425 is available in an industry-standard 208-pin Plastic Quad Flat Pack (PQFP) device package.

FEATURES

- Single-chip digital audio and video decoder and processor.
- MPEG-4 Advanced Simple Profile* at full screen D1 video playback (playability is dependent on memory card bandwidth).
- MPEG-2 video playback (playability is dependent on memory card bandwidth).
- MPEG-1 video playback.
- Motion JPEG playback.
- JPEG photo playback.
- Progressive JPEG photo playback.
- MP3 music playback.
- WMA music playback (Microsoft license required).
- Dolby® Digital decode (ES6425FDF only)
- AAC audio decode and playback.
- ESS Music Slideshow™.
- S/PDIF digital audio output.
- Integrated NTSC/PAL encoder with pixel adaptive de-interlacer and five 10-bit 54 MHz video DACs.
- High-quality progressive scan video output for flicker-free video display.
- Simultaneous Composite, S-Video, and YUV outputs.
- CCIR656/601 YUV 4:2:2 output.
- On-Screen-Display controller with 3-bit blending to provide 256 colors display.
- Integrated I²S serial port for up to 5.1 channel audio output and stereo input.
- Direct interface for IDE devices and flash memory cards including CF, MS, MS Pro, SD, xD, MMC, and SM.
- DRAM memory controller with interface to 8-bit or 16-bit SDRAM for up to 16 MB of memory.
- 16-bit SRAM interface for connecting to boot EPROM or flash memory.
- Lead-free leads using 98%-Sn/2%-Cu or 98%-Sn/2%-Bi.

ES6425 PINOUT DIAGRAM

The device pinout for the ES6425 is shown in Figure 1. The pound symbol (#) denotes an active-low signal.

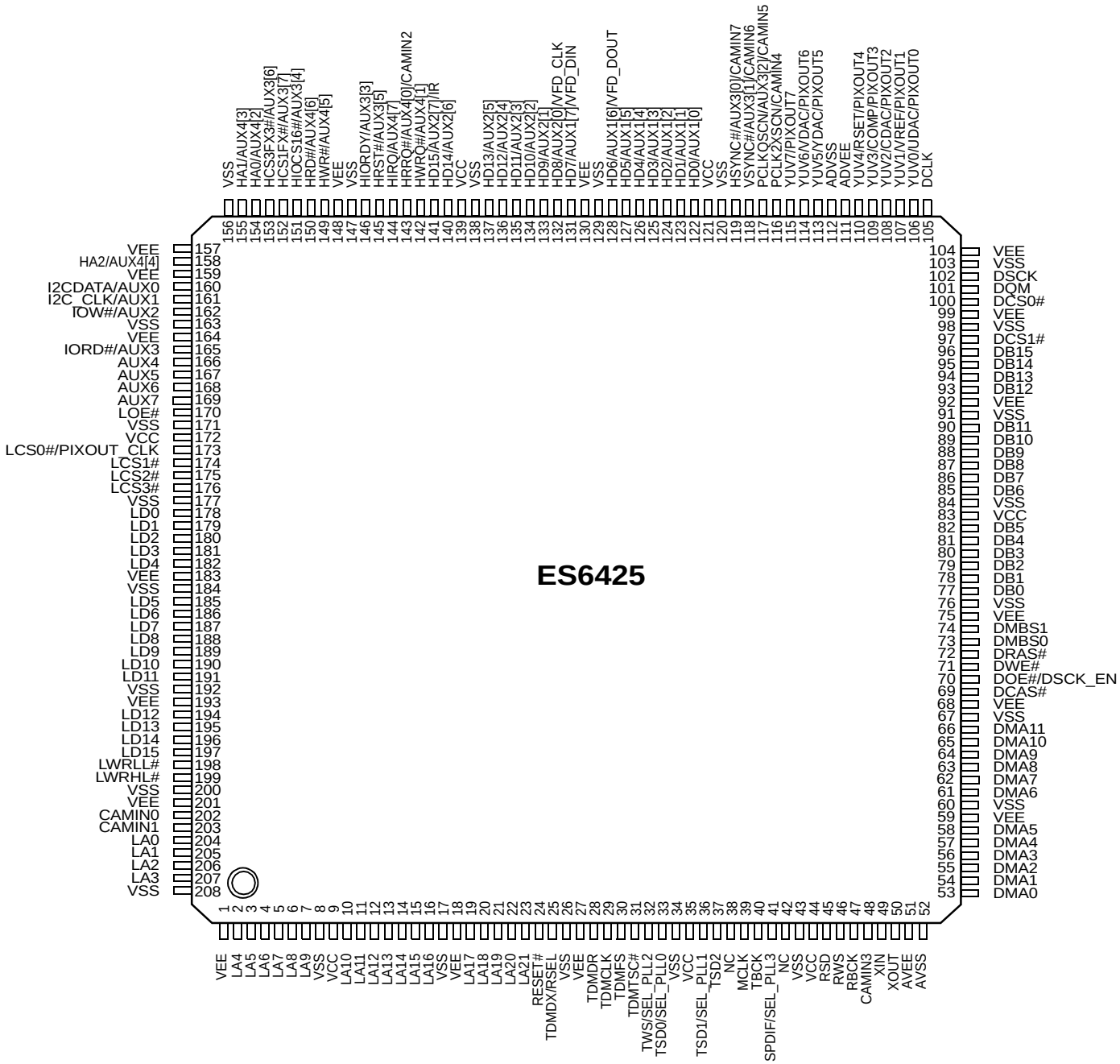

Figure 1 ES6425 Device Pinout

Note: (*) MPEG-4 Advanced Simple Profile without hardware Q-PEL and Global Motion Compensation (GMC).

ES6425 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES6425. The pound symbol (#) denotes an active-low signal.

Table 1 ES6425 Pin Description

<table>
<tr><th>Name</th><th>Pin Numbers</th><th>I/O</th><th>Definition</th></tr>
<tr><td>VEE</td><td>1,18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201</td><td>P</td><td>I/O power supply.</td></tr>
<tr><td>LA[21:0]</td><td>2-7, 10-16, 19-23, 204-207</td><td>O</td><td>RISC port address bus.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 60, 67, 76, 84, 91, 98, 103, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>G</td><td>Ground.</td></tr>
<tr><td>VCC</td><td>9, 35, 44, 83, 121, 139, 172</td><td>I</td><td>Core power supply.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input (active-low); (5V tolerant input).</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data.</td></tr>
<tr><td>RSEL</td><td>I</td><td>LCS3 ROM Boot Data Width Select. Strapped to VCC or ground via 4.7-kΩ resistor; read during reset.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>16-bit ROM</td></tr>
<tr><td>1</td><td>8-bit ROM</td></tr>
</table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data; (5V tolerant input).</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock; (5V tolerant input).</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync; (5V tolerant input).</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable (active-low).</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings. Pull up to VCC via 4.7-kΩ resistor for proper operation; read during reset.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DCLK x 4.5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DCLK x 5.0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DCLK x 4.0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>DCLK x 4.25</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DCLK x 4.75</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>DCLK x 5.5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DCLK x 6.0</td></tr>
</table></td></tr>
<tr><td>TSD0</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data output 0.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Pull up to VCC via 4.7-kΩ resistor for proper operation; read during reset.</td></tr>
</table>

Table 1 ES6425 Pin Description (Continued)

Name	Pin Numbers	I/O	Definition
TSD1	36	O	Audio transmit serial data output 1.
SEL_PLL1		I	Pull up to VCC via 4.7-kΩ resistor for proper operation; read during reset.
TSD2	37	O	Audio transmit serial data output 2. This pin must be pulled down to VSS via a 4.7-kΩ resistor for proper operation.
MCLK	39	I/O	Audio master clock for audio DAC.
TBCK	40	I/O	Audio transmit bit clock. TBCK is an input during reset and subsequently is programmed as an output via the AUDIOXMT register (addr 0x2000D00Ch, bit 4).
SPDIF	41	O	S/PDIF output.
SEL_PLL3		I	Pull down to ground via 4.7-kΩ resistor for proper operation; read during reset.
NC	38, 42	—	No connect.
RSD	45	I	Audio receive serial data; (5V tolerant input).
RWS	46	I	Audio receive frame sync; (5V tolerant input).
RBCK	47	I	Audio receive bit clock; (5V tolerant input).
CAMIN3	48	I	Camera and YUV input 3.
XIN	49	I	27-MHz crystal input.
XOUT	50	O	27-MHz crystal output.
AVEE	51	P	Analog power for PLL.
AVSS	52	G	Analog ground for PLL.
DMA[11:0]	53-58, 61-66	O	DRAM address bus.
DCAS#	69	O	DRAM column address strobe (active-low).
DOE#	70	O	DRAM output enable (active-low).
DSCK_EN		O	DRAM clock enable.
DWE#	71	O	DRAM write enable (active-low).
DRAS#	72	O	DRAM row address strobe (active-low).
DMBS0	73	O	SDRAM bank select 0.
DMBS1	74	O	SDRAM bank select 1.
DB[15:0]	77-82, 85-90, 93-96	I/O	DRAM data bus.
DCS[1:0]#	97,100	O	SDRAM chip select (active-low).
DQM	101	O	Data input/output mask.
DSCK	102	O	Output clock to SDRAM.
DCLK	105	I	Clock input to PLL; (5V tolerant input).

Table 1 ES6425 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Pin Numbers</th><th>I/O</th><th>Definition</th></tr>
<tr><td>UDAC</td><td>106</td><td>O</td><td>Video DAC output:
<table><tr><th>Value</th><th>DAC V (pin 114)</th><th>DAC Y (pin 113)</th><th>DAC C (pin 108)</th><th>DAC U (pin 106)</th></tr><tr><td>0</td><td>CVBS1</td><td>Y</td><td>N/A</td><td>C</td></tr><tr><td>1</td><td>CVBS1</td><td>Y</td><td>CVBS2</td><td>C</td></tr><tr><td>2</td><td>N/A</td><td>Y</td><td>N/A</td><td>C</td></tr><tr><td>3</td><td>CVBS1</td><td>N/A</td><td>CVBS2</td><td>N/A</td></tr><tr><td>4</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>5</td><td>CVBS1</td><td>Y</td><td>Pr</td><td>Pb</td></tr><tr><td>6</td><td>N/A</td><td>Y</td><td>Pr</td><td>Pb</td></tr><tr><td>7</td><td>SYNC</td><td>G</td><td>R</td><td>B</td></tr><tr><td>8</td><td>CHROMA</td><td>Y</td><td>Pr</td><td>Pb</td></tr><tr><td>9</td><td>CVBS1</td><td>G</td><td>R</td><td>B</td></tr><tr><td>10</td><td>CVBS1</td><td>G</td><td>B</td><td>R</td></tr><tr><td>11</td><td>SYNC</td><td>G</td><td>B</td><td>R</td></tr><tr><td>12</td><td>N/A</td><td>Y</td><td>Pb</td><td>Pr</td></tr><tr><td>13</td><td>CVBS1</td><td>Y</td><td>Pb</td><td>Pr</td></tr></table>
Y: Luma component for YUV and Y/C processing.
C: Chrominance signal for Y/C processing.
U: Chrominance component signal for YUV mode.
V: Chrominance component signal for YUV mode.</td></tr>
<tr><td>YUV0</td><td rowspan="2"></td><td>O</td><td>YUV pixel 0 output data.</td></tr>
<tr><td>PIXOUT0</td><td>O</td><td>CCIR656 output pixel 0.</td></tr>
<tr><td>VREF</td><td rowspan="3">107</td><td>I</td><td>Internal voltage reference to DAC. Bypass to ground with 0.1-µF capacitor.</td></tr>
<tr><td>YUV1</td><td>O</td><td>YUV pixel 1 output data.</td></tr>
<tr><td>PIXOUT1</td><td>O</td><td>CCIR656 output pixel 1.</td></tr>
<tr><td>CDAC</td><td rowspan="3">108</td><td>O</td><td>Chrominance signal for Y/C processing display.</td></tr>
<tr><td>YUV2</td><td>O</td><td>YUV pixel 2 output data.</td></tr>
<tr><td>PIXOUT2</td><td>O</td><td>CCIR656 output pixel 2.</td></tr>
<tr><td>COMP</td><td rowspan="3">109</td><td>I</td><td>Compensation input. Bypass to ADVEE with 0.1-µF capacitor.</td></tr>
<tr><td>YUV3</td><td>O</td><td>YUV pixel 3 output data.</td></tr>
<tr><td>PIXOUT3</td><td>O</td><td>CCIR656 output pixel 3.</td></tr>
<tr><td>RSET</td><td rowspan="3">110</td><td>I</td><td>DAC current adjustment resistor input.</td></tr>
<tr><td>YUV4</td><td>O</td><td>YUV pixel 4 output data.</td></tr>
<tr><td>PIXOUT4</td><td>O</td><td>CCIR656 output pixel 4.</td></tr>
<tr><td>ADVEE</td><td>111</td><td>P</td><td>Analog power.</td></tr>
<tr><td>ADVSS</td><td>112</td><td>G</td><td>Analog ground for video DAC.</td></tr>
<tr><td>YDAC</td><td rowspan="3">113</td><td>O</td><td>Luma component for Y/C processing display.</td></tr>
<tr><td>YUV5</td><td>O</td><td>YUV pixel 5 output data.</td></tr>
<tr><td>PIXOUT5</td><td>O</td><td>CCIR656 output pixel 5.</td></tr>
<tr><td>VDAC</td><td rowspan="3">114</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 106.</td></tr>
<tr><td>YUV6</td><td>O</td><td>YUV pixel 6 output data.</td></tr>
<tr><td>PIXOUT6</td><td>O</td><td>CCIR656 output pixel 6.</td></tr>
</table>

Table 1 ES6425 Pin Description (Continued)

Name	Pin Numbers	I/O	Definition
YUV7	115	O	YUV pixel 7 output data.
PIXOUT7		O	CCIR656 output pixel 7.
PCLK2XSCN	116	I/O	27-MHz video pixel clock.
CAMIN4		I	Camera and YUV input 4.
PCLKQSCN	117	O	13.5-MHz video output pixel clock.
AUX3[2]		I/O	Aux3 data I/O; (5V tolerant input).
CAMIN5		I	Camera and YUV input 5
VSYNC#	118	I/O	Vertical sync (active-low); (5V tolerant input).
AUX3[1]		I/O	Aux3 data I/O; (5V tolerant input).
CAMIN6		I	Camera and YUV input 6.
HSYNC#	119	I/O	Horizontal sync (active-low); (5V tolerant input).
AUX3[0]		I/O	Aux3 data I/O; (5V tolerant input).
CAMIN7		I	Camera and YUV input 7.
HD[5:0]	122-127	I/O	Host data bus; (5V tolerant input).
AUX1[5:0]		I/O	Aux1 data I/O; (5V tolerant input).
HD6	128	I/O	Host data bus; (5V tolerant input).
AUX1[6]		I/O	Aux1 data I/O; (5V tolerant input).
VFD_DOUT		O	VFD data output.
HD7	131	I/O	Host data bus; (5V tolerant input).
AUX1[7]		I/O	Aux1 data I/O; (5V tolerant input).
VFD_DIN		I	VFD data input.
HD8	132	I/O	Host data bus; (5V tolerant input).
AUX2[0]		I/O	Aux2 data I/O; (5V tolerant input).
VFD_CLK		I	VFD clock.
HD9	133	I/O	Host data bus; (5V tolerant input).
AUX2[1]		I/O	Aux2 data I/O; (5V tolerant input).
HD10	134	I/O	Host data bus; (5V tolerant input).
AUX2[2]		I/O	Aux2 data I/O; (5V tolerant input).
HD11	135	I/O	Host data bus; (5V tolerant input).
AUX2[3]		I/O	Aux2 data I/O; (5V tolerant input).
HD12	136	I/O	Host data bus; (5V tolerant input).
AUX2[4]		I/O	Aux2 data I/O; (5V tolerant input).
HD13	137	I/O	Host data bus; (5V tolerant input).
AUX2[5]		I/O	Aux2 data I/O; (5V tolerant input).
HD14	140	I/O	Host data bus; (5V tolerant input).
AUX2[6]		I/O	Aux2 data I/O; (5V tolerant input).
HD15	141	I/O	Host data bus; (5V tolerant input).
AUX2[7]		I/O	Aux2 data I/O 7; (5V tolerant input).
IR		I	IR remote control; (5V tolerant input).
HWRQ#	142	O	Host write request (active-low).
AUX4[1]		I/O	Aux4 data I/O 1; (5V tolerant input).

Table 1 ES6425 Pin Description (Continued)

Name	Pin Numbers	I/O	Definition
HRRQ#	143	O	Host read request (active-low).
AUX4[0]		I/O	Aux4 data I/O 0; (5V tolerant input).
CAMIN2		I	Camera and YUV input 2.
HIRQ	144	O	Host interrupt.
AUX4[7]		I/O	Aux4 data I/O 7; (5V tolerant input).
HRST#	145	O	Host reset (active-low).
AUX3[5]		I/O	Aux3 data I/O 5; (5V tolerant input).
HIORDY	146	I	Host I/O ready.
AUX3[3]		I/O	Aux3 data I/O 3; (5V tolerant input).
HWR#	149	O	Host write (active-low).
AUX4[5]		I/O	Aux4 data I/O 5; (5V tolerant input).
HRD#	150	O	Host read (active-low).
AUX4[6]		I/O	Aux4 data I/O 6; (5V tolerant input).
HIOCS16#	151	I	Device 16 bit data transfer (active-low).
AUX3[4]		I/O	Aux3 data I/O 4; (5V tolerant input).
CAMCLK		I	Camera and YUV port pixel clock.
HCS1FX#	152	O	Host select 1 (active-low).
AUX3[7]		I/O	Aux3 data I/O 7; (5V tolerant input).
HCS3FX#	153	O	Host select 3 (active-low).
AUX3[6]		I/O	Aux3 data I/O 6; (5V tolerant input).
HA[2:0]	154, 155, 158	I/O	Host address bus.
AUX4[4:2]		I/O	Aux4 data I/Os 2, 3, and 4; (5V tolerant input).
AUX0	160	I/O	Auxiliary port 0 (open collector); (5V tolerant input).
I2CDATA		I/O	I^2C data I/O; (5V tolerant input).
AUX1	161	I/O	Auxiliary port 1 (open collector); (5V tolerant input).
I2C_CLK		I/O	I^2C clock I/O; (5V tolerant input).
IOW#	162	O	I/O write strobe (LCS1) (active-low).
AUX2		I/O	Auxiliary port 2; (5V tolerant input).
IOR#	165	O	I/O read strobe (LCS1) (active-low).
AUX3		I/O	Auxiliary port 3; (5V tolerant input).
AUX4-7	166-169	I/O	Auxiliary ports 4-7; (5V tolerant input).
LOE#	170	O	RISC port output enable (active-low).
LCS0#	173	O	RISC port chip select 0 (active-low).
PIXOUT_CLK		O	CCIR656 output pixel clock.
LCS[3:1]#	174-176	O	RISC port chip select [3:1] (active-low).
LD[15:0]	178-182, 185-191, 194-197	I/O	RISC port data bus; (5V tolerant input).
LWRLL#	198	O	RISC port low-byte write enable (active-low).
LWRHL#	199	O	RISC port high-byte write enable (active-low).
CAMIN0	202	I	Camera and YUV input 0.
CAMIN1	203	I	Camera and YUV input 1.

SYSTEM BLOCK DIAGRAM

A sample system block diagram for the ES6425 board design is shown in Figure 2.

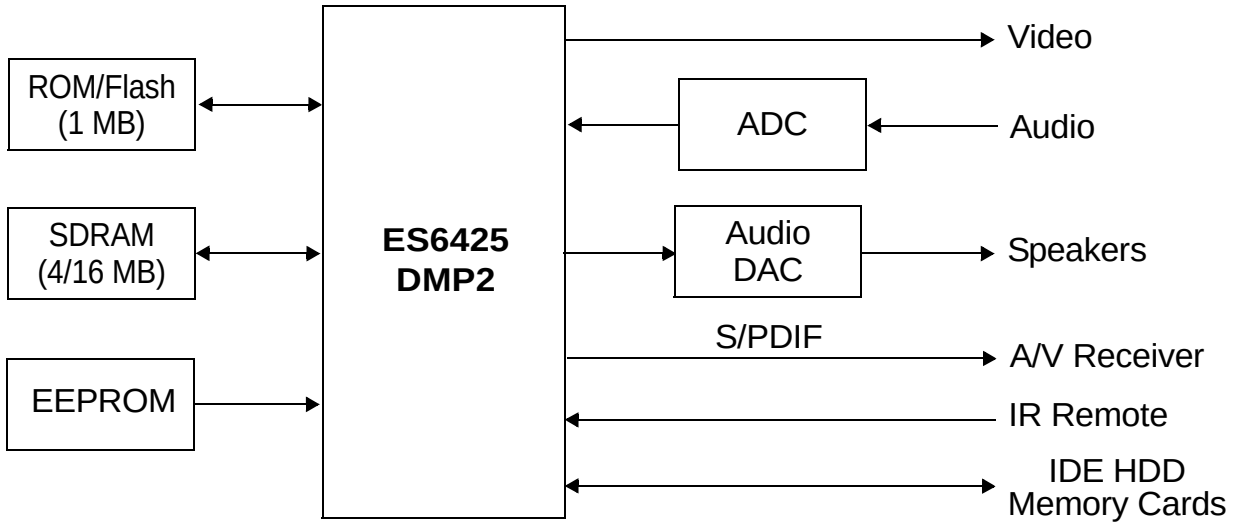

Figure 2 ES645 System Block Diagram

ORDERING INFORMATION

Part Number	Description	Package
ES6425FF	Digital Media Processor 2 with lead-free leads.	208-pin PQFP
ES6425FDF	Digital Media Processor 2 with Dolby Digital support and lead-free leads.	208-pin PQFP

The letter F at the end of the part number identifies the package type PQFP.

The second letter F at the end of the part number indicates lead-free leads with the device.

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