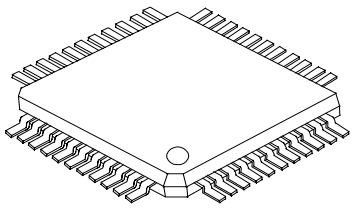
UA1538 **LINEAR INTEGRATED CIRCUIT**

4-CH MOTOR DRIVER FOR PORTABLE CD PLAYERS



QFP-44-0.8

*Pb-free plating product number: UA1538L

■ DESCRIPTION

The UTC UA1538 contains a 4ch H bridge driver and DC-DC converter control circuit on one chip, and was developed for use in portable CD players.

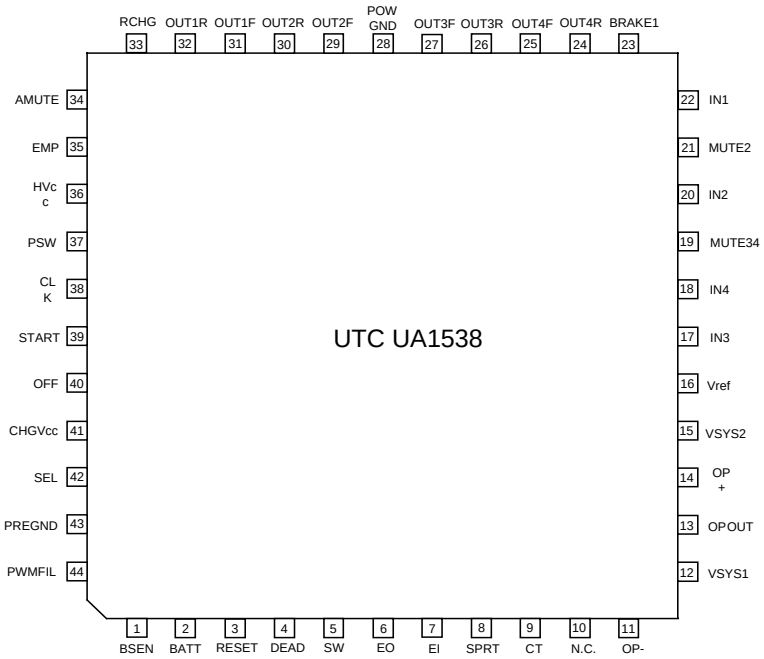
■ FEATURES

*Built-in 4ch H bridge driver, and PWM control of load drive voltage is made possible by external components.
*DC-DC converter control circuit on chip.
*With reset output inversion output pin.
*Empty detection level can be switched between rechargeable battery and dry battery.
*Constant current charging; current value can be varied using external resistor.
*Built-in power transistor for charging.
*Built-in independent thermal shutdown circuit.

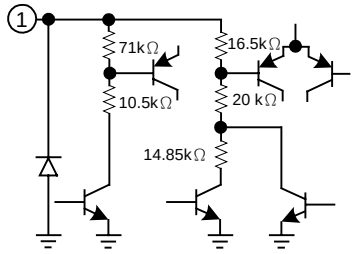
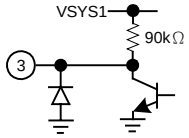
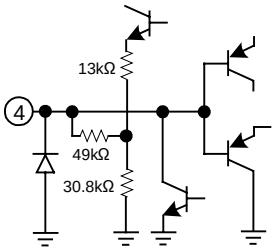
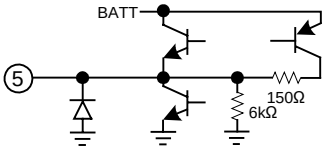
■ ORDERING INFORMATION

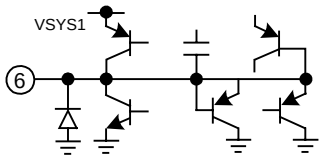
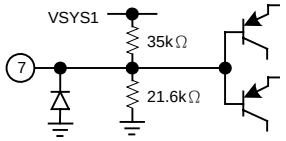
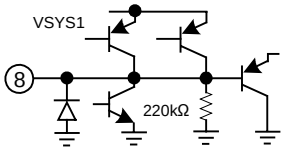
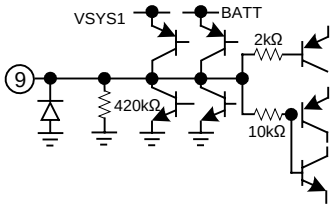
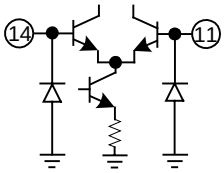
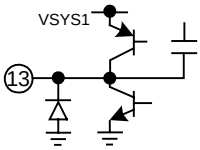
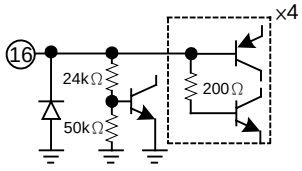
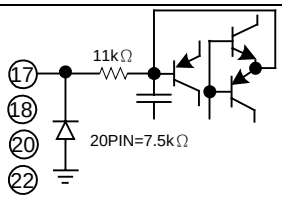
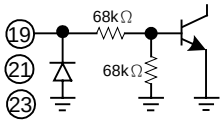
Ordering Number		Package	Packing
Normal	Lead Free Plating		
UA1538-QM1-T	UA1538L-QM1-T	QFP-44-0.8	Tube

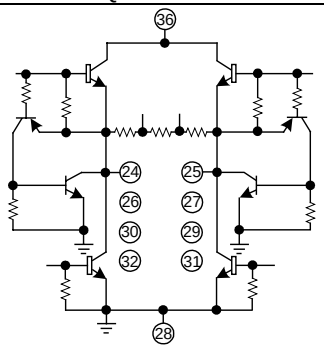
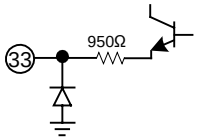
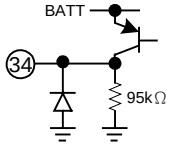
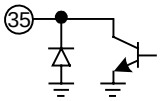
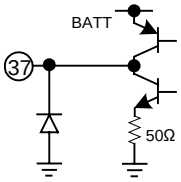
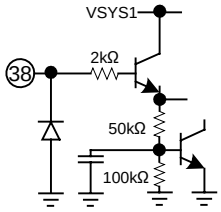
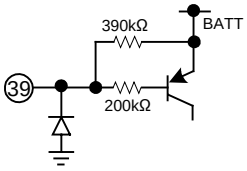
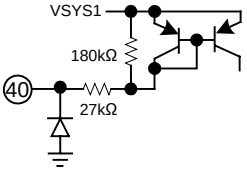
■ PIN CONFIGURATION

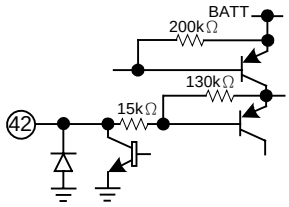
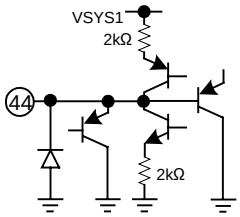


■ PIN DESCRIPTION

PIN NO.	PIN NAME	INPUT/OUTPUT	FUNCTION	INTERMAL EQUIVALENT CIRCUIT
1	BSEN	Input	Battery Voltage Monitor	
2	BATT	Input	Battery Power Supply Input	Power Supply
3	RESET	Output	Reset Detect Output	
4	DEAD	Input	DEAD Time Setting	
5	SW	Output	Transistor Drive For Voltage Multiplier	

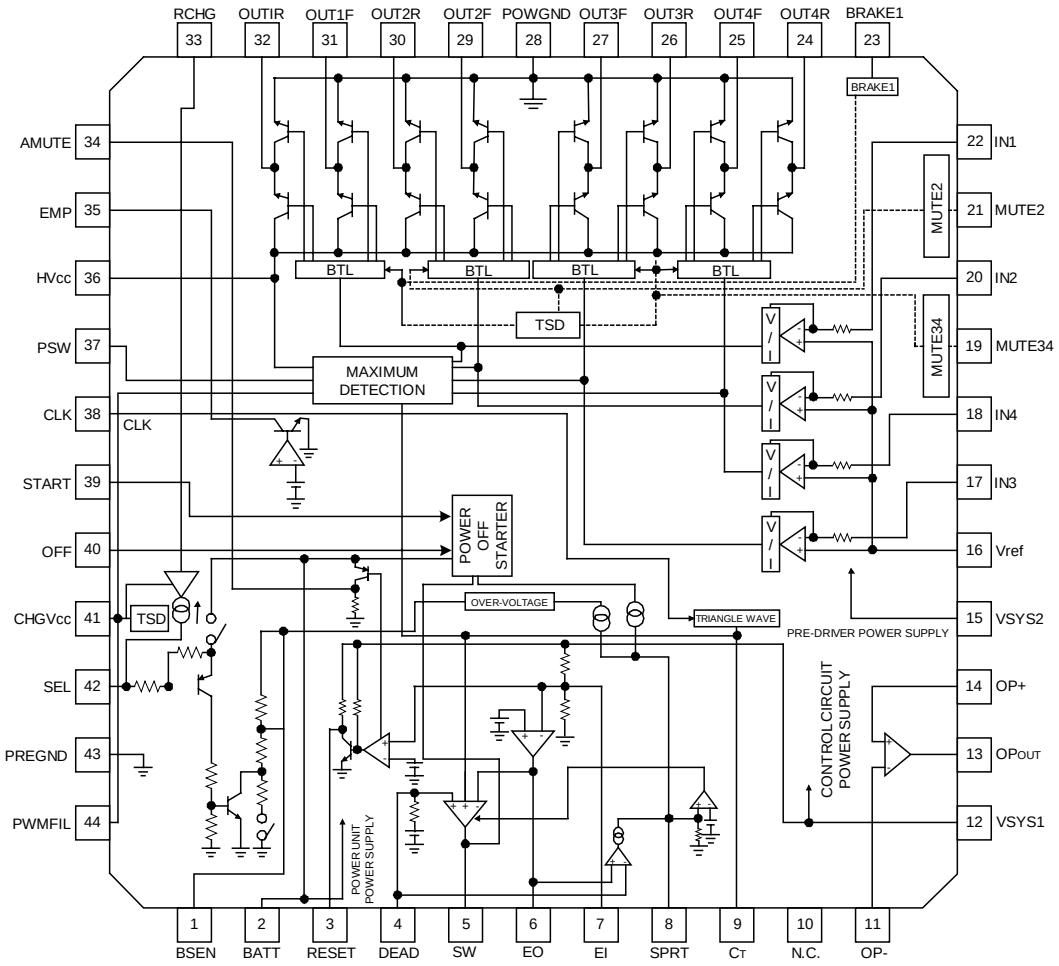
PIN NO.	PIN NAME	INPUT/OUTPUT	FUNCTION	INTERMAL EQUIVALENT CIRCUIT
6	EO	Output	Error Amplifier Output	
7	EI	Input	Error Amplifier Input	
8	SPRT	Output	Short Circuit Protection Setting	
9	CT	Output	Triangular-Wave Output	
10	N.C.			
11 14	OP- OP+	Input	Op Amp Negative Input Op Amp Positive Input	
12	VSYS1	Input	Control Circuit Power Supply Input	Control Circuit Power Supply
13	OPOUT	Output	Op Amp Output	
15	VSYS2	Input	Driver Pre-step Power Supply	Pre-Drive Power Supply
16	Vref	Input	Reference Voltage Input	
17 18 20 22	IN3 IN4 IN2 IN1	Input	Ch3 Control Signal Input Ch4 Control Signal Input Ch2 Control Signal Input Ch1 Control Signal Input	
19 21 23	MUTE34 MUTE2 BRAKE1	Input	Ch3 and 4 Mute Ch2 Mute Ch1 Brake	

PIN NO.	PIN NAME	INPUT/OUTPUT	FUNCTION	INTERMAL EQUIVALENT CIRCUIT
24	OUT4R	Output	Ch4 Negative Output	
25	OUT4F		Ch4 Positive Output	
26	OUT3R		Ch3 Negative Output	
27	OUT3F		Ch3 Positive Output	
29	OUT2F		Ch2 Positive Output	
30	OUT2R		Ch2 Negative Output	
31	OUT1F		Ch1 Positive Output	
32	OUT1R		Ch1 Negative Output	
28	POWGND		Power Block Power Supply Ground	
36	HVcc	Input	H-Bridge Power Supply Input	
33	RCHG	Input	Charge Current Setting	
34	AMUTE	Output	Reset Invert Output	
35	EMP	Output	Empty Detect Output	
37	PSW	Output	PWM Transistor Drive	
38	CLK	Input	External Clock Synchronizing Input	
39	START	Input	Voltage Multiplier DC-DC Converter Start	
40	OFF	Input	Voltage Multiplier DC-DC Converter OFF	
41	CHGVcc	Input	Charging Circuit Power Supply Input	Charging Circuit Power Supply

PIN NO.	PIN NAME	INPUT/OUTPUT	FUNCTION	INTERMAL EQUIVALENT CIRCUIT
42	SEL	Input/Output	Empty Detect Level Switch	
43	PREGND		Pre Section Power Supply Ground	Pre Section Power Supply Ground
44	PWMFIL	Input	PWM Phase Compensation	

*The positive and negative outputs are the polarity with respect to the input

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	Vcc *1	13.5	V
Driver Output Current	Io	500	mA
Power Dissipation	P_D	625	mW
Operating Temperature	T_{OPR}	0 ~ +70	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

*1: Vcc shows input voltage of VSYS1,VSYS2, HVcc, BATT,and CHGVcc.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Control Circuit Power Supply Voltage	VSYS1	2.7	3.2	5.5	V
Pre-Driver Circuit Power Supply Voltage	VSYS2	2.7	3.2	5.5	V
H-Bridge Power Supply Voltage	HVcc		PWM	BATT	V
Power Supply Voltage	BATT	1.5	2.4	8.0	V
Charging circuit Power supply Voltage	CHGVcc	3.0	4.5	8.0	V
Operating Temperature	Ta	-10	25	70	°C

■ ELECTRICAL CHARACTERISTICS

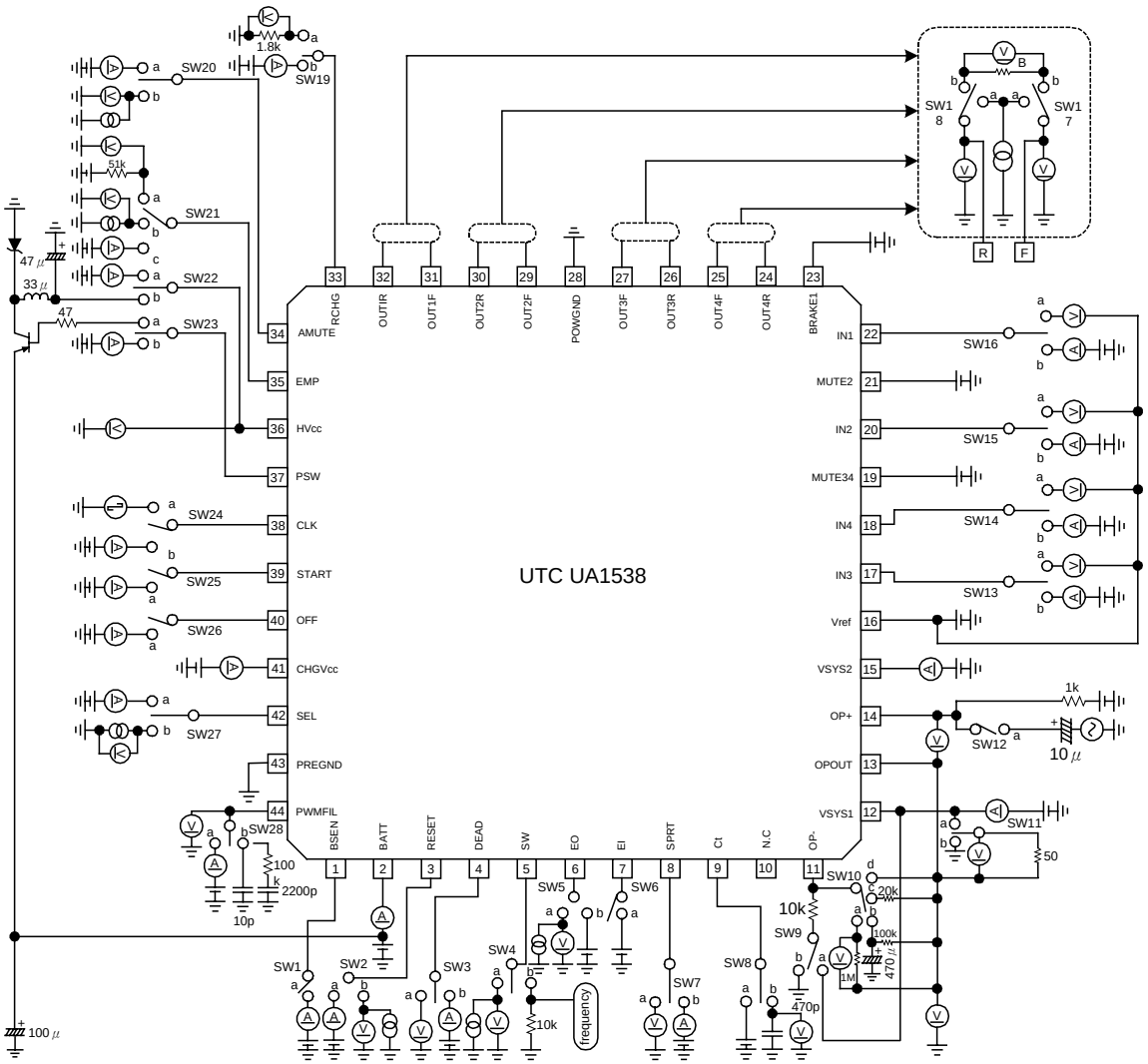
(Ta=25℃, BATT=2.4V, VSYS1=VSYS2=3.2V, Vref=1.6V, CHGVcc=0V, fCLK=88.2kHz, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Section						
BATT Stand-by Current	I_{ST}	BATT=9.0V, VSYS1=VSYS2=Vref=0V		0	3	μA
BATT Supply Current (No load)	I_{BAT}	HVcc=0.45V, MUTE34=3.2V		2.5	4.0	mA
VSYS1 Supply Current (No load)	I_{SYS1}	HVcc=0.45V, MUTE34=3.2V, EI=0V			4.5	mA
VSYS2 Supply Current (No load)	I_{SYS2}	HVcc=0.45V, MUTE34=3.2V		4.1	5.5	mA
CHGVcc Supply Current (No load)	I_{CGVCC}	CHGVCC=4.5V, R_{OUT}=OPEN		0.65	2.00	mA
H-Bridge Driver Part						
Voltage Gain ch1,ch3.ch4	G_{VC134}		12	14	16	dB
Voltage Gain ch2	G_{VC2}		21.5	23.5	24.5	dB
Gain Error By Polarity	ΔG_{VC}		-2	0	2	dB
Input pin resistance ch1,ch3,ch4	R_{IN134}	IN=1.7V and 1.8V	9	11	13	kΩ
Input pin resistance ch2	R_{IN2}	IN=1.7V and 1.8V	6	7.5	9	kΩ
Maximum Output Voltage	V_{OUT}	R_L=8Ω,HVcc=BATT=4.0V IN=0-3.2V	1.9	2.1		V
Saturation Voltage (Lower)	V_{satL}	Io=-300mA, IN=0 and 3.2V		240	400	mV
Saturation Voltage (Upper)	V_{satU}	Io=-300mA, IN=0 and 3.2V		240	400	mV
Input Offset Voltage	V_{OI}		-8	0	8	mV
Output Offset Voltage ch1,ch3,ch4	V_{OO134}	Vref=IN=1.6V	-50	0	50	mV
Output Offset Voltage ch2	V_{OO2}	Vref=IN=1.6V	-130	0	130	mV
Dead Zone	V_{DB}		-10	0	10	mV
BRAKE1ON Threshold Voltage	V_{BRON}	IN1=1.8V	2.0			V
BRAKE1OFF Threshold Voltage	V_{BROFF}	IN1=1.8V			0.8	V
MUTE2 ON Threshold Voltage	V_{M2ON}	IN2=1.8V	2.0			V
H-Bridge Driver Part						
MUTE2 OFF Threshold Voltage	V_{M2OFF}	IN2=1.8V			0.8	V
MUTE34 ON Threshold Voltage	V_{M34ON}	IN3=IN4=1.8V			0.8	V
MUTE34 OFF Threshold Voltage	V_{M34OFF}	IN3=IN4=1.8V	2.0			V
Vref ON Threshold Voltage	V_{refON}	IN1=IN2=IN3=IN4=1.8V	1.2			V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vref OFF Threshold Voltage	V_{refOFF}	IN1=IN2=IN3=IN4=1.8V			0.8	V
BRAKE1 Brake Current	I_{BRAKE1}	Current difference between BRAKE pin "H" time and "L" time.	4	7	10	mA
PWM Power Supply Driving						
PSW Sink Current	I_{PSW}	IN1=2.1V	10	13	17	mA
HVcc Level Shift Voltage	V_{SHIF}	IN1=1.8V, HVcc-OUT1F	0.35	0.45	0.55	V
HVcc Leak Current	I_{HLK}	HVcc=9.0V, VSYS1=VSYS2=BATT=0V		0	5	μA
PWM Amp Transfer Gain	G_{PWM}	IN1=1.8V, HVcc=1.2 ~ 1.4V	1/60	1/50	1/40	1/kΩ
DC-DC Converter						
Error Amp						
VSYS1 Threshold Voltage	V_{S1TH}		3.05	3.20	3.35	V
EO Pin Output Voltage "H"	V_{EOH}	EI=0.7V, Io=-100μA	1.4	1.6		V
EO Pin Output Voltage "L"	V_{EOL}	EI=1.3V, Io=100μA			0.3	V
Short Circuit Protection						
SPRT Pin Voltage	V_{SPR}	EI=1.3V		0	0.1	V
EO=H SPRT Pin Current1	I_{SPR1}	EI=0.7V	6	10	16	μA
OFF=L SPRT Pin Current2	I_{SPR2}	EI=1.3V, OFF=0V	12	20	32	μA
SPRT Pin Current3 Over-Voltage	I_{SPR3}	EI=1.3V, BATT=9.5V	12	20	32	μA
SPRT Pin Impedance	R_{SPR}		175	220	265	kΩ
SPRT Pin Threshold Voltage	V_{SPTH}	EI=0.7V, C_T=0V	1.10	1.20	1.30	V
Over-Voltage Protection Detect	V_{HVPR}	BSEN Pin Voltage	8.0	8.4	9.0	V
Transistor Driving						
SW Pin Output Voltage1 "H"	V_{SW1H}	BATT=C_T=1.5V, VSYS1=VSYS2=0V, Io=-2mA Starting Time	0.78	0.98	1.13	V
SW Pin Output Voltage2 "H"	V_{SW2H}	C_T=0V, Io=-10mA, EI=0.7V, SPRT=0V	1.00	1.50		V
SW Pin Output Voltage2 "L"	V_{SW2L}	C_T=2.0V, Io=10mA		0.30	0.45	V
SW Pin Oscillating Frequency1	f_{SW1}	C_T=470pF, VSYS1=VSYS2=0V Starting Time	65	80	95	kHz
SW Pin Oscillating Frequency2	f_{SW2}	C_T=470pF, CLK=0V	60	70	82	kHz
SW Pin Oscillating Frequency3	f_{SW3}	C_T=470pF		88.2		kHz
SW Pin Minimum Pulse Width	T_{SWmin}	C_T=470pF, EO=0.5V→0.7V Sweep	0.01		0.60	μs
Pulse Duty Start	D_{SW1}	C_T=470pF,VSYS1=VSYS2=0V	40	50	60	%
Max. Pulse Duty At Self-Running	D_{SW2}	C_T=470pF, EI=0.7V, CLK=0V	70	80	90	%
Max. Pulse Duty At CLK Synchronization	D_{SW3}	C_T=470pF, EI=0.7V	65	75	85	%
Interface						
OFF Pin Threshold Voltage	V_{OFTH}	EI=1.3V			VSYS1-2.0	V
OFF Pin Bias Current	I_{OFF}	OFF=0V	75	95	115	μA
START Pin ON Threshold Voltage	V_{STATH1}	VSYS1=VSYS2=0V, C_T=2.0V			BATT-1.0	V
START Pin OFF Threshold Voltage	V_{STATH2}	VSYS1=VSYS2=0V, C_T=2.0V	BATT-0.3			V
START Pin Bias Current	I_{START}	START=0V	10 13	20 16	30 19	μA
CLK Pin Threshold Voltage "H"	V_{CLKTHH}		2.0			V
CLK Pin Threshold Voltage "L"	V_{CLKTHL}				0.8	V
CLK Pin Bias Current	I_{CLK}	CLK=3.2V			10	μA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dead Time						
DEAD Pin Impedance	R_{DEAD}		52	65	78	kΩ
DEAD Pin Output Voltage	V_{DEAD}		0.78	0.88	0.98	V
Starter Circuit						
Starter Switching Voltage	V_{STNM}	VSYS1=VSYS2=0→3.2V, START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	V_{SNHS}	START=0V	130	200	300	mV
Discharge Release	V_{DIS}		1.63	1.83	2.03	V
Empty Detection						
EMP Detection Voltage 1	V_{EMPT1}	VSEL=0V	2.1	2.2	2.3	V
EMP Detection Voltage 2	V_{EMPT2}	ISEL=- 2μA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	V_{EMHS1}	VSEL=0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	V_{EMHS2}	ISEL=- 2μA	25	50	100	mV
EMP Pin Output Voltage	V_{EMP}	Io=1mA, BSEN=1V			0.5	V
EMP Pin Output Leak Current	I_{EMPL}	BSEN=2.4V			1.0	μA
BSEN Pin Input Resistance	R_{BSEN}	VSEL=0V	17	23	27	kΩ
BSEN Pin Leak Current	I_{BSENL}	VSYS1=VSYS2=0V BSEN=4.5V			1.0	V
SEL Pin Detection Voltage	V_{SELTH}	VSELTH=BATT-SEL BSEN=2.0V	1.5			V
SEL Pin Detection Current	I_{SELT}		-2			μA
Reset Circuit						
VSYS1 RESET Threshold Voltage Ratio	H_{SRT}	Comparison with error amplifier threshold voltage	85	90	95	%
RESET Detection Hysteresis Width	V_{RSTHS}		25	50	100	mV
RESET Pin Output Voltage	V_{RST}	Io=1mA, VSYS1=VSYS2=2.8V			0.5	V
RESET Pin PULL UP Resistance	R_{RST}		72	90	108	kΩ
AMUTE Pin Output Voltage 1	V_{AMT1}	Io=-1mA, VSYS1=VSYS2=2.8V	BATT -0.4		BATT	V
AMUTE Pin Output Voltage 2	V_{AMT2}	Io=-1mA, START=0V, VSYS1=VSYS2=0V	BATT -0.4		BATT	V
AMUTE Pin PULL DOWN Resistance	R_{AMT}		77	95	113	kΩ
Op Amp						
Input Bias Current	I_{BIAS}	OP+=1.6V			300	nA
Input Offset Voltage	V_{OIOP}		-5.5	0	5.5	mV
High Level Output Voltage	V_{OHOP}	R_L=OPEN	2.8			V
Low level Output Voltage	V_{OLOP}	R_L=OPEN			0.2	V
Output Drive Current (Source)	I_{SOU}	50Ω GND		-6.5	-3.0	mA
Output Drive Current (Sink)	I_{SIN}	50Ω VSYS1	0.4	0.7		mA
Open Loop Voltage Gain	G_{VO}	V_{IN}=-75dBV, f=1kHz		70		dB
Slew Rate	S_R			0.5		V/μs
Battery Charging Circuit						
RCHG Pin Bias Voltage	V_{RCHG}	CHGVcc=4.5V, RCHG=1.8kΩ.	0.71	0.81	0.91	V
RCHG Pin Output Resistance	R_{RCHG}	CHGVcc=4.5V, RCHG=0.5 and 0.6V	0.75	0.95	1.20	kΩ
SEL Pin Leak Current 1	I_{SELLK1}	CHGVcc=4.5V, RCHG=OPEN, BATT=4.5V			1.0	μA
SEL Pin Leak Current 2	I_{SELLK2}	CHGVcc=0.6V, RCHG=1.8kΩ, BATT=4.5V			1.0	μA
SEL Pin Saturation Voltage	V_{SELCG}	CHGVcc=4.5V, Io=300mA, RCHG=0Ω		0.45	1.00	V

■ MEASURING CIRCUIT



■ SWITCHING POSITION TABLE

ITEM	SW NO.									
	1	4	5	6	7	8	22	24	25	26
BATT Stand-by Current	-	-	-	-	-	-	-	-	-	-
BATT Supply Current (No load)	-	-	-	-	-	-	a	-	a	-
VSYS1 Supply Current (No load)	-	-	-	a	-	-	a	-	a	-
VSYS2 Supply Current (No load)	-	-	-	-	-	-	a	-	a	-
CHGVcc Supply Current (No load)	-	-	-	-	-	-	-	-	-	-
VSYS1 Threshold Voltage	-	-	a	-	-	-	-	-	-	-
EO Pin Output Voltage “H”	-	-	a	a	-	-	-	-	-	-
EO Pin Output Voltage ”L”	-	-	a	a	-	-	-	-	-	-
SPRT Pin Voltage	-	-	-	a	a	-	-	-	-	-
SPRT Pin Current1 EO=”H”	-	-	-	a	b	-	-	-	-	-
SPRT Pin Current2 OFF=”L”	-	-	-	a	b	-	-	-	-	a
SPRT Pin Current3 Over-Voltage	a	-	-	a	b	-	-	-	-	-
SPRT Pin Impedance	-	-	-	-	b	-	-	-	-	-
SPRT Pin Threshold Voltage	-	-	-	a	a	a	-	-	-	-
Over-Voltage Protection Detect	a	-	-	-	a	-	-	-	-	-
SW Pin Output Voltage1”H”	-	a	-	-	-	a	-	-	a	-
SW Pin Output Voltage2”H”	-	a	-	a	b	a	-	-	-	-
SW Pin Output Voltage2”L”	-	a	-	-	-	a	-	-	-	-
SW Pin Oscillating Frequency 1	-	b	-	-	-	b	-	-	a	-
SW Pin Oscillating Frequency 2	-	b	-	-	-	b	-	b	-	-
SW Pin Oscillating Frequency 3	-	b	-	-	-	b	-	a	-	-
SW Pin Minimum Pulse Width	-	b	b	-	-	b	-	-	-	-
Pulse Duty Start	-	b	-	-	-	b	-	b	a	-
Max Pulse Duty At Self-Running	-	b	-	-	-	b	-	b	-	-
Max Pulse Duty At CLK Synchronization	-	b	-	a	-	b	-	a	-	-

-: Turn off switch

ITEM	SW NO.									
	2	3	4	6	7	8	20	24	25	26
DEAD Pin Impedance	-	b	-	-	-	-	-	-	-	-
DEAD Pin Output Voltage	-	a	-	-	-	-	-	-	-	-
OFF Pin Threshold Voltage	-	-	-	a	a	-	-	-	-	a
OFF Pin Bias Current	-	-	-	-	-	-	-	-	-	a
START Pin ON Threshold Voltage	-	-	a	-	-	a	-	-	a	-
START Pin OFF Threshold Voltage	-	-	a	-	-	a	-	-	a	-
START Pin Bias Current	-	-	-	-	-	-	-	-	a	-
CLK Pin Threshold Voltage “H”	-	-	a	-	-	b	-	b	-	-
CLK Pin Threshold Voltage “L”	-	-	a	-	-	b	-	b	-	-
CLK Pin Bias Current	-	-	-	-	-	-	-	a	-	-
Starter Switching Voltage	-	-	a	-	-	-	-	-	a	-
Starter Switching Hysteresis Width	-	-	a	-	-	-	-	-	a	-
Discharge Release Voltage	-	-	-	-	a	-	-	-	-	-
VSYS1 Pin RESET Threshold Voltage Ratio	b	-	-	-	-	-	-	-	-	-
RESET Detection Hysteresis Width	b	-	-	-	-	-	-	-	-	-
RESET Pin Output Voltage	b	-	-	-	-	-	-	-	-	-
RESET Pin PULL UP Resistance	a	-	-	-	-	-	-	-	-	-
AMUTE Pin Output Voltage 1	-	-	-	-	-	-	b	-	--	-
AMUTE Pin Output Voltage 2	-	-	-	-	-	-	b	-	a	-
AMUTE Pin PULL DOWN Resistance	-	-	-	-	-	-	a	-	-	-

-: Turn off switch

ITEM	SW NO.						
	1	9	10	11	12	21	27
EMP Detection Voltage 1	a	-	-	-	-	a	a
EMP Detection Voltage 2	a	-	-	-	-	a	b
EMP Detection Hysteresis Voltage 1	a	a	-	-	-	a	a
EMP Detection Hysteresis Voltage 2	a	-	-	-	-	a	b
EMP Pin Output Voltage	a	-	-	-	-	b	-
EMP Pin Output Leak Current	a	-	-	-	-	c	-
BSEN Pin Input Resistance	a	-	-	-	-	-	a
BSEN Pin Leak Current	a	-	-	-	-	-	-
SEL Pin Detection Voltage	a	-	-	-	-	a	a
SEL Pin Detection Current	a	-	-	-	-	a	b
Input Bias Current	-	-	a	-	-	-	-
Input Offset Voltage	-	-	d	-	-	-	-
“H” Level Output Voltage	-	b	c	-	-	-	-
“L” Level Output Voltage	-	a	c	-	-	-	-
Output Drive Current (Source)	-	-	d	b	-	-	-
Output Drive Current (Sink)	-	-	d	a	-	-	-
Open Loop Voltage Gain	-	-	b	-	a	-	-
Slew Rate	-	-	d	-	a	-	-

-: Turn off switch

ITEM		SW NO.						
		13	14	15	16	17	18	22
Voltage Gain	Ch1R	-	-	-	b	b	b	a
	Ch2R	-	-	b	-	b	b	a
	Ch3R	b	-	-	-	b	b	a
	Ch4R	-	b	-	-	b	b	a
Gain Error By Polarity	Ch1	-	-	-	b	b	b	a
	Ch2	-	-	b	-	b	b	a
	Ch3	b	-	-	-	b	b	a
	Ch4	-	b	-	-	b	b	a
Input Pin resistance	Ch1	-	-	-	b	b	b	a
	Ch2	-	-	b	-	b	b	a
	Ch3	b	-	-	-	b	b	a
	Ch4	-	b	-	-	b	b	a
Maximum Output Voltage	Ch1R	-	-	-	b	b	b	a
	Ch2R	-	-	b	-	b	b	a
	Ch3R	b	-	-	-	b	b	a
	Ch4R	-	b	-	-	b	b	a
Saturation Voltage (Lower)	Ch1F	-	-	-	b	a	-	a
	Ch1R	-	-	-	b	-	a	a
	Ch2F	-	-	b	-	a	-	a
	Ch2R	-	-	b	-	-	a	a
	Ch3F	b	-	-	-	a	-	a
	Ch3R	b	-	-	-	-	-	a
	Ch4F	-	b	-	-	a	-	a
	Ch4R	-	b	-	-	-	a	a
Saturation Voltage (Upper)	Ch1F	-	-	-	b	a	-	a
	Ch1R	-	-	-	b	-	a	a
	Ch2F	-	-	b	-	a	-	a
	Ch2R	-	-	b	-	-	a	a
	Ch3F	b	-	-	-	a	-	a
	Ch3R	b	-	-	-	-	a	a
	Ch4F	-	b	-	-	a	-	a
	Ch4R	-	b	-	-	-	a	a

Input Offset Voltage	Ch1	-	-	-	a	-	-	a
	Ch2	-	-	a	-	-	-	a
	Ch3	a	-	-	-	-	-	a
	Ch4	-	a	-	-	-	-	a
Output Offset Voltage	Ch1	-	-	-	b	b	b	a
	Ch2	-	-	b	-	b	b	a
	Ch3	b	-	-	-	b	b	a
	Ch4	-	b	-	-	b	b	a
Dead Zone	Ch1	-	-	-	b	b	b	a
	Ch2	-	-	b	-	b	b	a
	Ch3	b	-	-	-	b	b	a
	Ch4	-	b	-	-	b	b	a

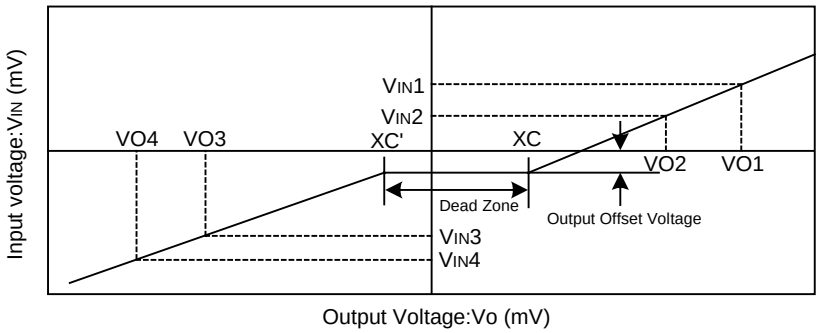
-: Turn off switch

ITEM		SW NO.								
		13	14	15	16	17	18	22	23	28
BRAKE1 ON Voltage	Ch1	-	-	-	b	b	b	a	-	-
BRAKE1 OFF Voltage	Ch1	-	-	-	b	b	b	a	-	-
MUTE2 ON Voltage	Ch2	-	-	b	-	b	b	a	-	-
MUTE2 OFF Voltage	Ch2	-	-	b	-	b	b	a	-	-
MUTE34 ON Voltage	Ch3	b	-	-	-	b	b	a	-	-
	Ch4	-	b	-	-	b	b	a	-	-
MUTE34 OFF Voltage	Ch3	b	-	-	-	b	b	a	-	-
	Ch4	-	b	-	-	b	b	a	-	-
Vref ON Voltage	Ch1	-	-	-	b	b	b	a	-	-
	Ch2	-	-	b	-	b	b	a	-	-
	Ch3	b	-	-	-	b	b	a	-	-
	Ch4	-	b	-	-	b	b	a	-	-
Vref OFF Voltage	Ch1	-	-	-	b	b	b	a	-	-
	Ch2	-	-	b	-	b	b	a	-	-
	Ch3	b	-	-	-	b	b	a	-	-
	Ch4	-	b	-	-	b	b	a	-	-
BREAK1 Brake Current	Ch1	-	-	-	b	b	b	a	-	-
PWM Sink Current		-	-	-	b	-	-	a	b	a
HVcc Level Shift Voltage		-	-	-	b	b	b	b	a	b
HVcc Leak Current		-	-	-	-	b	b	a	-	-
PWM Amp Transfer Gain		-	-	-	b	b	b	a	-	-

ITEM	SW NO.	
	19	27
CHGSET Pin Bias Voltage	a	-
CHGSET Pin Output Resistance	b	-
SEL Pin Leak Current 1	-	a
SEL Pin Leak Current 2	a	a
SEL Pin Saturation Voltage	b	b

-: Turn off switch

■ SWITCHING POSITION TABLE



* Voltage Gain

$$Gvc(+)=20\log\frac{VO1-VO2}{V_{IN}1-V_{IN}2}$$

$$Gvc(-)=20\log\frac{VO3-VO4}{V_{IN}3-V_{IN}4}$$

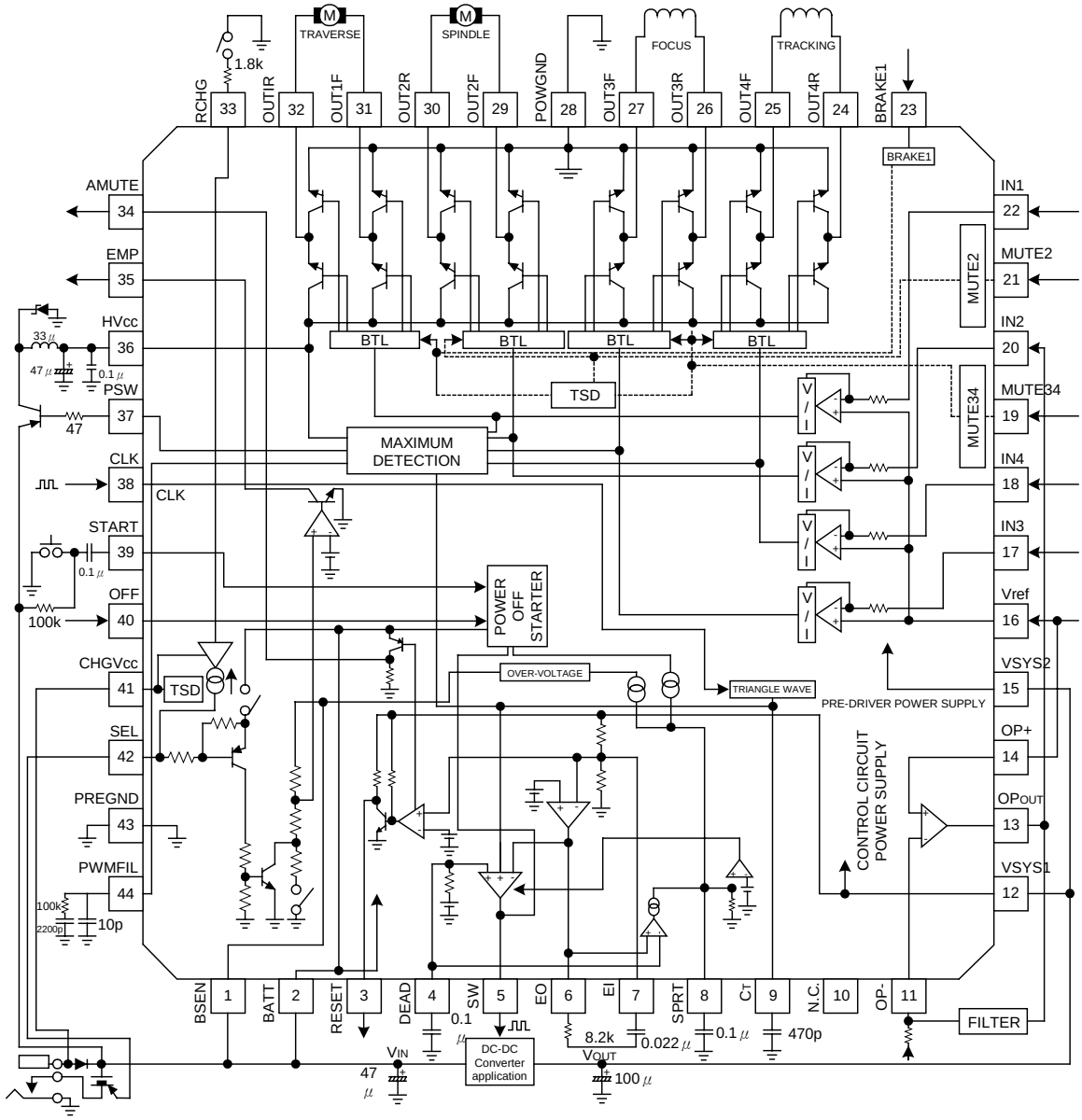
* Gain Error By Polarity

Gvc=Gvc (+)-Gvc (-)

* Dead Zone

$$XC-XC'=\frac{V_{IN}2\cdot VO1-V_{IN}1\cdot VO2}{VO1-VO2}-\frac{V_{IN}3\cdot VO4-V_{IN}4\cdot VO3}{VO3-VO4}$$

■ APPLICATION CIRCUIT



* We shall not be liable for any trouble or damege caused by using this circuit.
*In the evert a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit,Mitsumi Electric Co.,Ltd.shall not be liable for any such problem,nor grant a license therefor.

■ CIRCUIT OPERATION

1 H-bridge driver block

(1) Gain setting

• The driver input resistance (ch 1,3 and 4) are 11kΩ typ. ,ch2 is 7.5kΩ typ. . Set the gain according to the following formula.

ch1 ch2 ch3	$GV=20\log\left\|\frac{55k}{11k+R}\right\|$ (db)
ch2	$GV=20\log\left\|\frac{110k}{7.5k+R}\right\|$ (db)

R:Externally-connected input

• The driver output stage power supply is HVcc (36PIN), and the bridge circuit power supply is VSYS2 (15PIN). Connect a bypass capacitor between these two power supplies (approximately 0.1μF).

(2) Mute function

• Of the four drivers,ch1 has a brake function, and the other channels have a mute function.
• When BRAKE1(23PIN)is set to high level, both ch1 outputs go low level, and the circuit enters brake mode.
• When MUTE2(21PIN)is set to high level, the ch2 output is muted.
• When MUTE34(19PIN)is set to high level, the ch3 and 4 outputs are muted.

(3) Vref drop mute

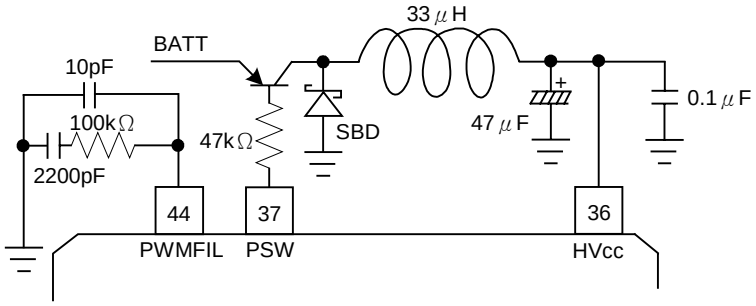
• When the voltage applied to Vref (16PIN)is 1.0V or less typ. , the driver outputs are set to high impedance.

(4) Thermal shutdown

• When the chip temperature reaches 150℃ typ. the output current is cut. The chip starts operating again at about 120℃ typ. .

2 PWM power supply drive block

• This detects the maximun output level from among the four channels, and supplies the load drive power supply (36PIN)for the PWM. The external components are a PNP transistor, coil, Schottky diode, and capacitor.

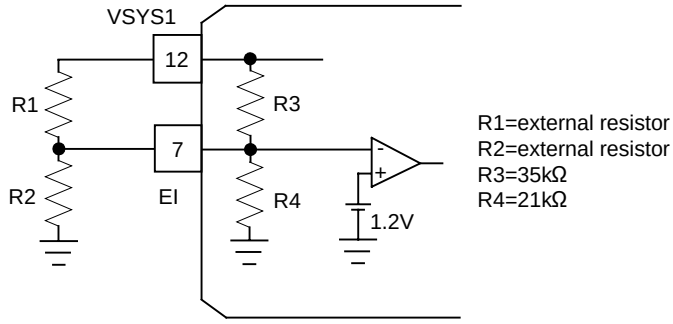


3 DC-DC converter block

(1) Output voltage

• 3.2V typ. voltage multiplier circuit can be constructed using external components. This voltage can be varied with the addition of an external resistor. The setting method is as follows.

$$VSYS1=1.2\times\frac{\frac{R1\cdot R3}{R1+R3}+\frac{R2\cdot R4}{R2+R4}}{\frac{R2\cdot R4}{R2+R4}}\ (V)$$



(2) Short protect function

• When the error amplifier output(6PIN)has switched to the high-level state, SPRT (8PIN)is charged, and when the voltage reaches 1.2V typ. , the SW(5PIN)switching stops. The time until switching stops is set by the capacitor connected to SPRT(8PIN)according to the following formula.

$t=CSPRT \times \frac{V_{TH}}{ISPRT}$ (sec) (V_{TH}=1.2V,ISPRT=10 μA)

(3) Soft start function

• The soft start function operates when a capacitor is connected between DEAD(4PIN)and GND. Also, the maximum duty can be varied by connecting a resistor to 4PIN.

t=CDEAD × R(sec) (R=65kΩ)

(4) Power off function

• When low-level is applied to OFF(40PIN), SPRT(8PIN)is charged, and when the voltage reaches 1.2V typ. , the SW(5PIN)switching stops. The time until switching stops is set by the capacitor connected to SPRT (8PIN)according to the following formula.

$t=CSPRT \times \frac{V_{TH}}{I_{OFF}}$ (sec) (V_{TH}=1.2V,I_{OFF}=20 μA)

(5) Over voltage protection circuit

• When the voltage applied to BSEN(1PIN)reaches 8.4V typ. , SPRT (8PIN) is charged, and when the voltage reaches 1.2V typ. , theSW (5PIN)switching stops. The time until switching stops is set by the capacitor connected to SPRT(8PIN)according to the following formula.

$t=CSPRT \times \frac{V_{TH}}{I_{HV}}$ (sec) (V_{TH}=1.2V,I_{HV}=20 μA)

4 Empty detector block

(1) Output voltage

• When the voltage applied to the BSEN(1PIN)falls below the detector voltage, EMP(35PIN)goes from high level to low level(open-collector output). The detector voltage has 50mV typ. of hysteresis to prevent output chattering. Use SEL (42PIN) to switch the detection voltage as shown below.

SEL	Detect Voltage	Return Voltage
L	2.20V typ.	2.25V typ.
High-Z	1.80V typ.	1.85V typ.

5 Reset circuit block

• At about 90% typ. of the DC-DC converter output voltage, RESET(3PIN)goes from low level to high level, and AMUTE(34PIN)goes from high level to low level. The reset voltage has 50mV typ. of hysteresis to prevent output chattering.

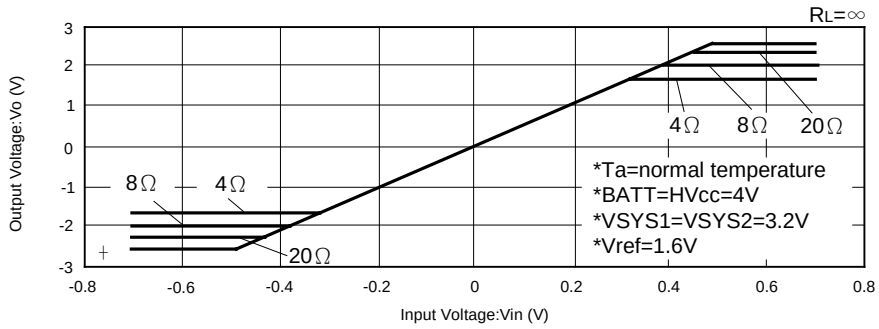
6 Charging circuit block

• The power supply for the charging circuit block is CHGVCC(41PIN), and is independent from the other circuits. The resistance between RCHG (33PIN) and GND sets the charging current. This current is drawn from SEL (42PIN).

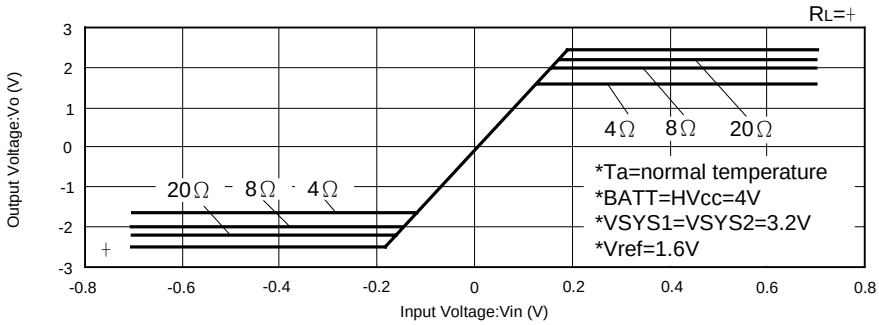
• A thermal shutdown circuit is provided, and when the chip temperature reaches 150℃ typ. the charging current is cut. The chip starts operating again at about 120℃ typ. .

■ TYPICAL CHARACTERISTIC

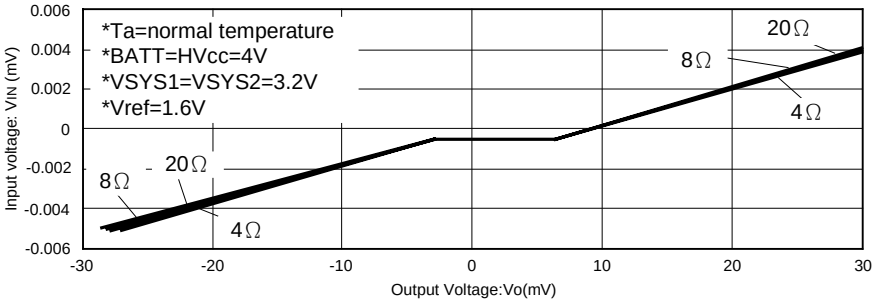
Input Load Fluctuation



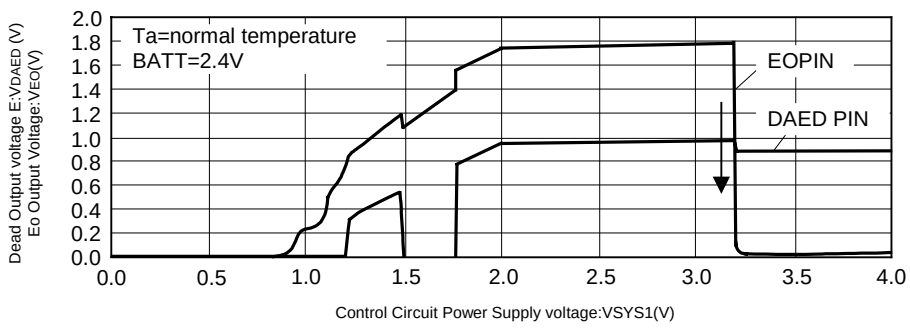
Input Load Fluctuation (ch2)



Dead Zone



Error Amp Output Voltage



Resete Pin Voltage