

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1,048,576-WORD BY 16-BIT/2,097,152-WORD BY 8-BIT FULL CMOS STATIC RAM

**DESCRIPTION**

The TC55W1600FT is a 16,777,216-bit static random access memory (SRAM) organized as 1,048,576 words by 16 bits/2,097,152 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.1 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 0.5  $\mu$ A standby current (at V<sub>DD</sub> = 3.0 V, T<sub>a</sub> = 25°C, maximum) when chip enable ( $\overline{CE1}$ ) is asserted high or ( $\overline{CE2}$ ) is asserted low. There are three control inputs.  $\overline{CE1}$  and  $\overline{CE2}$  are used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. Data byte control pin ( $\overline{LB}$ ,  $\overline{UB}$ ) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to 85°C, the TC55W1600FT can be used in environments exhibiting extreme temperature conditions. The TC55W1600FT is available in a plastic 48-pin thin-small-outline package (TSOP).

**FEATURES**

- Low-power dissipation  
Operating: 9.3 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.1 V
- Power down features using  $\overline{CE1}$  and  $\overline{CE2}$
- Data retention supply voltage of 1.5 to 3.1 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum):

3.1 V	10 $\mu$ A
3.0 V	5 $\mu$ A

- Access Times (maximum):

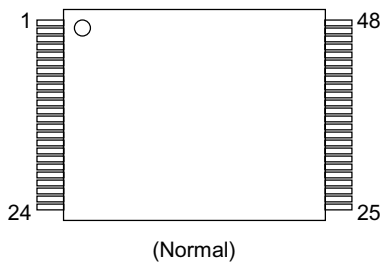
	TC55W1600FT	
	-55	-70
Access Time	55 ns	70 ns
$\overline{CE1}$ Access Time	55 ns	70 ns
$\overline{CE2}$ Access Time	55 ns	70 ns
$\overline{OE}$ Access Time	30 ns	35 ns

- Package:

TSOP 48-P-1220-0.50 (Weight: 0.52 g typ)

**PIN ASSIGNMENT (TOP VIEW)**

48 PIN TSOP



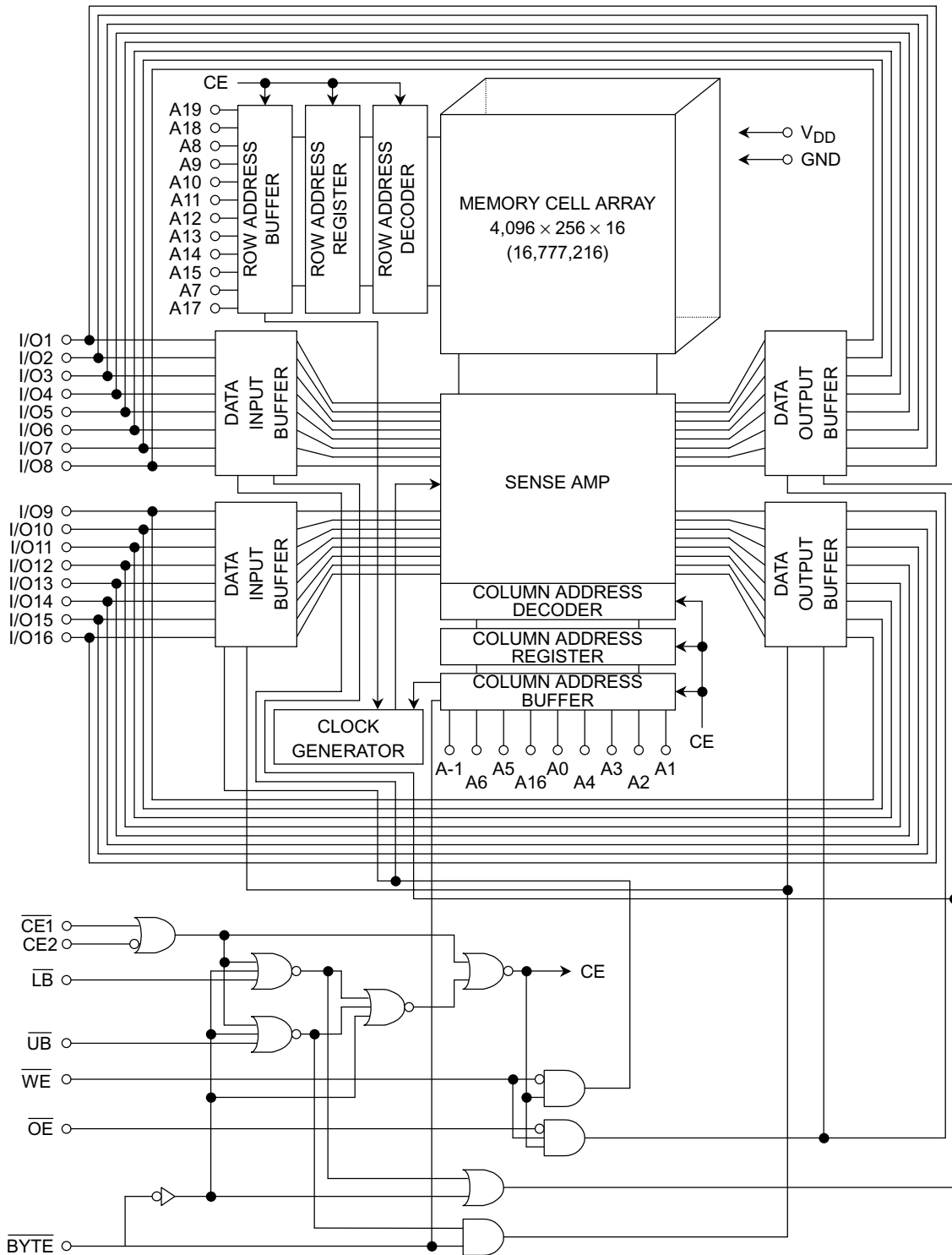
**PIN NAMES**

A0~A19	Address Inputs (Word Mode)
A-1~A19	Address Inputs (Byte Mode)
$\overline{CE1}$ , $\overline{CE2}$	Chip Enable
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$ , $\overline{UB}$	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
$\overline{BYTE}$	Byte ( $\times 8$ mode) Enable
V <sub>DD</sub>	Power
GND	Ground
NC	No Connection
NU	Not Used (Input)

\*: NU pin must be open or connected to GND.

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A15	A14	A13	A12	A11	A10	A9	A8	A19	NC	R/W	$\overline{CE2}$	NU	$\overline{UB}$	$\overline{LB}$	A18
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A17	A7	A6	A5	A4	A3	A2	A1	A0	$\overline{CE1}$	GND	$\overline{OE}$	I/O1	I/O9	I/O2	I/O10
Pin No.	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Pin Name	I/O3	I/O11	I/O4	I/O12	V <sub>DD</sub>	I/O5	I/O13	I/O6	I/O14	I/O7	I/O15	I/O8	I/O16 /A-1	GND	$\overline{BYTE}$	A16

**BLOCK DIAGRAM**



## OPERATING MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{BYTE}$	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O15	I/O16	POWER
Read	L	H	L	H	L	*	*	Output	High-Z	A-1	I <sub>DDO</sub>
	L	H	L	H	H	L	L	Output	Output	Output	I <sub>DDO</sub>
	L	H	L	H	H	H	L	High-Z	Output	Output	I <sub>DDO</sub>
	L	H	L	H	H	L	H	Output	High-Z	High-Z	I <sub>DDO</sub>
Write	L	H	*	L	L	*	*	Input	High-Z	A-1	I <sub>DDO</sub>
	L	H	*	L	H	L	L	Input	Input	Input	I <sub>DDO</sub>
	L	H	*	L	H	H	L	High-Z	Input	Input	I <sub>DDO</sub>
	L	H	*	L	H	L	H	Input	High-Z	High-Z	I <sub>DDO</sub>
Output Deselect	L	H	H	H	L	*	*	High-Z	High-Z	A-1	I <sub>DDO</sub>
	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	I <sub>DDO</sub>
	L	H	H	H	H	H	L	High-Z	High-Z	High-Z	I <sub>DDO</sub>
	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	I <sub>DDO</sub>
Standby	H	*	*	*	H or L	*	*	High-Z	High-Z	High-Z	I <sub>DDS</sub>
	*	L	*	*	H or L	*	*	High-Z	High-Z	High-Z	I <sub>DDS</sub>
	*	*	*	*	H	H	H	High-Z	High-Z	High-Z	I <sub>DDS</sub>

\* = don't care  
H = logic high  
L = logic low

## MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~3.9	V
V <sub>IN</sub>	Input Voltage	-0.3~3.9	V
V <sub>I/O</sub>	Input/Output Voltage	-0.5~V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.6	W
T <sub>solder</sub>	Soldering Temperature (10s)	260	°C
T <sub>stg</sub>	Storage Temperature	-55~150	°C
T <sub>opr</sub>	Operating Temperature	-40~85	°C

## DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	2.3	—	3.1	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	V <sub>DD</sub> × 0.22	V
V <sub>DH</sub>	Data Retention Supply Voltage	1.5	—	3.1	V

## DC CHARACTERISTICS (Ta = -40° to 85°C, VDD = 2.3 to 3.1 V)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V~V <sub>DD</sub>		—	—	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.4V		-1.0	—	—	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V		1.0	—	—	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$ or $\overline{LB} = \overline{UB} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ , V <sub>OUT</sub> = 0 V~V <sub>DD</sub>		—	—	±1.0	μA	
I <sub>DDO1</sub>	Operating Current	$\overline{CE1} = V_{IL}$ , $\overline{CE2} = V_{IH}$ , R/W = V <sub>IH</sub> , $\overline{LB} = \overline{UB} = V_{IL}$ , I <sub>OUT</sub> = 0 mA Other Input = V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub>	55 ns	—	—	60	mA
				70 ns	—	—	50	
				1 μs	—	—	10	
I <sub>DDO2</sub>	Operating Current	$\overline{CE1} = 0.2 V$ , $\overline{CE2} = V_{DD} - 0.2 V$ R/W = V <sub>DD</sub> - 0.2 V, $\overline{LB} = \overline{UB} = 0.2 V$ , I <sub>OUT</sub> = 0 mA Other Input = V <sub>DD</sub> - 0.2 V/0.2 V	t <sub>cycle</sub>	55 ns	—	—	55	mA
				70 ns	—	—	45	
				1 μs	—	—	5	
I <sub>DDS1</sub>	Standby Current	1) $\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$ (at $\overline{BYTE} \geq V_{DD} - 0.2 V$ or $\leq 0.2 V$ ) 2) $\overline{LB} = \overline{UB} = V_{IH}$ (at $\overline{BYTE} \geq V_{DD} - 0.2 V$ )		—	—	2	mA	
I <sub>DDS2</sub>		1) $\overline{CE1} = V_{DD} - 0.2 V$ , $\overline{CE2} = V_{DD} - 0.2 V$ (at $\overline{BYTE} \geq V_{DD} - 0.2 V$ or $\leq 0.2 V$ ) 2) $\overline{CE2} = 0.2 V$ (at $\overline{BYTE} \geq V_{DD} - 0.2 V$ or $\leq 0.2 V$ ) 3) $\overline{LB} = \overline{UB} = V_{DD} - 0.2 V$ , $\overline{CE1} = 0.2 V$ , $\overline{CE2} = V_{DD} - 0.2 V$ (at $\overline{BYTE} \geq V_{DD} - 0.2 V$ )	V <sub>DD</sub> = 3.1 V	Ta = 25°C	—	—	1	μA
				Ta = -40~85°C	—	—	10	
			V <sub>DD</sub> = 3.0 V	Ta = 25°C	—	0.05	0.5	
				Ta = -40~40°C	—	—	1	
Ta = -40~85°C	—	—	5					

## CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

## AC CHARACTERISTICS AND OPERATING CONDITIONS

( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $3.1\text{ V}$ )

### READ CYCLE

SYMBOL	PARAMETER	TC55W1600FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
$t_{RC}$	Read Cycle Time	55	—	70	—	ns
$t_{ACC}$	Address Access Time	—	55	—	70	
$t_{CO1}$	Chip Enable( $\overline{CE1}$ ) Access Time	—	55	—	70	
$t_{CO2}$	Chip Enable(CE2) Access Time	—	55	—	70	
$t_{OE}$	Output Enable Access Time	—	30	—	35	
$t_{BA}$	Data Byte Control Access Time	—	55	—	70	
$t_{COE}$	Chip Enable Low to Output Active	5	—	5	—	
$t_{OEE}$	Output Enable Low to Output Active	0	—	0	—	
$t_{BE}$	Data Byte Control Low to Output Active	0	—	0	—	
$t_{OD}$	Chip Enable High to Output High-Z	—	25	—	30	
$t_{ODO}$	Output Enable High to Output High-Z	—	25	—	30	
$t_{BD}$	Data Byte Control High to Output High-Z	—	25	—	30	
$t_{OH}$	Output Data Hold Time	10	—	10	—	

### WRITE CYCLE

SYMBOL	PARAMETER	TC55W1600FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
$t_{WC}$	Write Cycle Time	55	—	70	—	ns
$t_{WP}$	Write Pulse Width	45	—	50	—	
$t_{CW}$	Chip Enable to End of Write	50	—	60	—	
$t_{BW}$	Data Byte Control to End of Write	50	—	60	—	
$t_{AS}$	Address Setup Time	0	—	0	—	
$t_{WR}$	Write Recovery Time	0	—	0	—	
$t_{ODW}$	R/W Low to Output High-Z	—	20	—	25	
$t_{OEW}$	R/W High to Output Active	0	—	0	—	
$t_{DS}$	Data Setup Time	25	—	30	—	
$t_{DH}$	Data Hold Time	0	—	0	—	

### AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	$V_{DD} - 0.2\text{ V}$ , 0.2 V
Timing measurements	$V_{DD} \times 0.5$
Reference level	$V_{DD} \times 0.5$
$t_R$ , $t_F$	5 ns

## AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = -40° to 85°C, V<sub>DD</sub> = 2.3 to 3.1 V)

### READ CYCLE

SYMBOL	PARAMETER	TC55W1600FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	70	—	85	—	ns
t <sub>ACC</sub>	Address Access Time	—	70	—	85	
t <sub>CO1</sub>	Chip Enable( $\overline{CE1}$ ) Access Time	—	70	—	85	
t <sub>CO2</sub>	Chip Enable(CE2) Access Time	—	70	—	85	
t <sub>OE</sub>	Output Enable Access Time	—	35	—	45	
t <sub>BA</sub>	Data Byte Control Access Time	—	70	—	85	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	—	5	—	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	—	0	—	
t <sub>BE</sub>	Data Byte Control Low to Output Active	0	—	0	—	
t <sub>OD</sub>	Chip Enable High to Output High-Z	—	30	—	35	
t <sub>ODO</sub>	Output Enable High to Output High-Z	—	30	—	35	
t <sub>BD</sub>	Data Byte Control High to Output High-Z	—	30	—	35	
t <sub>OH</sub>	Output Data Hold Time	10	—	10	—	

### WRITE CYCLE

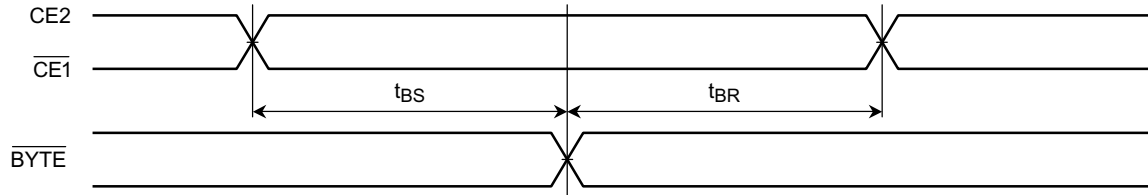
SYMBOL	PARAMETER	TC55W1600FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	70	—	85	—	ns
t <sub>WP</sub>	Write Pulse Width	50	—	55	—	
t <sub>CW</sub>	Chip Enable to End of Write	60	—	70	—	
t <sub>BW</sub>	Data Byte Control to End of Write	60	—	70	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	R/W Low to Output High-Z	—	25	—	30	
t <sub>OEW</sub>	R/W High to Output Active	0	—	0	—	
t <sub>DS</sub>	Data Setup Time	30	—	35	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

### AC TEST CONDITIONS

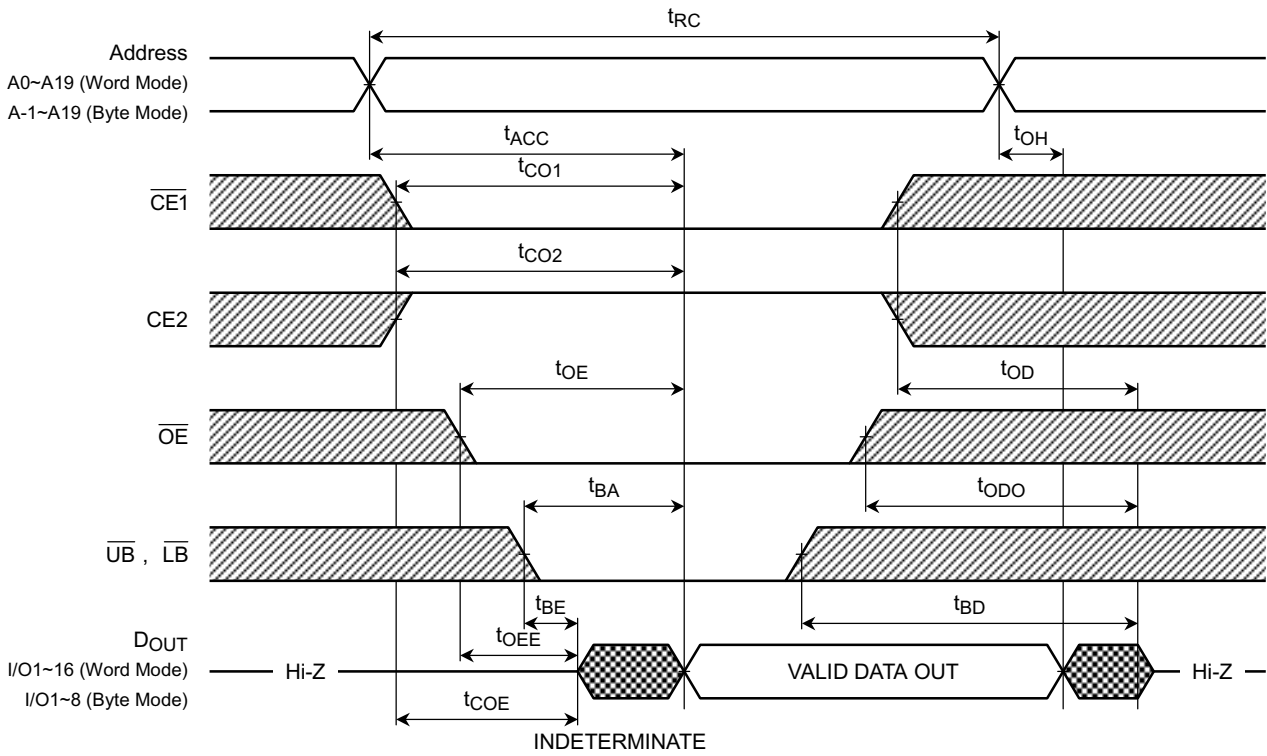
PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	V <sub>DD</sub> - 0.2 V, 0.2 V
Timing measurements	V <sub>DD</sub> × 0.5
Reference level	V <sub>DD</sub> × 0.5
t <sub>R</sub> , t <sub>F</sub>	5 ns

**BYTE FUNCTION**

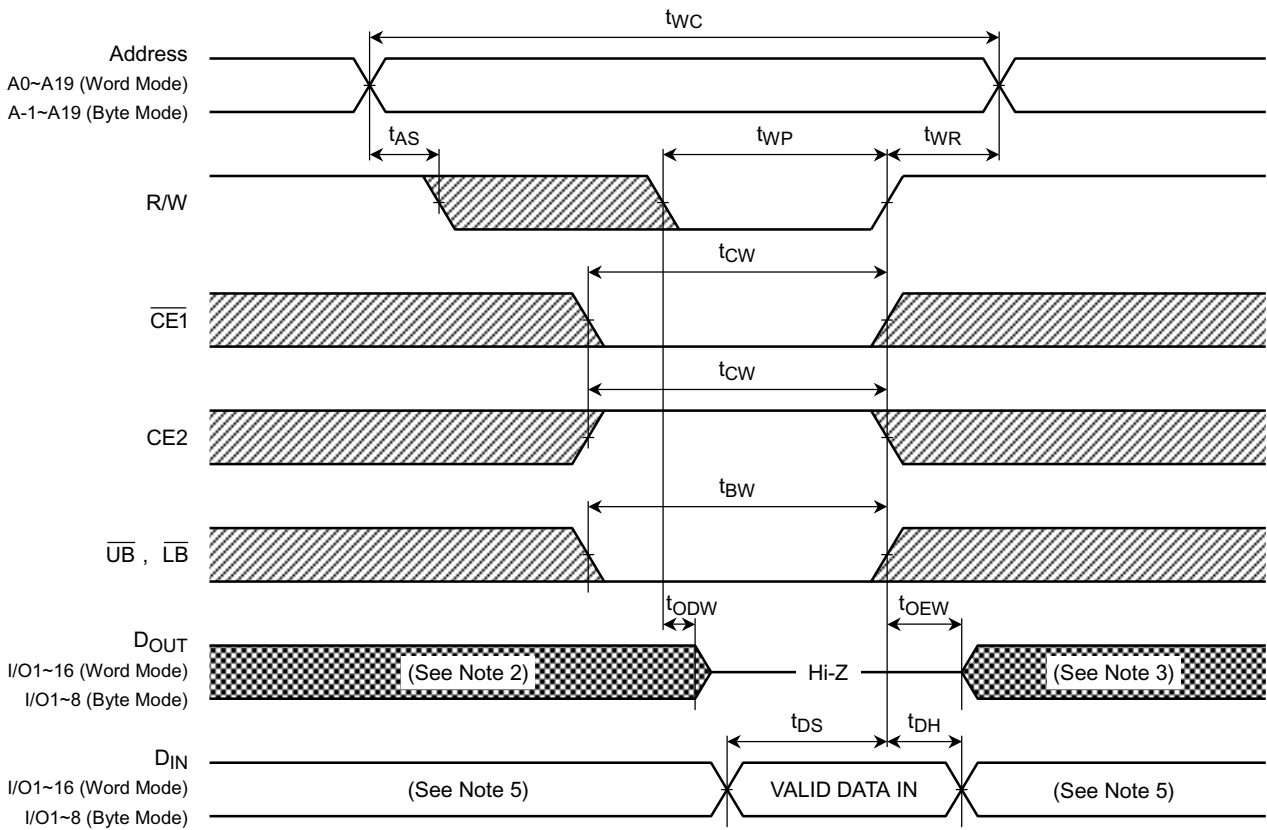
SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{BS}$	$\overline{BYTE}$ Setup Time	5	—	ms
$t_{BR}$	$\overline{BYTE}$ Recovery Time	5	—	ms

**TIMING DIAGRAMS** **$\overline{BYTE}$** 

READ CYCLE (See Note 1)

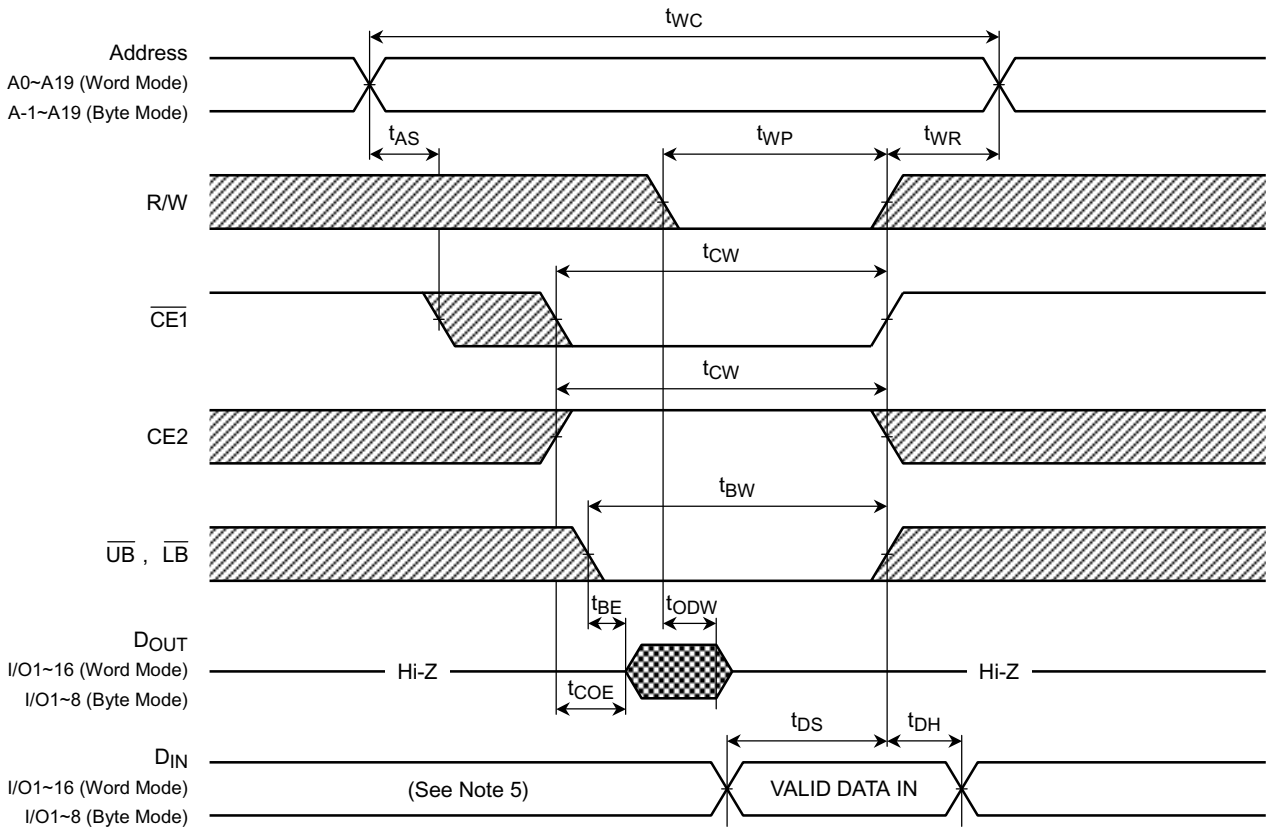


WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)

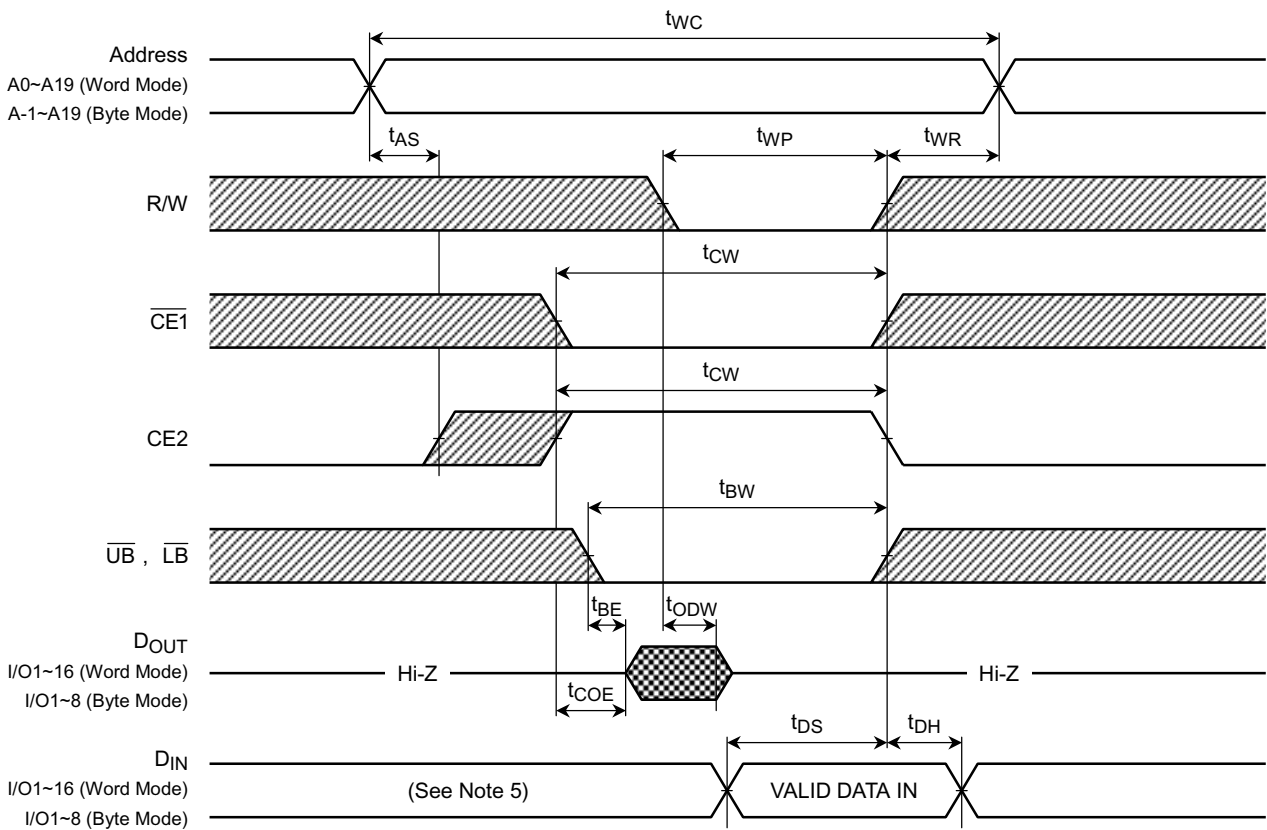




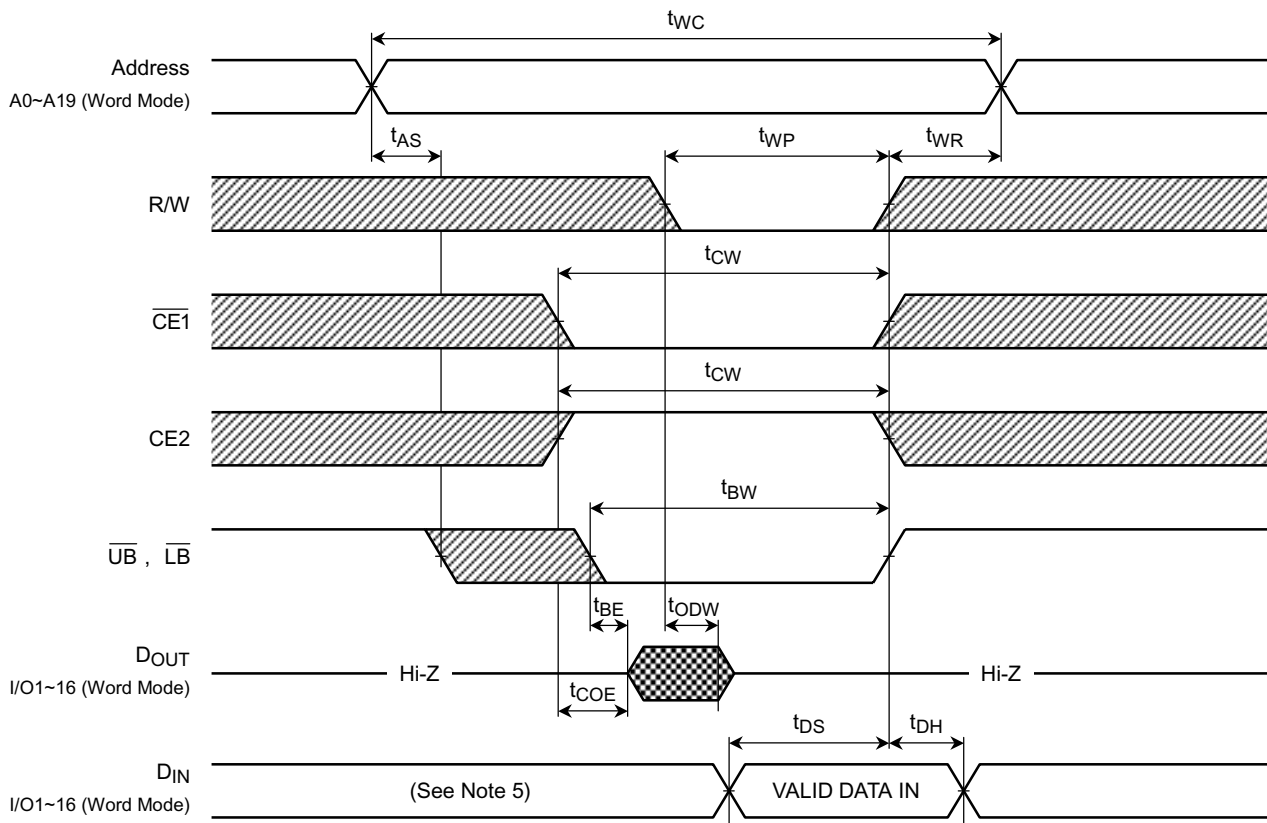
WRITE CYCLE 2 ( $\overline{CE1}$  CONTROLLED) (See Note 4)



WRITE CYCLE 3 ( $CE2$  CONTROLLED) (See Note 4)



WRITE CYCLE 4 ( $\overline{UB}$ ,  $\overline{LB}$  CONTROLLED) (See Note 4)



Note:

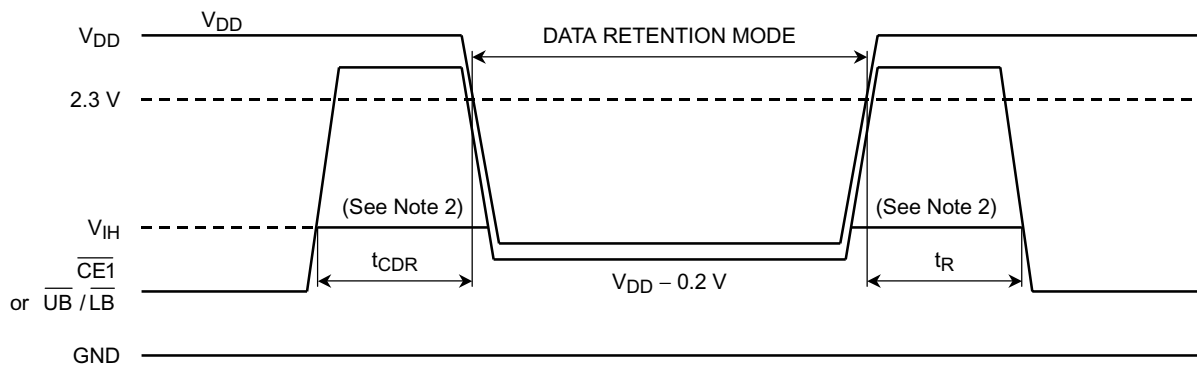
- (1) R/W remains HIGH for the read cycle.
- (2) If  $\overline{CE1}$  or  $\overline{UB}/\overline{LB}$  goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If  $\overline{CE1}$  or  $\overline{UB}/\overline{LB}$  goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

## DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

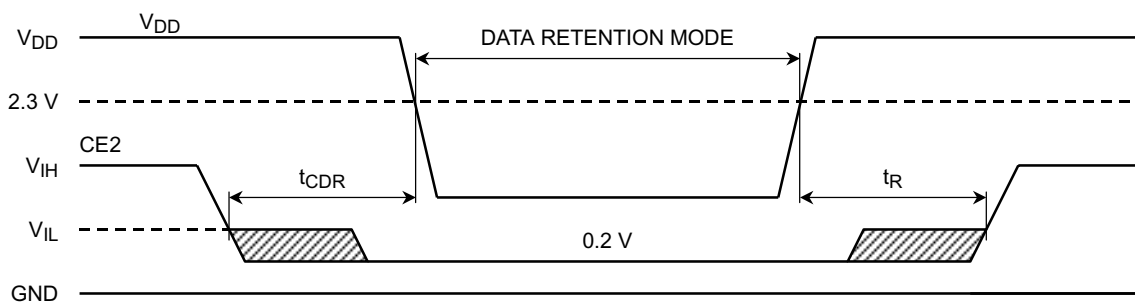
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage		1.5	—	3.1	V	
I <sub>DDSS2</sub>	Standby Current	V <sub>DH</sub> = 3.1 V	Ta = -40~85°C	—	—	10	μA
		V <sub>DH</sub> = 3.0 V	Ta = -40~40°C	—	—	1	
			Ta = -40~85°C	—	—	5	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time		0	—	—	ns	
t <sub>R</sub>	Recovery Time		t <sub>RC</sub> (See Note)	—	—	ns	

Note: Read cycle time

### CE1, UB/LB CONTROLLED DATA RETENTION MODE (See Note 1,4)



### CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



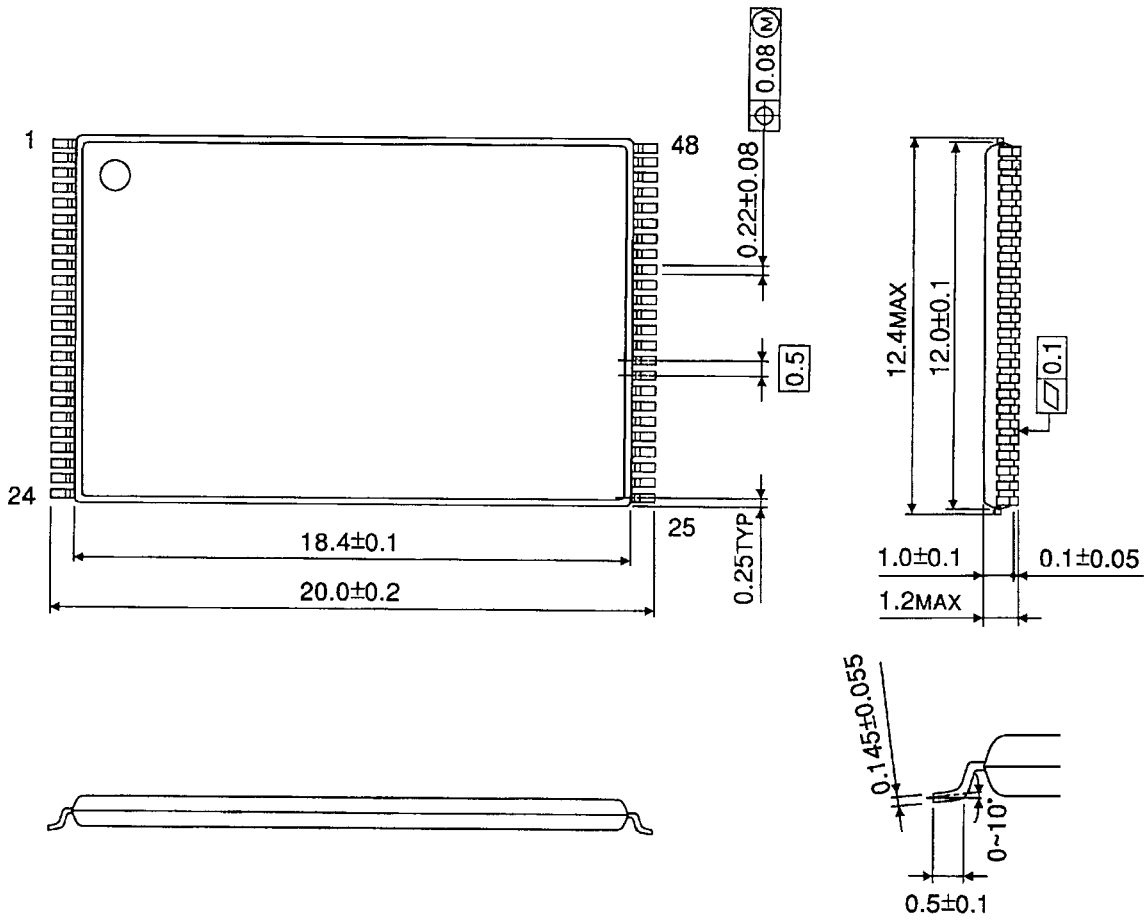
Note:

- (1) In  $\overline{CE1}$  or  $\overline{UB/LB}$  controlled data retention mode, minimum standby current mode is entered when  $CE2 \leq 0.2 \text{ V}$  or  $CE2 \geq V_{DD} - 0.2 \text{ V}$ .
- (2) When  $\overline{CE1}$  or  $\overline{UB/LB}$  is operating at the V<sub>IH</sub> minimum level, the operating current is given by I<sub>DDSS1</sub> during the transition of V<sub>DD</sub> from 3.1 V to 2.4 V.
- (3) In CE2 controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V.
- (4) In  $\overline{UB/LB}$  controlled data retention mode, minimum standby current mode is entered when  $\overline{CE1}/CE2 \leq 0.2 \text{ V}$  or  $\overline{CE1}/CE2 \geq V_{DD} - 0.2 \text{ V}$ .

## PACKAGE DIMENSIONS

TSOP I 48-P-1220-0.50

Unit : mm



Weight: 0.52 g (typ)

**RESTRICTIONS ON PRODUCT USE**

000707EBA

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