



ST662A

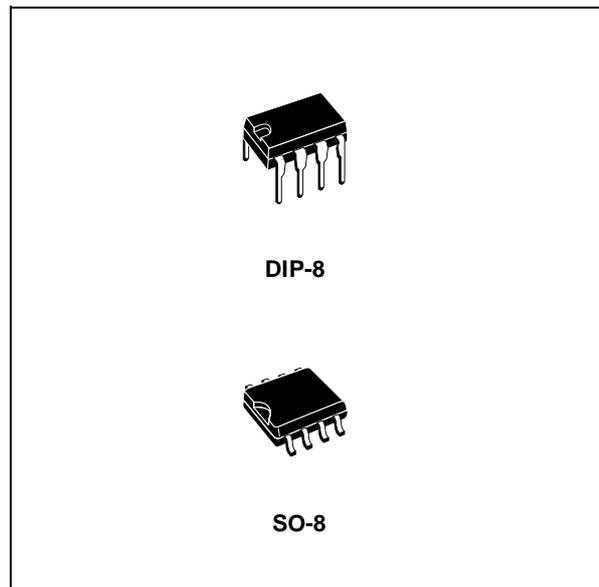
DC-DC CONVERTER FROM 5V TO 12V, 0.03A FOR FLASH MEMORY PROGRAMMING SUPPLY

- OUTPUT VOLTAGE: $12V \pm 5\%$
- SUPPLY VOLTAGE RANGE: 4.5V TO 5.5V
- GUARANTEED OUTPUT CURRENT UP TO 30mA
- VERY LOW QUIESCENT CURRENT: 100mA
- LOGIC CONTROLLED ELECTRONIC SHUTDOWN: $1\mu A$
- JUST CAPACITORS NEEDED (NO INDUCTOR)

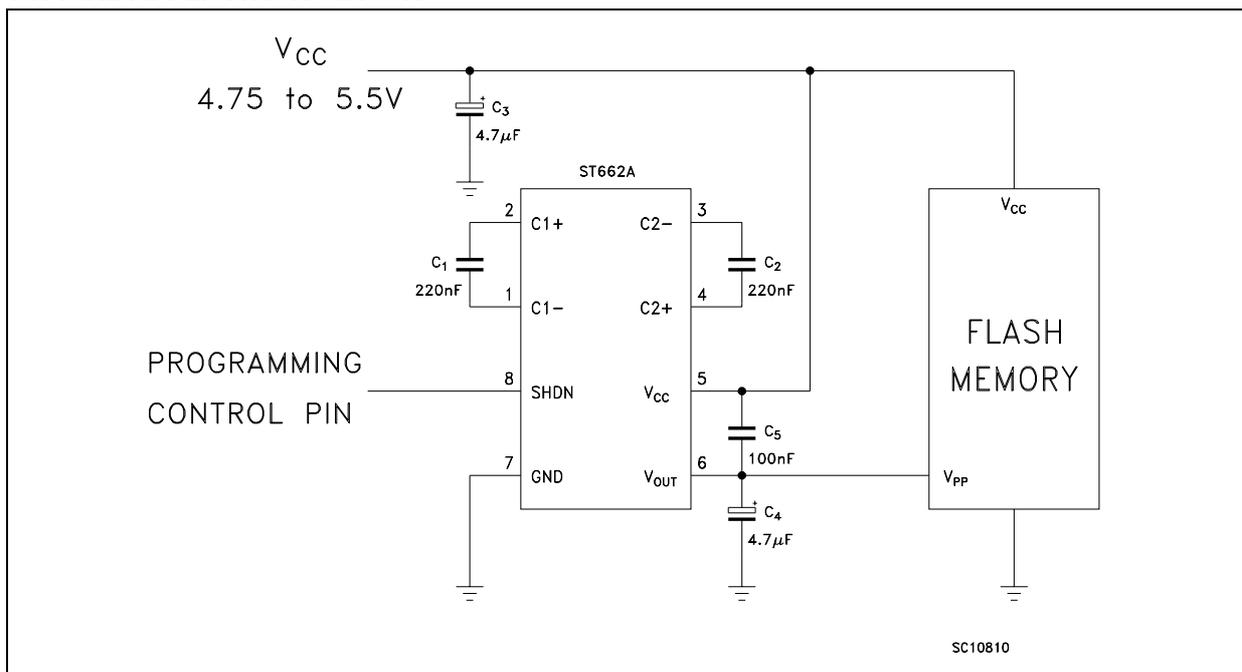
DESCRIPTION

The ST662A is a regulated charge pump DC-DC converter. It provides $12V \pm 5\%$ output voltage to program byte-wide flash memory, and can supply 30mA output current from input as low as 4.75V.

A logic controlled shut down pin that interfaces directly with microprocessor reduces the supply current to only $1\mu A$.



TYPICAL APPLICATION CIRCUIT



ST662A

ABSOLUTE MAXIMUM RATINGS

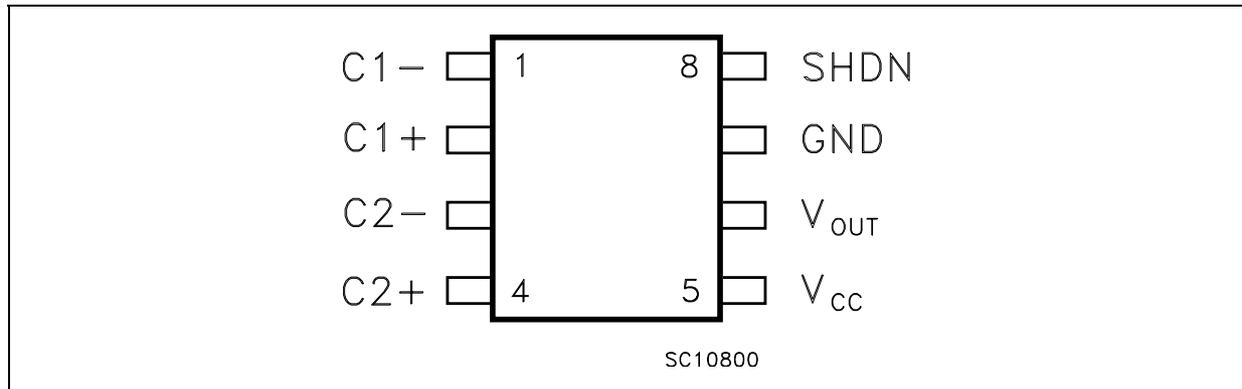
Symbol	Parameter	Value	Unit
V_{CC}	DC Input Voltage to GND	-0.3 to 6	V
SHDN	Shutdown Voltage	-0.3 to $V_{CC}+0.3$	V
I_O	Output Current Continuous	50	mA
P_{tot}	Power Dissipation	500	mW
T_{op}	Operating Ambient Temperature Range(for AC SERIES) (for AB SERIES)	-0 to 70 -40 to 85	°C
T_{stg}	Storage Temperature Range	-40 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

Symbol	Parameter	SO-8	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	20	°C/W

CONNECTION DIAGRAM (top view)



ORDERING CODES

TYPE	DIP-8	SO-8 (*)
ST662AB	ST662ABN	ST662ABD
ST662AC	ST662ACN	ST662ACD

(*) AVAILABLE IN TAPE & REEL WITH "-TR" SUFFIX.

PIN DESCRIPTION

PIN N°	Symbol	Name and Function
1	C1-	Negative Terminal For The First Charge Pump Capacitor
2	C1+	Positive Terminal For The First Charge Pump Capacitor
3	C2-	Negative Terminal For The Second Charge Pump Capacitor
4	C2+	Positive Terminal For The Second Charge Pump Capacitor
5	V_{CC}	Supply Voltage
6	V_{OUT}	12V Output Voltage $V_{OUT} = V_{CC}$ When in Shutdown Mode
7	GND	Ground
8	SHDN	Active High C-MOS logic level Shutdown Input. SHDN is internally pulled up to V_{CC} . Connect to GND for Normal Operation. In Shutdown mode the charge pumps are turned off and $V_{OUT} = V_{CC}$

ELECTRICAL CHARACTERISTICS (refer to the test circuits, $V_{CC} = 4.5V$ to $5.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise specified. Typical Value are referred at $T_A = 25^\circ C$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	$I_O = 0$ to 20 mA	11.4	12	12.6	V
		$I_O = 0$ to 30 mA, $V_{CC} = 4.75$ to 5.5 V	11.4	12	12.6	
I_{Q1}	Quiescent Current	NO LOAD, $V_{SHDN} = 0$		100	500	μA
I_{Q2}	Shutdown Current	NO LOAD, $V_{SHDN} = V_{CC}$		1	10	μA
I_{SH}	Shutdown Pin Current	$V_{SHDN} = 0$, $V_{CC} = 5V$	-50	-12	-5	μA
		$V_{SHDN} = V_{CC} = 5V$		0		μA
V_{IL}	Shutdown Input Low Threshold				0.4	V
V_{IH}	Shutdown Input High Threshold		2.4			V
f_O	Oscillator Frequency	$V_{CC} = 5$ V, $I_O = 30$ mA		400		KHz
ν	Power Efficiency	$V_{CC} = 5$ V, $I_O = 30$ mA		72		%
R_{SW}	$V_{CC} - V_{OUT}$ Switch Impedance	$V_{SHDN} = V_{CC} = 5V$, $I_O = 100$ μA		1	2	$K\Omega$

Figure 1 : Output Voltage vs Temperature

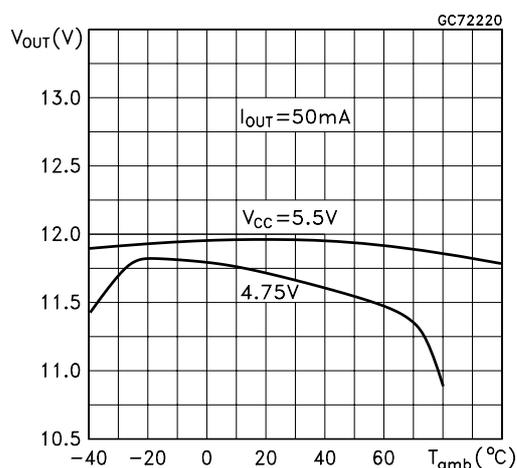


Figure 2 : Output Voltage vs Temperature

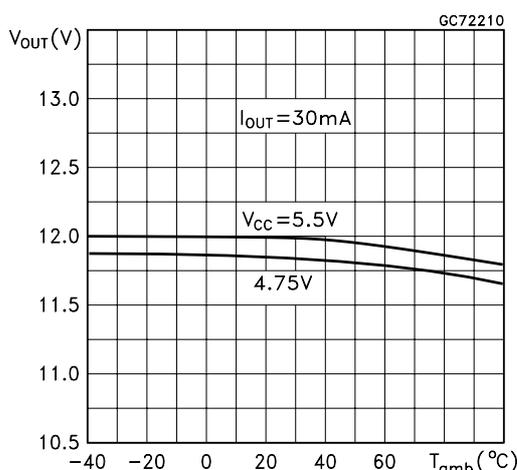


Figure 3 : Supply Current vs Temperature

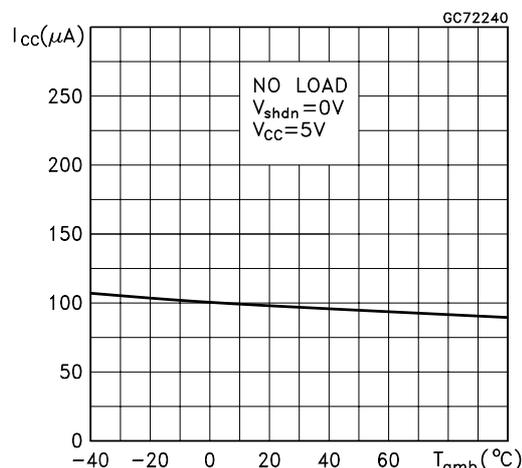


Figure 4 : Supply Current vs Supply Voltage

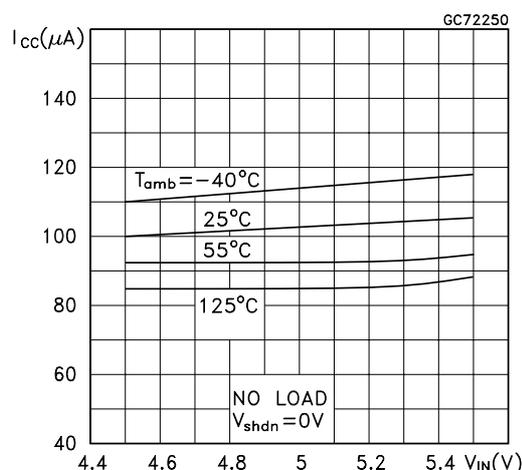


Figure 5 : SHDN Pin Current vs Temperature

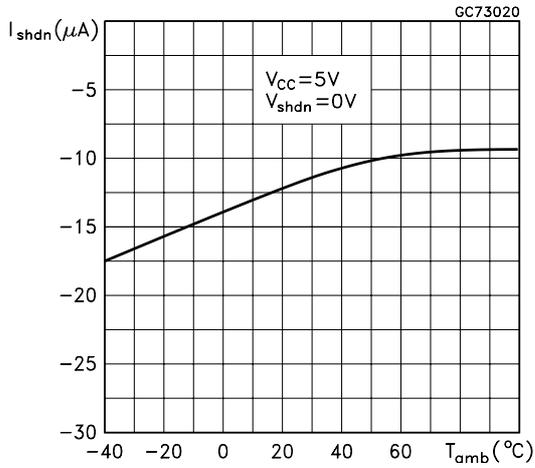


Figure 7 : Output Voltage vs Shutdown Input Voltage

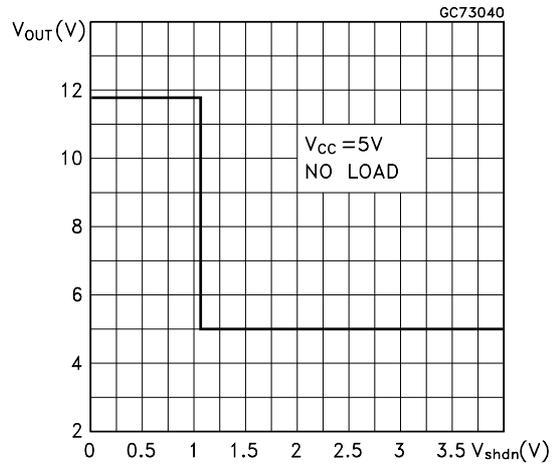


Figure 6 : Output Voltage vs Shutdown Input Voltage

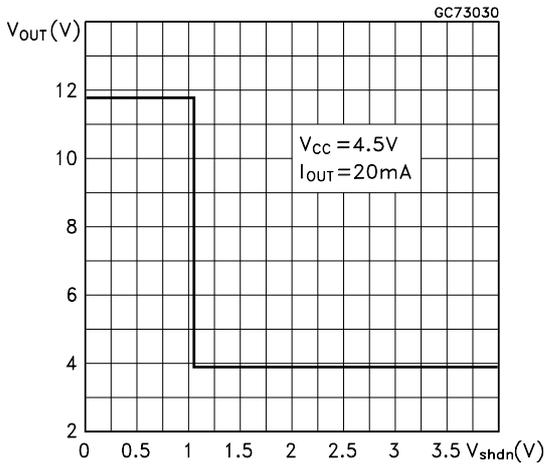


Figure 8 : Output Voltage vs Shutdown Input Voltage

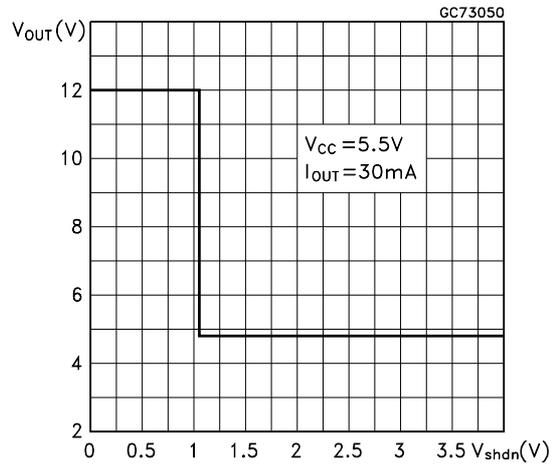
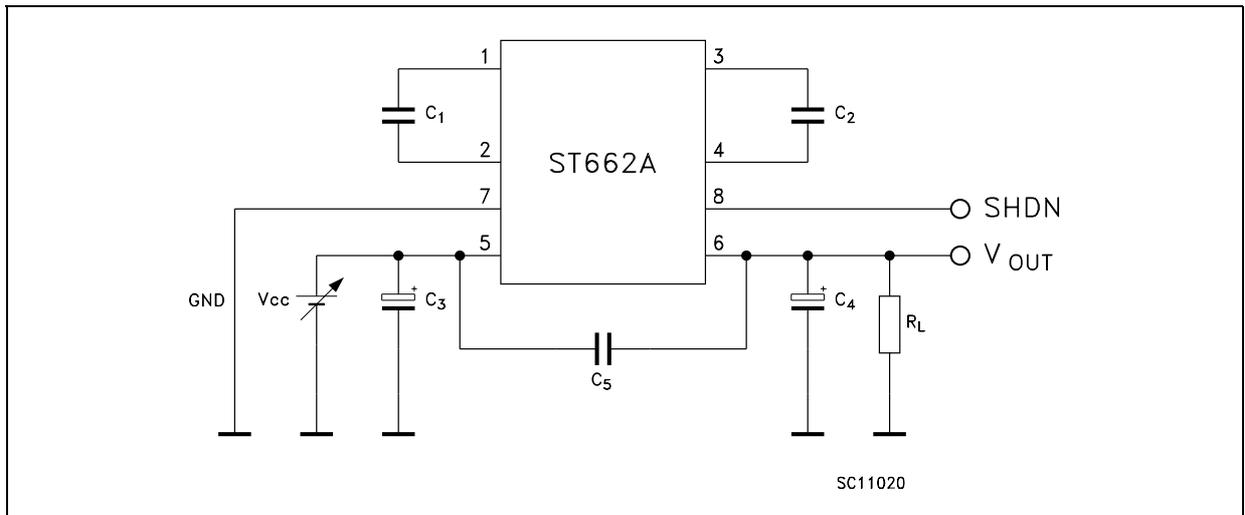


Figure 9 : Test Circuit



DESCRIPTION

The ST662 is an IC developed to provide a 12V regulated output 30mA from voltage input as low as 4.75 without any inductors. It is useful for a wide range of applications and its performances makes it ideal for flash memory programming supply.

An evaluation kit is provided to facilitate the application. This include a single-side demo board designed for surface-mount components. The operating principle of ST662 (see fig. 10) is to charge C1 and C2 capacitor by closing the S1 switch (while S2 is opened) at the V_{CC} voltage. After S1 will be opened and S2 closed so that C1 and C2 capacitors are placed in series one to each other, and both are in series with V_{IN}. The sum of V_{C1} and V_{C2} and V_I is applied to the capacitor C4. This works as voltage triple. An amplifier error checks the output voltage and blocks the oscillator if the output voltage is greater than 12V. The shutdown pin is internally pulled to V_{CC}. When it is held low the output voltage rises to +12V. Fig.11 shows the transition time of the shut down pin when the V_{SHDN} goes from 5V to 0V. Input logic levels of this input are CMOS compatible Applying a logic high at this input, the V_{OUT} oscillator will be blocked and the V_{OUT} will reach the V_I value by D1. In this condition I_{CC} will be low as 1µA. The fig.12 shows the transition time of the shut down pin when the V_{SHDN} goes from 0V to 5V.

Figure 10 : Operating Principle Circuit

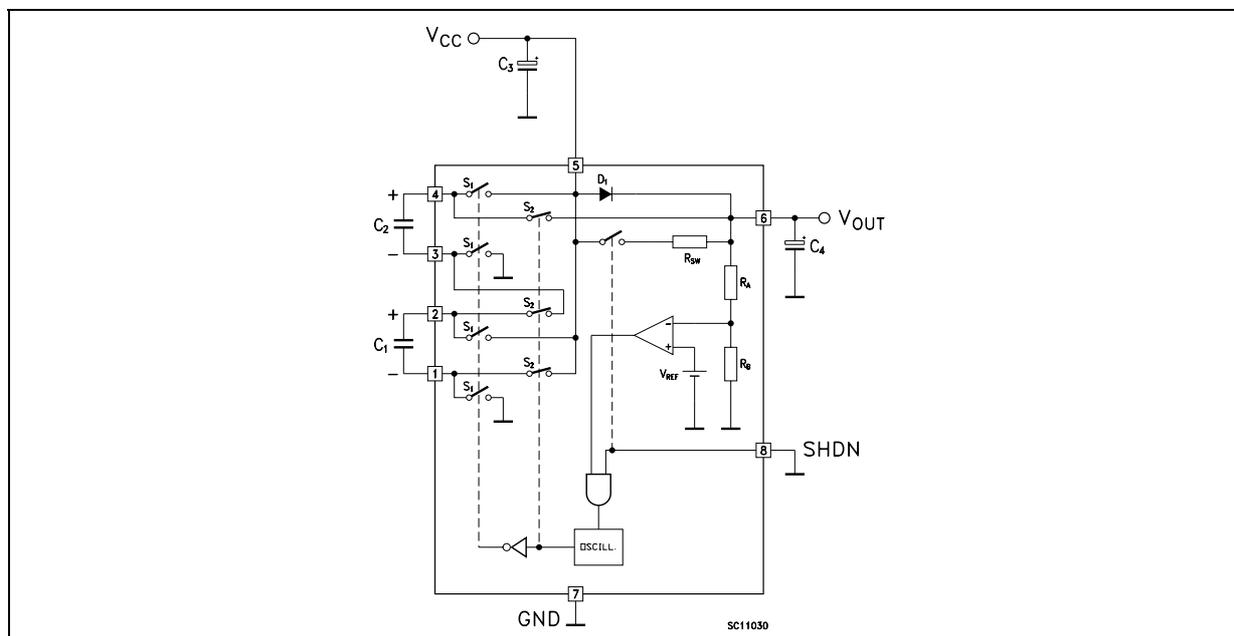
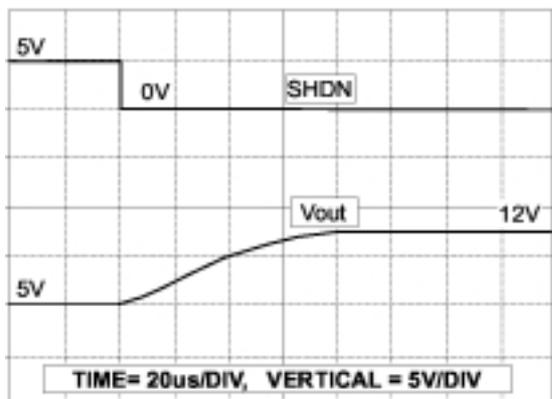
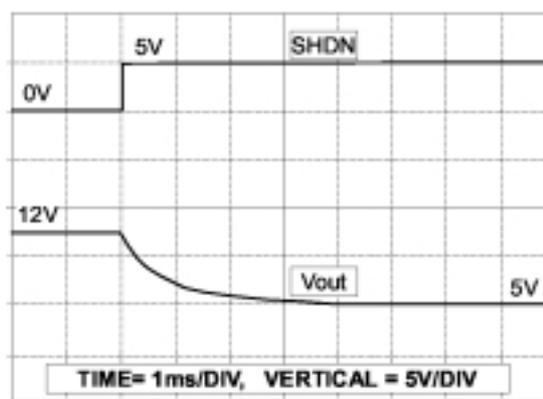


Figure 11 : Exiting Shutdown

Figure 12 : Entering Shutdown



NOTE: V_{CC} = 5 V, I_{OUT} = 200 µA



NOTE: V_{CC} = 5 V, I_{OUT} = 200 µA

APPLICATION CIRCUIT

Based on fast charge/discharge of capacitors, this circuit involves high di/dt values limited only by R_{ON} of switches. This implies a critical layout design due to the need to minimize inductive paths and place capacitors as close as possible to the device.

A good layout design is strongly recommended for noise reason. For best performance, use very short connections to the capacitors and the values shown in table 1.

C3 and C4 must have low ESR in order to minimize the output ripple. Their values can be reduced to $2\mu\text{F}$ and $1\mu\text{F}$, respectively, when using ceramic capacitors, but must be of $10\mu\text{F}$ or larger if aluminium electrolytic are chosen.

C5 must be placed as close to the device as possible and could be omitted if very low output noise performance are not required.

Fig 13 and Fig 14 show, respectively, our EVALUATION kit layout and the relatively.

Figure 13 : KIT Lay-out

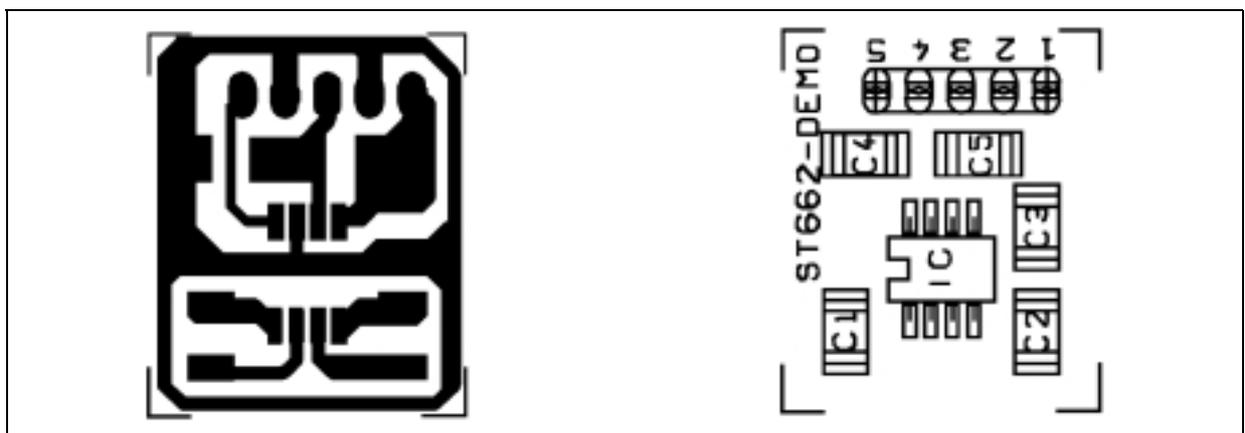


Figure 14 : Electrical Schematic

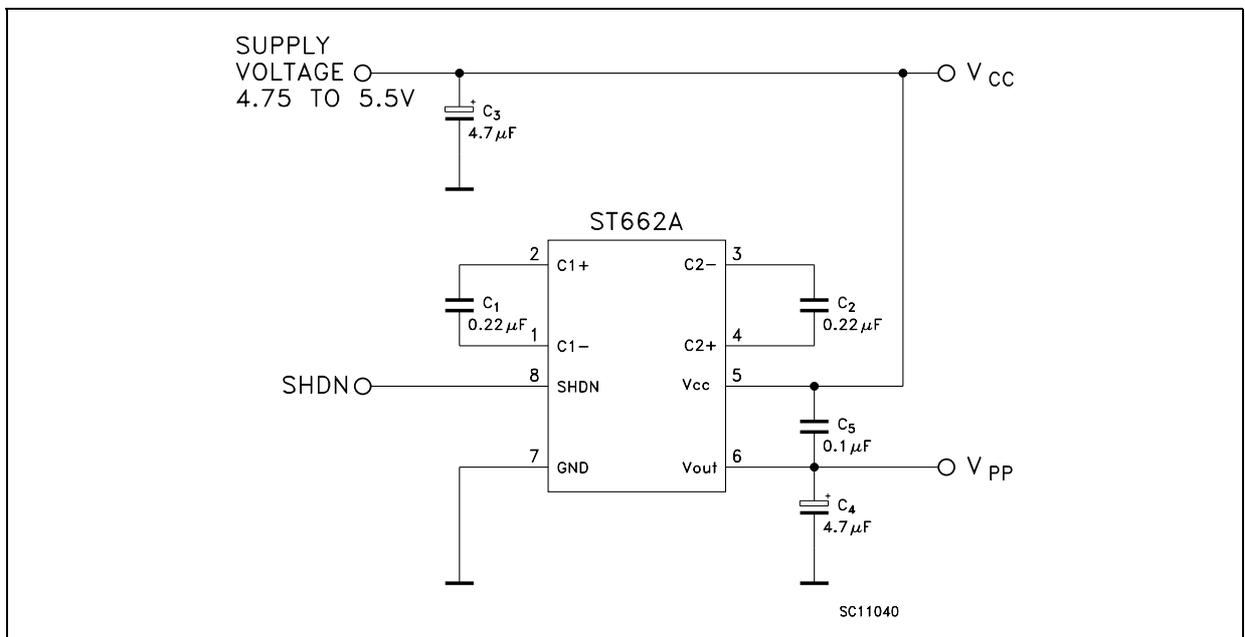


TABLE 1: List of Components

CAPACITOR	TYPE	VALUE (μF)
Charge Pump C1	Ceramic	0.22
Charge Pump C1	Ceramic	0.22
Input C3	Electrolytic Tantalum	4.7
Output C4	Electrolytic Tantalum	4.7
Decoupling C5	Ceramic	0.1

ST662A OUTPUT PERFORMANCE

Figure 15 : Output Voltage vs Output Current

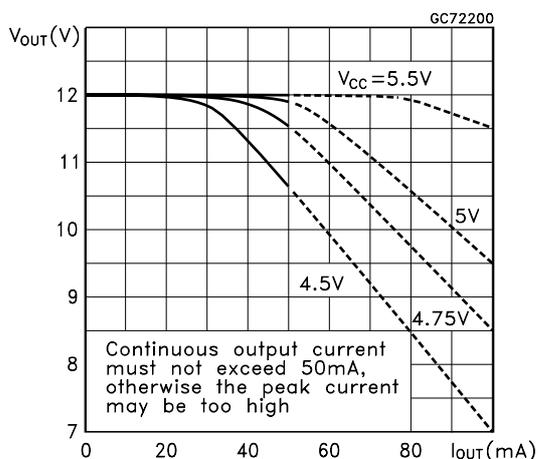


Figure 17 : Load Transient Response

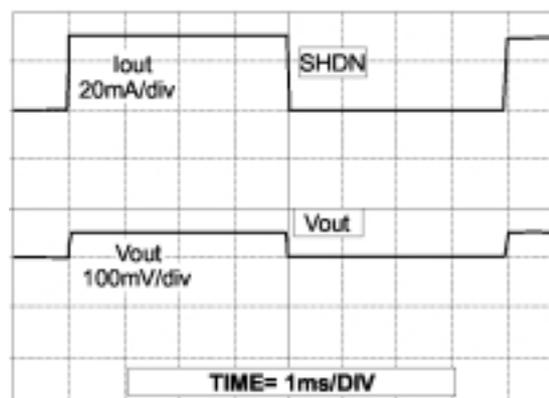


Figure 16 : Efficiency vs Output Current

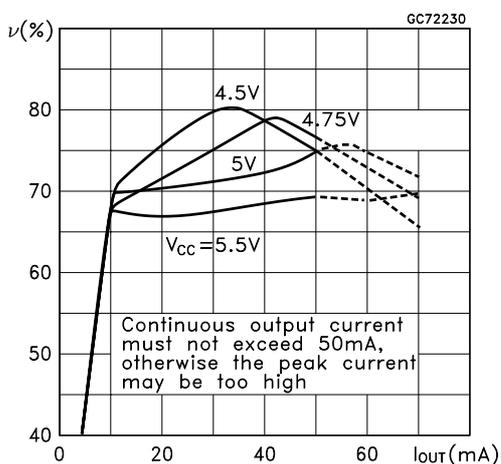
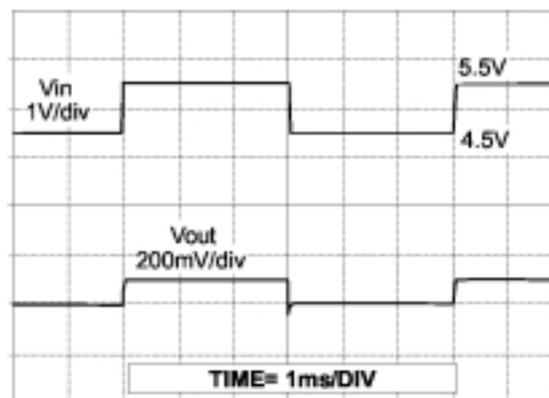


Figure 18 : Load Transient Response



HOW TO INCREASE OUTPUT CURRENT OR OUTPUT VOLTAGE CAPABILITY

Current capability is limited by R_{ON} of internal switches. It is possible to increase it connecting in parallel two or more ST662A devices; each one of them can supply 30mA. The figure 19 shows the electric schematic. The capacitors C_3 , C_4 and C_5 must be placed very close to the ICs on the board. If this is not possible, you can place two different capacitors, each of them of half value, very close to the respective integrated circuit.

Fig. 21 show the Output Current capability of the proposed circuit.

If an output voltage greater than 12V is required, it's possible to realize the circuit of the following diagram (figure 20). The relevant Output Current capability is shown in figure 22 in which is shown the output voltage vs load current.

Figure 19 : Application Circuit for Two ST662A in Parallel

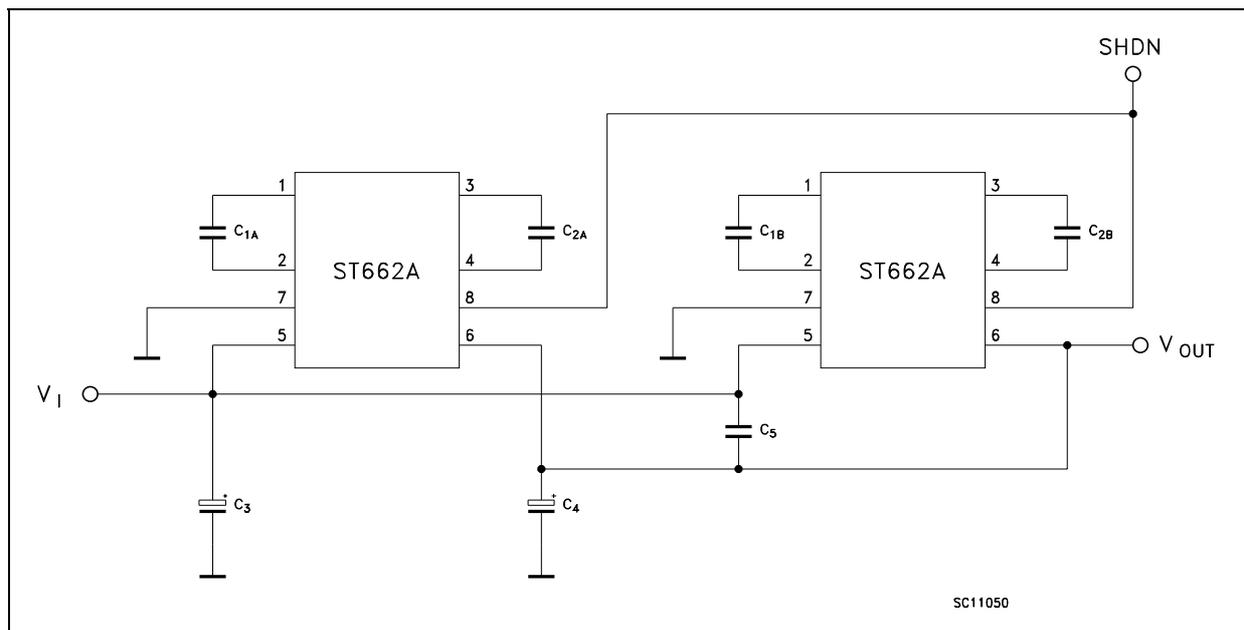


TABLE 2: List of Components

CAPACITOR	TYPE	VALUE (μ F)
C1A	Ceramic	0.22
C2A	Ceramic	0.22
C1B	Ceramic	0.22
C2B	Ceramic	0.22
C3	Electrolytic Tantalum	10
C4	Electrolytic Tantalum	10
C5	Ceramic	0.22

Figure 20 : Application Circuit for Output Voltage greater than 12V

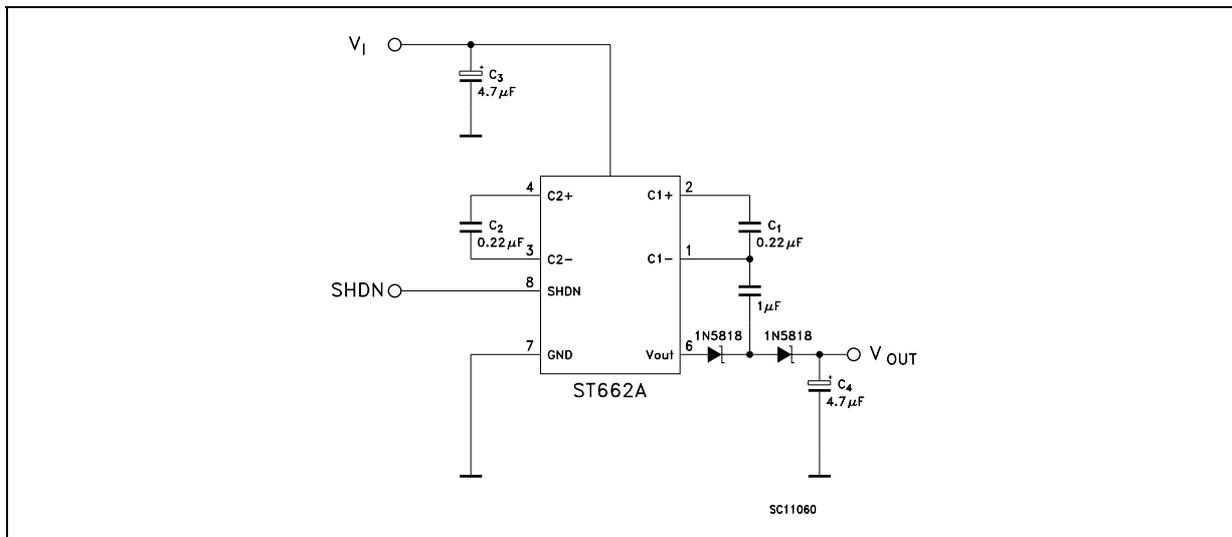


Figure 21 : Output Voltage for the Application with Two Device in Parallel

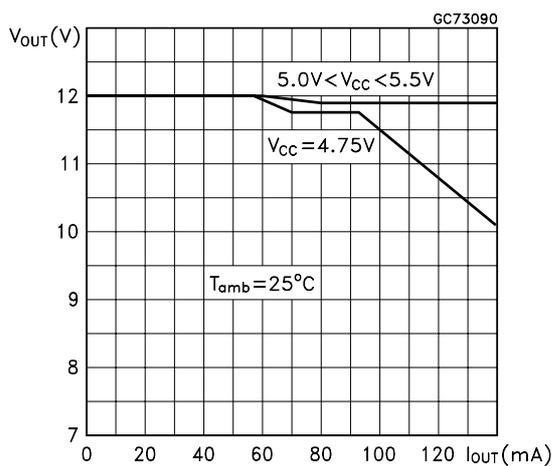
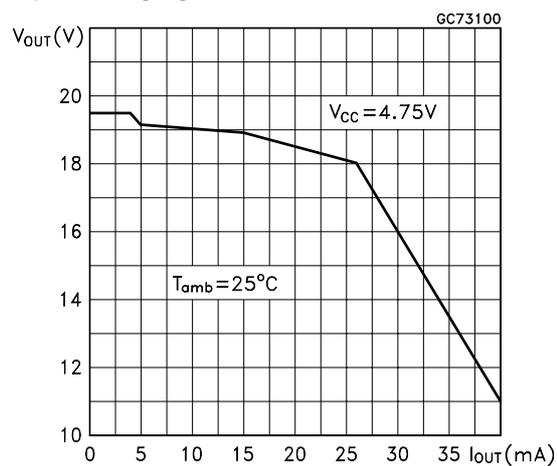
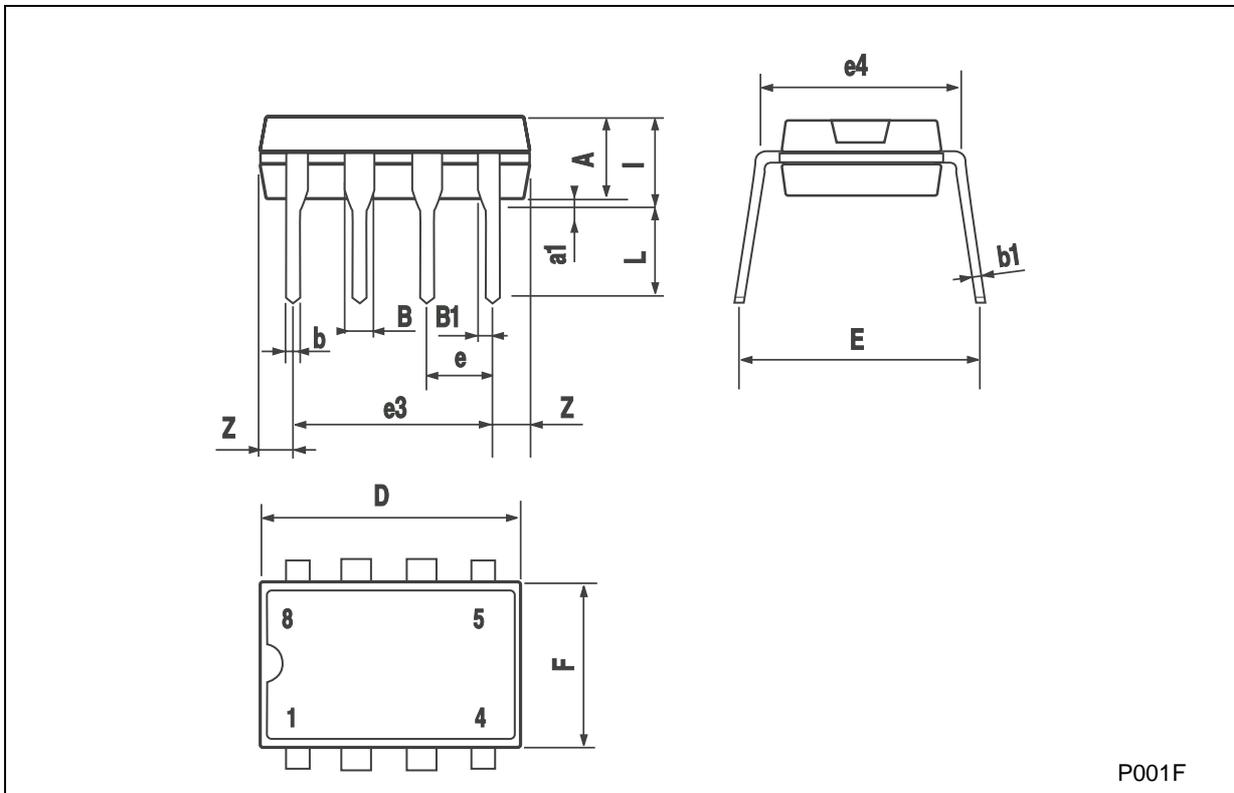


Figure 22 : Output Voltage for Application with Output Voltage greater than 12V



Plastic DIP-8 MECHANICAL DATA

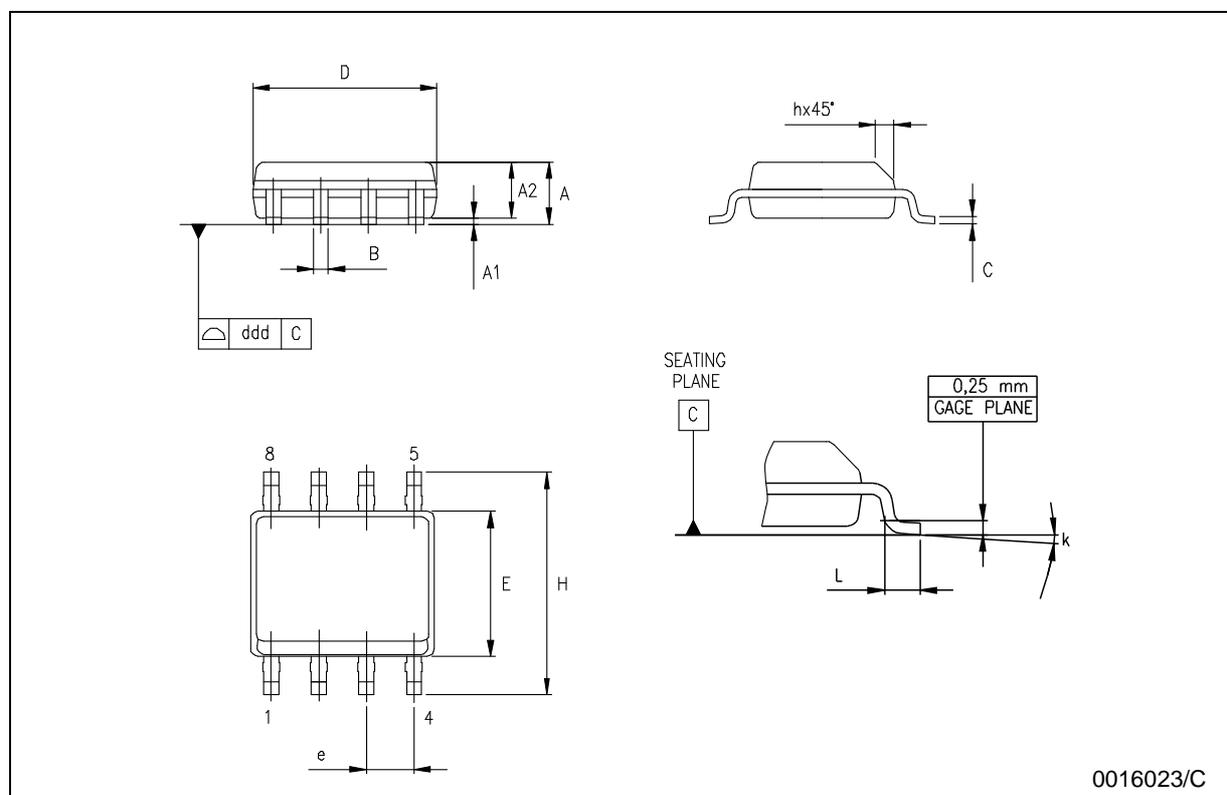
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063



P001F

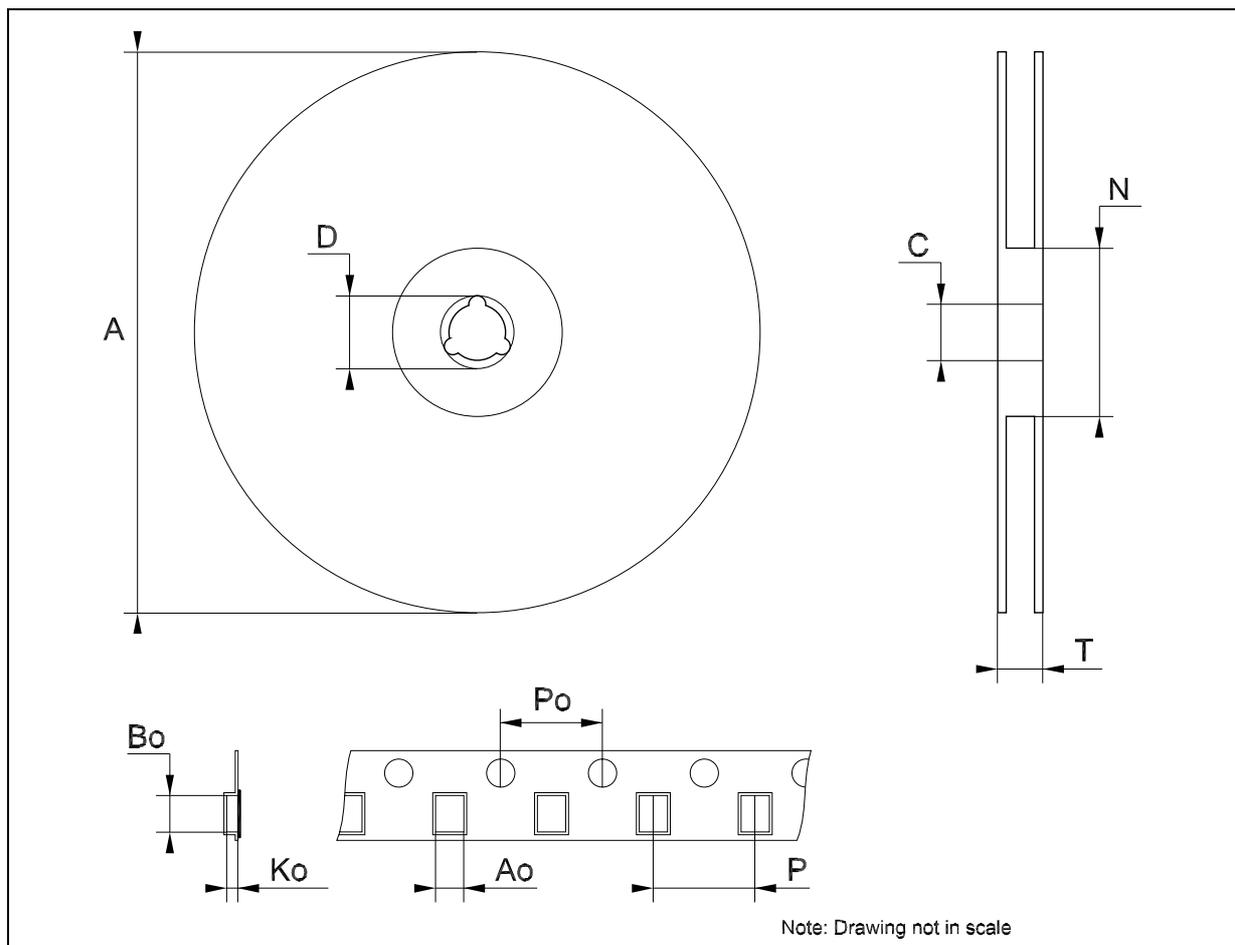
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



Tape & Reel SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics
All other names are the property of their respective owners

© 2004 STMicroelectronics - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>

