SPT7868

10-BIT, 80 MSPS A/D CONVERTER

PRELIMINARY INFORMATION

FEATURES

- 80 MSPS maximum sample rate
- 9.2 effective number of bits at f_{IN} = 15 MHz and f_S = 80 MSPS
- 2 V_{P-P} full-scale input range
- Differential input 2.5 V common mode
- Internal or external voltage reference
- Common-mode voltage reference output
- +3.3 V / +5 V digital output logic compatibility
- +5 V analog power supply

APPLICATIONS

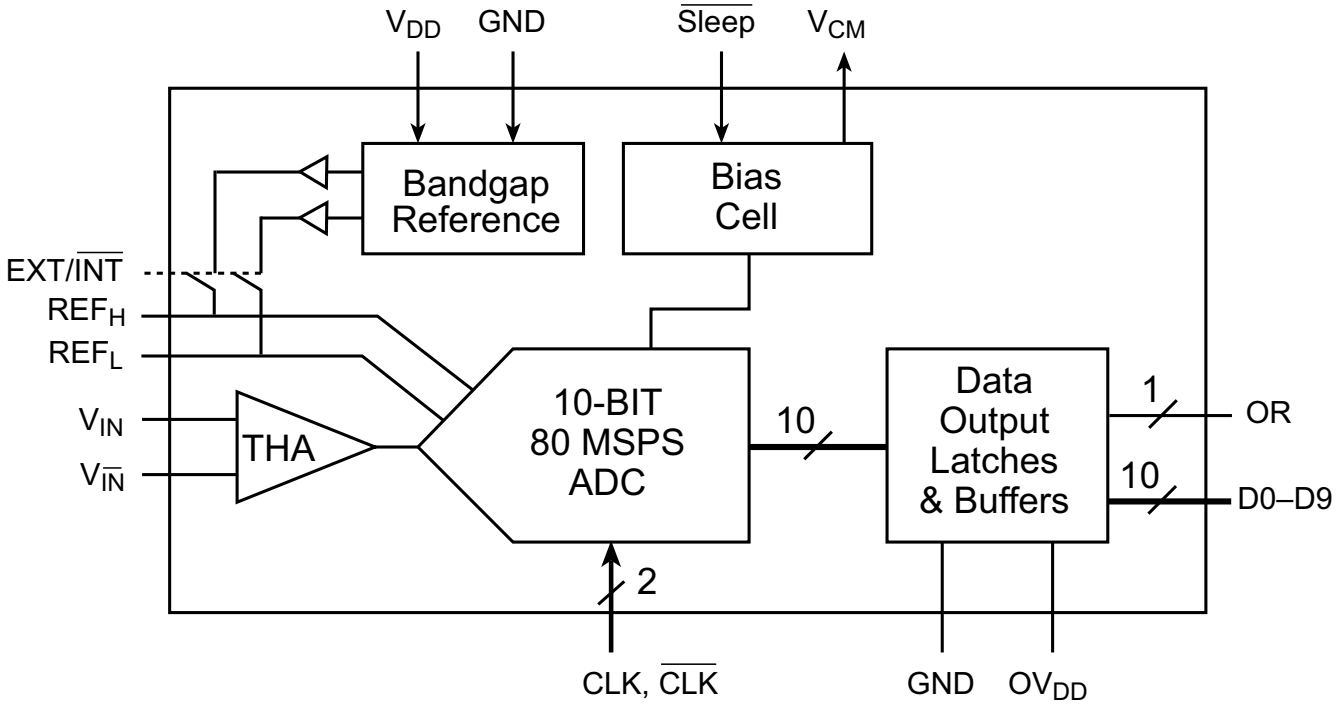
- High-speed applications where low power dissipation is required
- Video imaging
- Medical imaging
- Radar receivers
- IR imaging
- Digital communications

GENERAL DESCRIPTION

The SPT7868 is a 10-bit, 80 MSPS analog-to-digital converter with low power dissipation at only 627 mW typical at 80 MSPS with a power supply of +5.0 V. The digital outputs are +3 V or +5 V, and are user selectable. The SPT7868 has incorporated proprietary circuit design and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS compatible to interface with TTL/CMOS logic systems. Output data format is straight binary.

The SPT7868 is available in a 28-lead SSOP package over the industrial temperature range.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{DD} ..... TBD
OV_{DD} ..... TBD

Input Voltages

Analog Input ..... TBD
CLK Input ..... TBD

Output

Digital Outputs ..... TBD

Temperature

Operating Temperature ..... –40 to +85 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5.0 V, f_S=80 MSPS, V_{RHS}=3.0 V, V_{RLS}=2.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7868 MIN	SPT7868 TYP	SPT7868 MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Differential Linearity Error (DLE)	@ +25 °C	V		±0.5		LSB
	full temperature			±0.75		LSB
Integral Linearity Error (ILE)	@ +25 °C	V		±0.8		LSB
	full temperature			±1.0		LSB
No Missing Codes		VI		Guaranteed		
Analog Input						
Input Voltage Range (Differential)		V		±1		V
Input Common Mode		V		2.5		V
Input Capacitance		V		2		pF
Common Mode Rejection Ratio (CMRR)				TBD		
Timing Characteristics						
Conversion Rate		VI	80			MSPS
Pipeline Delay (Latency)		IV		7		clocks
Output Delay (t_D)		IV	TBD	TBD	TBD	ns
Aperture Delay Time		V		TBD		ns
Aperture Jitter Time		V		TBD		ps (rms)
Dynamic Performance						
Effective Number of Bits (ENOB)						
f_{IN} = 15 MHz, f_{CLK} = 80 MSPS	25 °C	I	9.0	9.2		Bits
	–40 °C to +85 °C	IV	8.8	9.0		Bits
Signal-to-Noise Ratio (SNR)						
f_{IN} = 15 MHz, f_{CLK} = 80 MSPS	25 °C	I	57	57		dB
	–40 °C to +85 °C	IV	TBD	TBD		dB
Total Harmonic Distortion (THD)						
f_{IN} = 15 MHz, f_{CLK} = 80 MSPS	25 °C	I		–69	–66	dB
	–40 °C to +85 °C	IV		TBD	TBD	dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN} = 15 MHz, f_{CLK} = 80 MSPS	25 °C	I	56	57		dB
	–40 °C to +85 °C	IV	TBD	TBD		dB
Spurious Free Dynamic Range (SFDR)						
f_{IN} = 15 MHz, f_{CLK} = 80 MSPS	25 °C	I	69	72		dB
	–40 °C to +85 °C	IV	TBD	TBD		dB

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5.0 V, f_S=80 MSPS, V_{RHS}=3.0 V, V_{RLS}=2.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7868 MIN	SPT7868 TYP	SPT7868 MAX	UNITS
Power Supply Requirements						
V_{DD} Voltage (Analog Supply)		IV	4.75	5.0	5.25	V
OV_{DD} Voltage (Output Supply)		IV	2.7	3.3/5.0	5.25	V
V_{DD} Current		VI		125	131	mA
OV_{DD} Current		VI		14	16	mA
Power Dissipation						
External Voltage Reference		VI		619	643	mW
Internal Voltage Reference		VI		627	651	mW
Sleep Mode Power Dissipation						
External Voltage Reference		VI		TBD	TBD	mW
Internal Voltage Reference		VI		TBD	TBD	mW
Power Supply Rejection Ratio (PSRR)		V		TBD		mV/V
Internal References						
Common Mode Voltage Reference (V_{CM})	IO = –1 µA	VI	TBD	2.5	TBD	V
Common Mode Voltage Tempco		V		100		ppm/°C
Output Impedance		V		TBD		kΩ
Current Capability		VI		TBD		µA
Reference Low Output Voltage (V_{REFL})	(EXT/$\overline{INT}$) = 0	VI	1.95	2.0	2.05	V
Reference High Output Voltage (V_{REFH})	(EXT/INT) = 0	VI	2.95	3.0	3.05	V
External References						
Reference Low Input Voltage Range	(EXT/$\overline{INT}$) = 1	IV	1.7	2.0	2.3	V
Reference High Input Voltage Range	(EXT/INT) = 1	IV	2.7	3.0	3.3	V
Digital Outputs						
Output Voltage High	IO = –2 mA	VI	85% OV_{DD}	90% OV_{DD}	OV_{DD}	V
Output Voltage Low	IO = 2 mA	VI		0.2	0.4	V
Digital Inputs						
Input High Voltage		VI	80% V_{DD}			V
Input Low Voltage		VI			20% V_{DD}	V
Input High Current		VI			±10	µA
Input Low Current		VI			±10	µA
Clock Inputs						
Clock Inputs High Voltage		VI	2		5	V
Clock Inputs Low Voltage		VI			0.4	V

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 – Driving Differential Inputs with a Differential Configuration

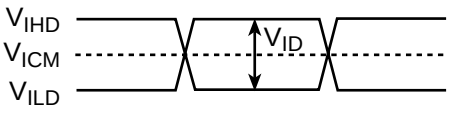
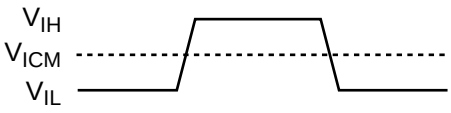
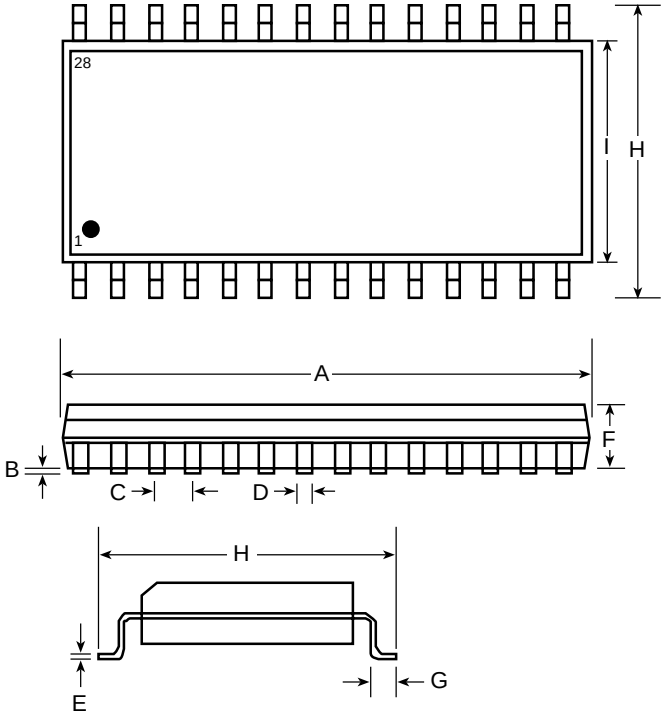


Figure 2 – Driving Differential Inputs with a Single-Ended Configuration



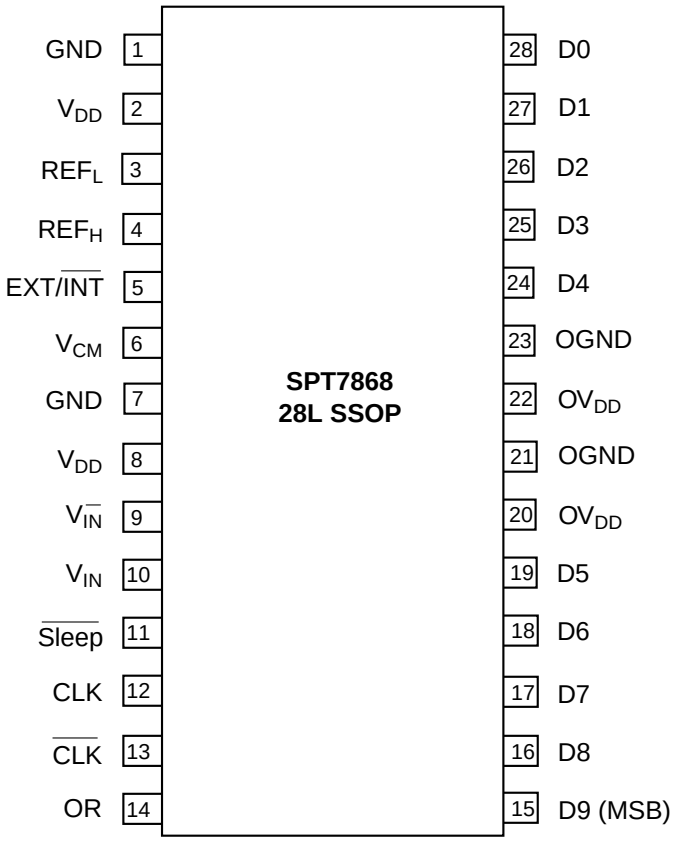
PACKAGE OUTLINE

28-Lead SSOP



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.397	0.407	10.07	10.33
B	0.002	0.008	0.05	0.21
C		0.0256 typ		0.65 typ
D	0.010	0.015	0.25	0.38
E	0.004	0.008	0.09	0.20
F	0.066	0.070	1.68	1.78
G	0.025	0.037	0.63	0.95
H	0.301	0.311	7.65	7.90
I	0.205	0.212	5.20	5.38

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
GND	Analog ground
V_{DD}	Analog +5 V
OGND	Output ground
OV_{DD}	Supply voltage for digital outputs +5 V or +3.3 V
REF_L	Reference pin low, input for external reference, bypass with capacitor (100 nF) when internal reference is selected.
REF_H	Reference pin high, input for external reference, bypass with capacitor (100 nF) when internal voltage is selected.
V_{CM}	2.5 V common mode voltage reference output
V_{IN}	Non-inverted analog input
$V_{\overline{IN}}$	Inverted analog input
CLK	Clock input pin
$\overline{CLK}$	Complement of clock input pin, internally biased to 1.5 V; if single-ended clock is used, bypass to GND with 100 nF
D0–D9	Digital outputs; D0 = LSB; 3.3 V/5 V compatible
OR	Overrange bit; 3.3 V/5 V compatible
EXT/$\overline{INT}$	EXT/$\overline{INT}$ = 1, external reference used; internal reference powered down EXT/$\overline{INT}$ = 0, internal reference used; internally pulled down
$\overline{Sleep}$	$\overline{Sleep}$ = 1, normal operation; internally pulled up $\overline{Sleep}$ = 0, powered-down mode

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7868SIR	–40 to +85 °C	28L SSOP