

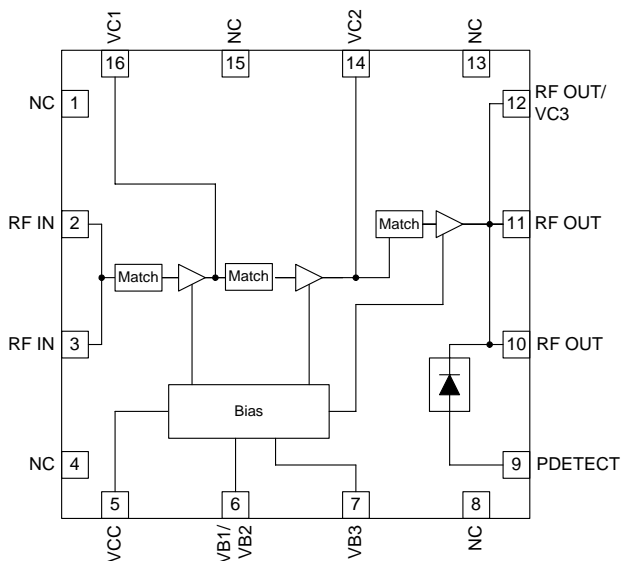


Features

- Single Power Supply 3.0V to 3.6V
- 34 dB Typical Small Signal Gain
- 50Ω Input and Interstage Matching
- 2400MHz to 2500MHz Frequency Range
- +18dBm, 2.5% EVM (typ.), 130mA@V_{CC}=3.3V

Applications

- IEEE802.11b/g/n WLAN Applications
- 2.5GHz ISM Band Applications
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- Spread-Spectrum and MMDS Systems



Functional Block Diagram

Product Description

The RF5152 is a linear, medium-power, high-efficiency, three-stage amplifier IC designed specifically for battery-powered WLAN applications such as PC cards, mini PCI, and compact flash applications. The device is manufactured on an advanced InGaP Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.5GHz OFDM and other spread-spectrum transmitters. The device is provided in a 3mmx3mm, 16-pin, QFN with a backside ground. The RF5152 is designed to maintain linearity over a wide range of supply voltages and power outputs.

Ordering Information

RF5152 3V to 3.6V, 2.4GHz to 2.5GHz Linear Power Amplifier
 RF5152PCBA-41X Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

- | | | | |
|---|--------------------------------------|-------------------------------------|-----------------------------------|
| <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input type="checkbox"/> Si CMOS | |
| <input checked="" type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | |

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V
Power Control Voltage (V_{REG})	-0.5 to +3.5	V_{DC}
DC Supply Current	600	mA
Input RF Power	+5	dBm
Operating Ambient Temperature	-10 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	JEDEC Level 2	



Caution! ESD sensitive device.

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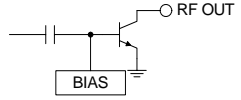
RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Temperature = +25°C, V_{CC} = 3.3V, V_{REG} = 2.8V, Frequency = 2450MHz, pulsed at 1% to 100% duty cycle, circuit per evaluation board schematic
Frequency	2.40		2.50	GHz	IEEE802.11g IEEE802.11n
Output Power		18			IEEE802.11g modulation, 54 Mbit/s, 64QAM, OFDM modulation
EVM*		2.5	3.3	%	RMS, mean
IP3		33		dBm	
Gain	32	34	37	dB	-11dBm Pin
Gain Variance			1.5	±dB	-15°C to +85°C
Input Impedance	49	50	51	Ω	Internally Matched Input and Interstage
Output VSWR			10:1		The PA is stable, no spurs above -43dBm
Power Detector (P_{detect})					
P_{OUT} = 8dBm		0.2	0.3	V_{DC}	
P_{OUT} = 18dBm	0.7	0.9	1.1	V_{DC}	
Power Supply					
Operating Voltage	3.0	3.3	3.6	V	
V_{REG} (Bias) Voltage (V_{B1}/V_{B2} , V_{B3})	2.7	2.8	3.0	V_{DC}	
Current Consumption	85	130	170	mA	RF P_{OUT} = +18dBm, V_{CC} = 3.3V, 54Mbps OFDM <2.5% EVM
Quiescent Current	45	75	105	mA	V_{CC} = +3.3V V_{DC} ; RF In = OFF; V_{REG} OFF
V_{REG} (Bias) Current (Total)	1	2	6	mA	V_{CC} = 3.3V
Input Return Loss		-15	-10	dB	
Turn-on Time**	300	700	1000	nS	Output stable to within 90% of final gain

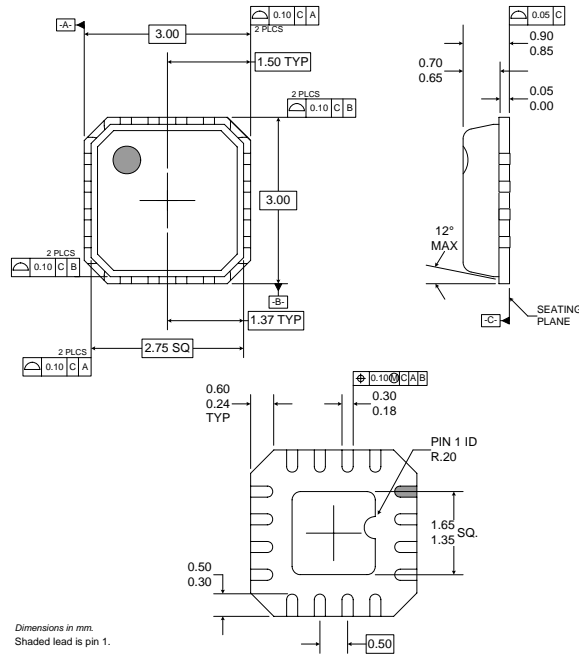
Notes:

*The EVM specification is obtained with a signal generator that has an EVM floor of less than 0.7%.

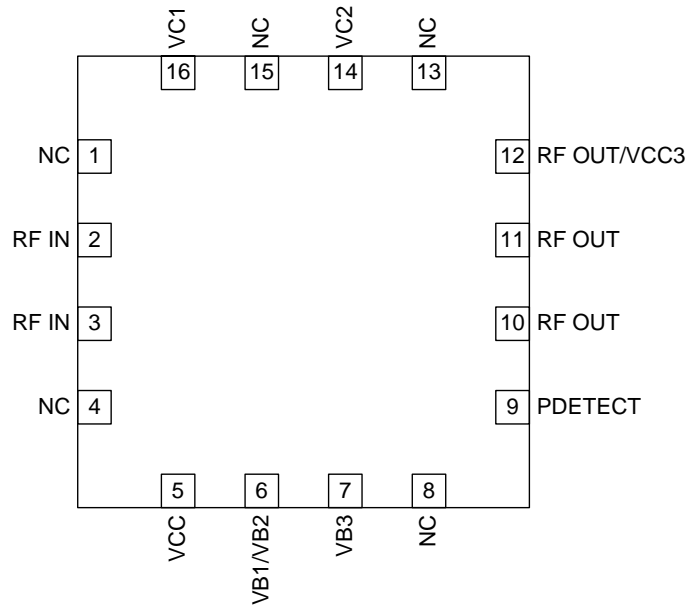
**The PA must operate with gated bias voltage input at 1% to 99% duty cycles without any EVM or other parameter degradation.

Pin	Function	Description	Interface Schematic
1	NC	Not connected. May be connected to ground (GND).	
2	RF IN	RF input. See evaluation board schematic for details.	
3	RF IN	RF input. See evaluation board schematic for details.	
4	NC	Not connected. Note: Connection of VC1 at this pin will not damage the RF5152 or adversely affect RF5152 performance.	
5	VCC	Supply voltage for the bias reference and control circuits. May be connected with VC1, VC2 and VC3 with a single-supply voltage as long as V_{CC} does not exceed $3.3V_{DC}$ in this configuration.	
6	VB1/VB2	Bias current control voltage for the first and second stages.	
7	VB3	Bias current control voltage for the third stage.	
8	NC	Not connected.	
9	PDETECT	Provides an output voltage proportional to the output RF level.	
10	RF OUT	RF output. The output requires external matching components which consist of a one or two shunt capacitors and a series capacitor for DC blocking.	
11	RF OUT	Same as pin 10.	See pin 10.
12	RF OUT/ VC3	RF output and bias for the output stage. The power supply for the output transistor needs to be supplied to this pin. This can be done through a quarter-wave ($\lambda_o/4$) length microstrip line that is RF grounded at the other end, or through an RF inductor that supports the required DC current. See evaluation board schematic.	See pin 10.
13	NC	Not connected. May be connected to ground (GND).	
14	VC2	Second stage power supply input. Connect as shown on evaluation board schematic.	
15	NC	Not connected. May be connected to ground (GND).	
16	VC1	First stage power supply input. Connect as shown on evaluation board schematic.	
Pkg Base	GND	Ground connection. The back side of the package should be connected to the ground plane through as short a connection as possible (e.g., PCB vias under the device are required).	

Package Drawing



Pin Out



Theory of Operation and Application Information

The RF5152 is a three-stage power amplifier (PA) with a minimum gain of 32dB (34dB typical) in the 2.4GHz to 2.5GHz Industrial, Scientific, and Medical (ISM) band. The RF5152 has a 50Ω internal input and interstage match. Only the RF5152 output stage requires matching. The RF5152 is designed primarily for IEEE802.11g/n wireless local area network (WLAN) applications where the available supply voltage and current are limited. This amplifier will operate to and below the lowest expected voltage made available by a typical PC Card (PCMCIA or CardBus) slot in a laptop personal computer (PC). The RF5152 maintains required linearity at decreased supply voltages.

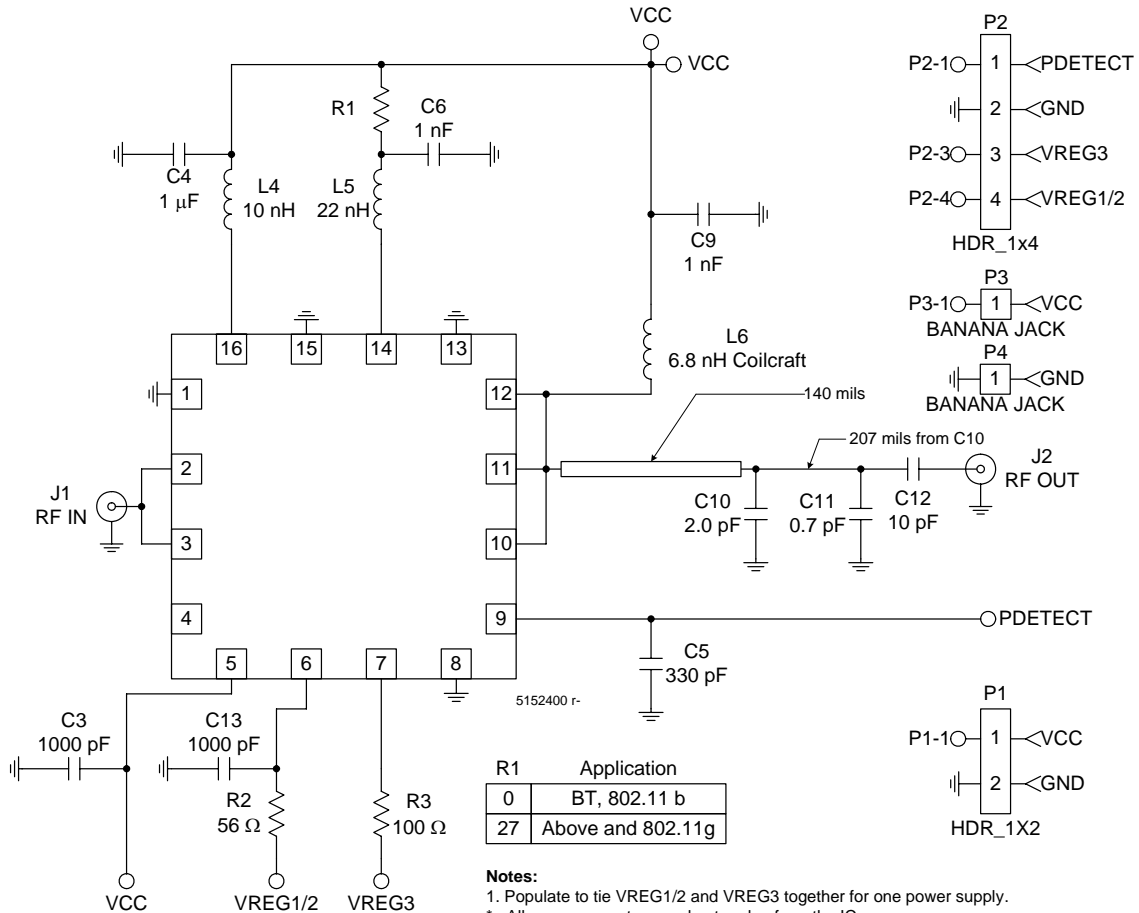
The RF5152 operates from a single supply voltage of 3.0V_{DC} to 3.6V_{DC} to deliver specified performance. Power control is provided through two (2) bias control input pins (VB1/VB2 and VB3). In most applications these two (2) bias control input pins are connected together and employed as a single control input. The RF5152 has been primarily characterized with a VB voltage of 2.8V_{DC}. However, the RF5152 will operate from a wide range of bias control voltages and within a wide range of frequencies (typically 1800MHz to 2800MHz). If a bias control voltage other than 2.8V_{DC} is preferred or if a different frequency range (other than 2.4GHz to 2.5GHz) is desired, please contact RFMD Sales or Applications Engineering for assistance.

Though not difficult to implement to achieve state-of-the-art performance, the RF5152 is employed at frequencies greater than 2GHz, where care in circuit layout and component selection is advisable. Of primary concern with RF5152 PCB layout is the selection and placement of output matching components (RF5152PCBA bill of materials (BOM) is available upon request). High-Q (quality factor) capacitors and inductors are not required in every RF5152 based design; however, it is highly recommended that the RF5152PCBA evaluation board BOM be followed exactly for all initial end product designs. Upon initial baseline of RF5152 based PCB performance, less costly (Lower-Q) output matching circuit components may be substituted and evaluated against the initial design performance. RFMD experience indicates that end product FTY improvements more than offset the cost difference between “High-Q” and “Low-Q” components.

There is no required matching on the RF5152 input or interstage circuits. Only the RF5152 output stage requires matching allowing the RF5152 to be implemented in applications requiring the fewest end product bill of materials (BOM) parts count and lowest BOM cost. The input stage requires a DC-blocking capacitor. In most cases the capacitor used as part of the RF5152 output matching circuit is also employed to accomplish DC-blocking. The RF5152PCBA evaluation board (available from RF Micro Devices, Inc. (RFMD)) is optimized for 3.3V_{DC} supply input. The output matching capacitor is C10 which is located approximately 120mils from the IC (as shown on the *RF5152PCBA Evaluation Board Schematic*). The capacitor C10 is selected in value and positioned with reference to 50Ω transmission line segment TL1. Transmission line segment TL1 should be duplicated as closely as possible in specified length and thickness in any customer PCB layout. Due to PCB material variation (e.g., FR4) and PCB manufacturer variations, the customer may benefit from small adjustments made to the length of TL1 when the RF5152PCBA evaluation board is duplicated to produce an end product PCB design. The initial PCB layout should include exposed ground area near C10 to allow ease of RF5152 output circuit optimization. Smith Chart-based design tools may be used to assist in determining the desired capacitor value and transmission line physical characteristics. Note that the use of a single capacitor output circuit match will result in a more sensitive match and slightly reduced RF5152 bandwidth. In this configuration the RF5152 will exhibit sufficient output spectrum bandwidth to meet IEEE802.11b/g requirements when matched properly.

For best results, the RF5152PCBA evaluation board circuit layout should be copied as closely as possible. In particular, the RF5152PCBA evaluation board ground layout, ground vias, and output matching components and location should be copied without deviation. Other PCB layout configurations may provide acceptable RF5152 performance; however, the end product design process will be faster and manufacturing first time yield (FTY) better if the RF5152PCBA evaluation board design is followed. RFMD provides RF5152PCBA design and Gerber files upon request.

Evaluation Board Schematic - IEEE802.11b/g

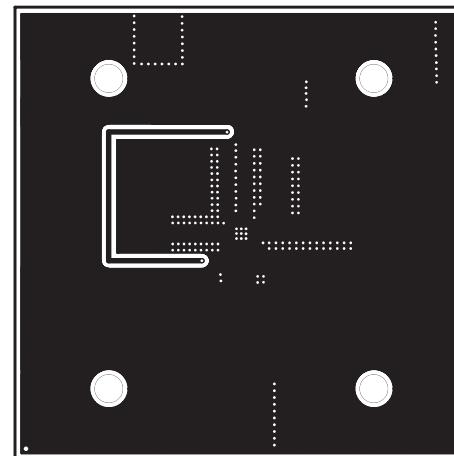
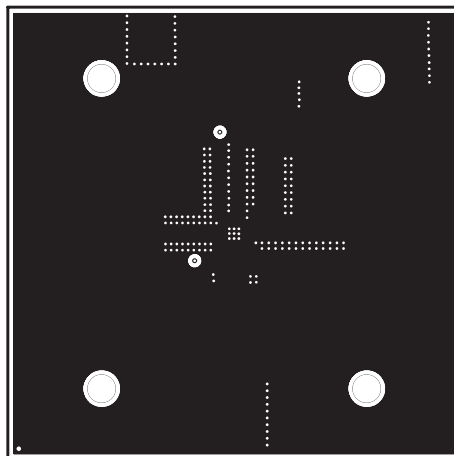
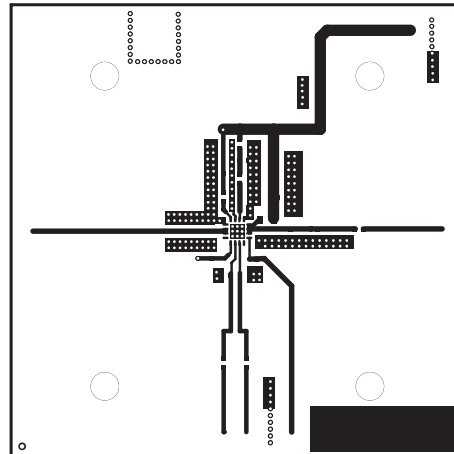
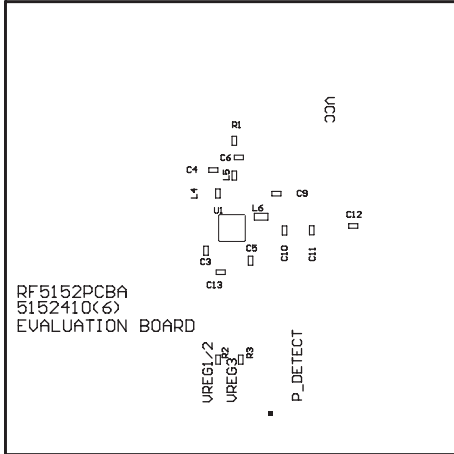


Notes:

- 1. Populate to tie VREG1/2 and VREG3 together for one power supply.
- * All measurements are edge to edge from the IC.
- Components labeled with a "*" may not be needed on the eval board.

Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.031", Board Material FR-4, Multi-Layer



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

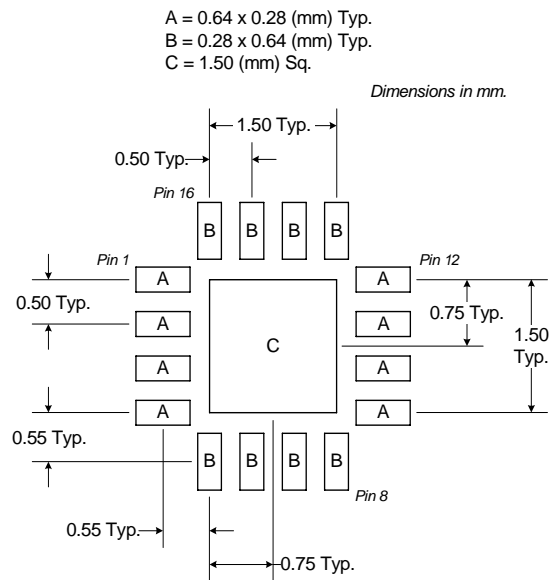


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

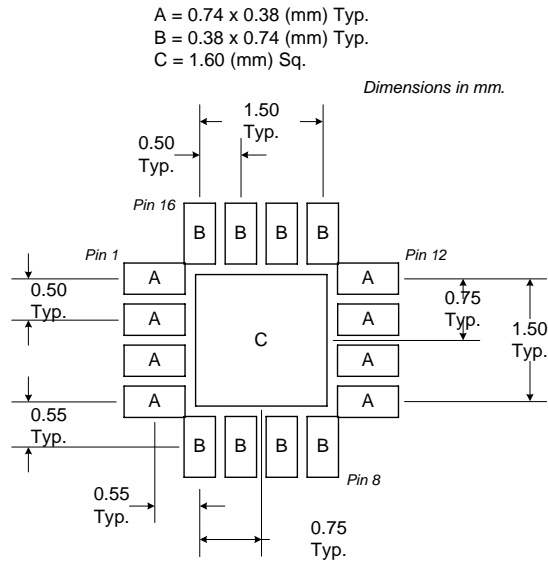


Figure 2. PCB Solder Mask Pattern (Top View)

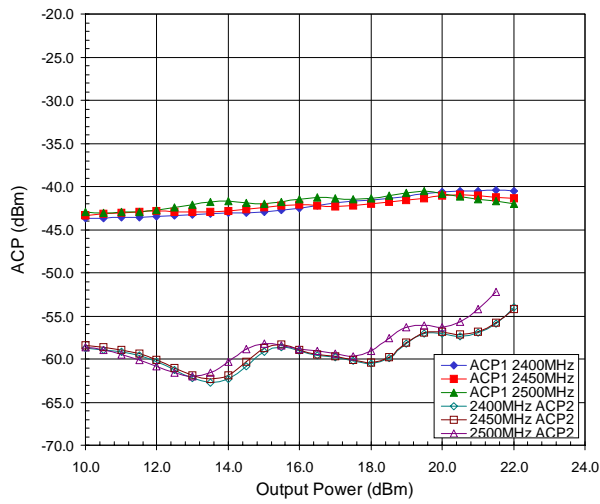
Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

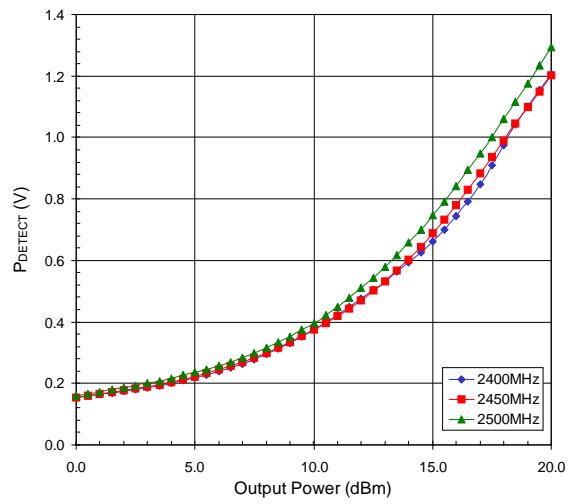
Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

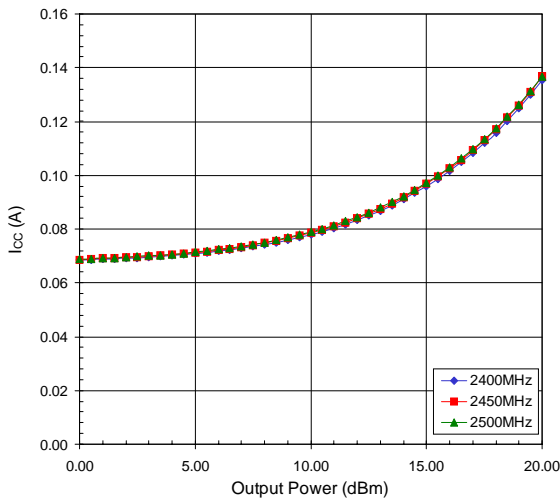
ACP versus P_{OUT}



P_{DETECT} versus P_{OUT}



Operating Current versus P_{OUT}



EVM versus P_{OUT}

