



# MICROCHIP

# PIC18F2525/2620/4525/4620

## PIC18F2525/2620/4525/4620 Data Sheet Errata

### Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39626B), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F2525/2620/4525/4620 devices will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

#### 1. Module: I/O Ports

The TRIS setting for the TX pin on PORTC in Table 10-5 of the Device Data Sheet was incorrectly stated as '1'.

The correct TRIS setting for the TX pin on PORTC is '0'.

#### 2. Module: Resets

The PR2 initialization condition shown in Table 4-4 for MCLR Resets, WDT Reset, RESET Instruction, Stack Resets and Wake-up via WDT or Interrupt should read "uuuu uuuu" as shown in the following table (changes are shown in **bold text**):

**TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS**

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
	2525	2620	4525	4620			
PR2					1111 1111	<b>uuuu uuuu</b>	<b>uuuu uuuu</b>

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

#### 3. Module: Voltage-Frequency Graph

The title information for Figure 26-2: Voltage-Frequency Graph (Extended), references the wrong device family and has been changed to read as follows:

**FIGURE 26-2: PIC18F2525/2620/4525/4620 VOLTAGE-FREQUENCY GRAPH (EXTENDED)**

# PIC18F2525/2620/4525/4620

## 4. Module: DC Characteristics

In Section 26.3 “DC Characteristics” (page 336), the specifications for  $V_{IL}$  parameters D033B and D034 have been clarified and now read as follows:

### 26.3 DC Characteristics: PIC18F2525/2620/4525/4620 (Industrial, Extended) PIC18LF2525/2620/4525/4620 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_a \leq +85^{\circ}\text{C}$ for industrial			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D033B D034	$V_{IL}$	<b>Input Low Voltage</b> OSC1 T13CKI	$V_{SS}$ $V_{SS}$	0.3 0.3	V V	XT, LP modes

## 5. Module: A/D Converter Characteristics

In Table 26-24: A/D Converter Characteristics (page 359), specification A40 has been added:

**TABLE 26-24: A/D CONVERTER CHARACTERISTICS: PIC18FX525/X620 (INDUSTRIAL, EXTENDED)  
PIC18LFX525/X620 (INDUSTRIAL)**

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A40	IAD	A/D Current from $V_{DD}$					
		PIC18FXXXX	—	180	—	$\mu\text{A}$	Average current during conversion
		PIC18LFX20	—	90	—	$\mu\text{A}$	

## 6. Module: Instruction Set

In Table 24-2: PIC18FXXXX Instruction Set (pages 270-271), the `ADDWF`, `ADDWFC` and `BTG` instructions have been modified. The changes are shown in **bold** text:

**TABLE 26-25: PIC18FXXXX INSTRUCTION SET**

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word				Status Affected	Notes	
			MSb		LSb				
<b>BYTE-ORIENTED OPERATIONS</b>									
ADDWF	f, d, a	Add WREG and f	1	0010	<b>01da</b>	ffff	ffff	C, DC, Z, OV, N	1, 2
ADDWFC	f, d, a	Add WREG and Carry bit to f	1	0010	<b>00da</b>	ffff	ffff	C, DC, Z, OV, N	1, 2
<b>BIT-ORIENTED OPERATIONS</b>									
BTG	f, b, a	Bit Toggle f	1	0111	bbba	ffff	ffff	None	1, 2

- Note 1:** When a Port register is modified as a function of itself (e.g., `MOVWF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- Note 2:** If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.

# PIC18F2525/2620/4525/4620

## 7. Module: Timing Diagrams and Specifications

Table 26-6: External Clock Timing Requirements (page 343), has been revised (changes and additions are shown in **bold** text).

**TABLE 26-6: EXTERNAL CLOCK TIMING REQUIREMENTS**

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	Fosc	External CLKI Frequency <sup>(1)</sup>	DC	1	MHz	XT, RC Oscillator mode
			<b>DC</b>	<b>25</b>	<b>MHz</b>	<b>HS Oscillator mode</b>
			DC	31.25	kHz	LP Oscillator mode
			<b>DC</b>	<b>40</b>	<b>MHz</b>	<b>EC Oscillator mode</b>
		Oscillator Frequency <sup>(1)</sup>	DC	4	MHz	RC Oscillator mode
			0.1	4	MHz	XT Oscillator mode
			<b>4</b>	<b>25</b>	<b>MHz</b>	<b>HS Oscillator mode</b>
			<b>4</b>	<b>10</b>	<b>MHz</b>	<b>HS + PLL Oscillator mode</b>
		5	200	kHz	LP Oscillator mode	
1	Tosc	External CLKI Period <sup>(1)</sup>	1000	—	ns	XT, RC Oscillator mode
			<b>40</b>	—	<b>ns</b>	<b>HS Oscillator mode</b>
			32	—	μs	LP Oscillator mode
			<b>25</b>	—	<b>ns</b>	<b>EC Oscillator mode</b>
		Oscillator Period <sup>(1)</sup>	250	—	ns	RC Oscillator mode
			250	1	μs	XT Oscillator mode
			<b>40</b>	<b>250</b>	<b>ns</b>	<b>HS Oscillator mode</b>
			<b>100</b>	<b>250</b>	<b>ns</b>	<b>HS + PLL Oscillator mode</b>
		5	200	μs	LP Oscillator mode	

**Note 1:** Instruction cycle period (T<sub>CY</sub>) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

## 8. Module: EUSART

The RX pin sampling information in **Section 18.1.2 “Sampling”** has changed. This section now reads as follows:

### 18.1.2 SAMPLING

The data on the RX pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin when SYNC is clear or when BRG16 and BRGH are both not set.

The data on the RX pin is sampled once when SYNC is set or when BRGH16 and BRGH are both set.

## 9. Module: MSSP

In **Section 17.3.2 “Operation”**, the following note has been added:

**Note:** The SSPBUF register cannot be used with read-modify-write instructions, such as BCF, BTFSC, COMF, etc.

## 10. Module: QFN

In the QFN pin diagram on page 3 and in Table 1-3: PIC18F4525/4620 Pinout I/O Descriptions, the following note has been added:

**Note:** It is recommended to connect the bottom pad of QFN package parts to V<sub>SS</sub>.

# PIC18F2525/2620/4525/4620

## 11. Module: Electrical Characteristics

Parameters D031A and D041A have been added to Section 26-3 “DC Characteristics”, as shown below:

### 26.3 DC Characteristics: PIC18F2525/2620/4525/4620 (Industrial) PIC18LF2525/2620/4525/4620 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D031A	V <sub>IL</sub>	<b>Input Low Voltage</b> I/O ports: with SMBus buffer	V <sub>SS</sub>	0.8	V	
D041A	V <sub>IH</sub>	<b>Input High Voltage</b> I/O ports: with SMBus buffer	2.1	V <sub>DD</sub>	V	

## 12. Module: Electrical Characteristics

In Table 26-1: Memory Programming Requirements, parameters D132, D132A, D133 and D133A have been changed. The changes are shown in **bold**:

**TABLE 26-1: MEMORY PROGRAMMING REQUIREMENTS**

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D132	V <sub>IE</sub>	<b>Program Flash Memory</b> V <sub>DD</sub> for Block Erase	<b>3.0</b>	—	5.5	V	Using ICSP™ port, <b>25°C</b>
D132A	V <sub>IW</sub>	V <sub>DD</sub> for Externally Timed Erase or Write	4.5	—	5.5	V	Using ICSP port, <b>25°C</b>
D133	T <sub>IE</sub>	ICSP Block Erase Cycle Time	—	4	—	ms	<b>V<sub>DD</sub> ≥ 4.5V</b>
D133A	T <sub>IW</sub>	ICSP Erase or Write Cycle Time (externally timed)	1	—	—	ms	<b>V<sub>DD</sub> ≥ 4.5V, 25°C</b>
<b>D133A</b>	<b>T<sub>IW</sub></b>	<b>Self-Timed Write Cycle Time</b>	—	<b>2</b>	—	<b>ms</b>	

## 13. Module: Pinout I/O Descriptions

The QFN column has been removed from Table 1-2: PIC18F2525/2620 Pinout I/O Descriptions.

The PIC18F2525/2620 devices are not available in a QFN package.

## REVISION HISTORY

### Rev A Document (01/2005)

First revision of this document.

Data Sheet Clarification issues 1 (I/O Ports), 2 (Resets), 3 (Voltage-Frequency Graph), 4 (DC Characteristics), 5 (A/D Converter Characteristics), 6 (Instruction Set) and 7 (Timing Diagrams and Specifications).

### Rev B Document (09/2005)

Added Data Sheet Clarification issues 8 (EUSART), 9 (MSSP), 10 (QFN), 11-12 (Electrical Characteristics) and 13 (Pinout I/O Descriptions).

# PIC18F2525/2620/4525/4620

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NOTES:

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