LVDS Dual 2x2 Crosspoint/Repeater Switch

Features

- Dual 2x2 Crosspoint/Repeater Switch
- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995
- Designed for Signaling Rates up to 650 Mbit/s (325Mhz)
- Operates from a single 3.3V Supply: –40°C to 85°C
- Low-Voltage Differential Signaling with Output Voltages of ±350mV into:
  - 100Ω load (PI90LV044)
  - 50Ω load Bus LVDS Signaling (PI90LVB044)
- Accepts ±350mV differential inputs
- Wide common mode input range: 0.2V to 2.7V
- Output drivers are high impedance when disabled or when $V_{CC} \leq 1.5V$
- Inputs are open, short, and terminated fail safe
- Propagation Delay Time: 3.5ns
- ESD protection is 10kV on bus pins
- Bus Pins are High Impedance when disabled or with V_{CC} less than 1.5V
- TTL Inputs are 5V Tolerant
- Power Dissipation at 400 Mbit/s of 250mW
- Packaging (Pb-free & Green available):
  - 28-pin QSOP (Q)
  - 28-pin TSSOP (L)

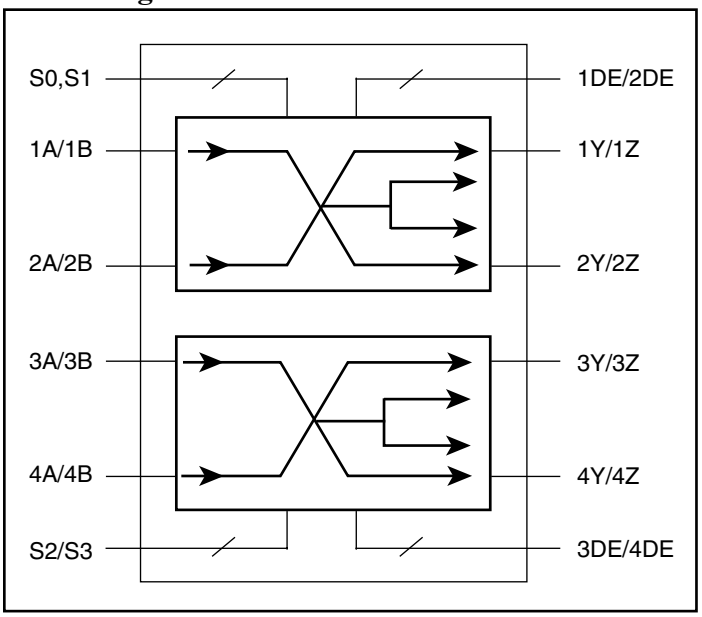
Description

The PI90LV044 and PI90LVB044 are monolithic dual 2x2 asynchronous crosspoint/repeater switches. The crosspoint function is based on a multiplexer tree architecture. Each 2x2 switch can be considered as a pair of 2:1 multiplexers that share the same inputs. The signal path through each switch is fully differential with minimal propagation delay. The signal path is unregistered, so no clock is required for the data inputs. The signal line drivers and receivers use Low Voltage Differential Signaling (LVDS) to achieve signaling rates as high as 650Mbps.

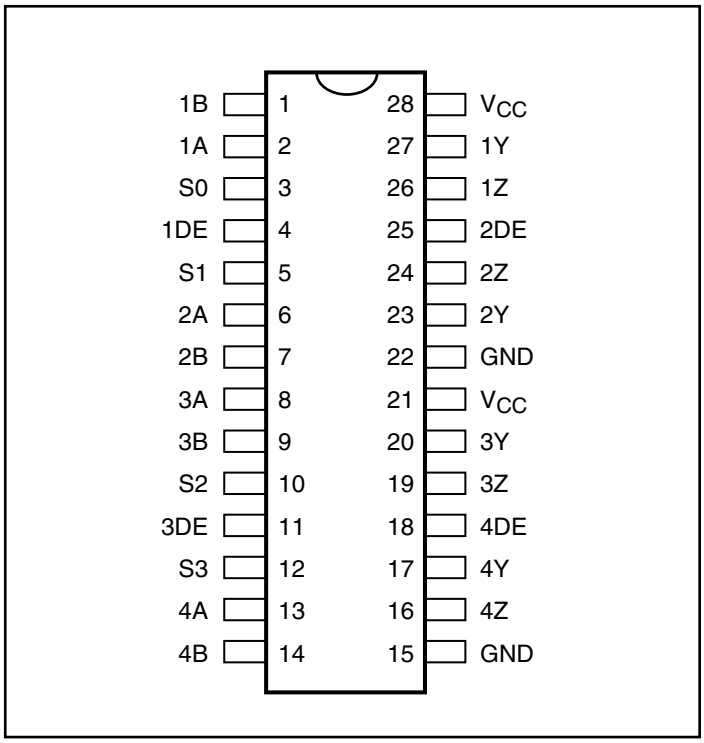
The LVDS standard provides a minimum differential output voltage magnitude of 247 mV into a 100Ω load and receipt of 100 mV signals with up to 1V of ground potential difference between a transmitter and receiver. The PI90LVB044 doubles the output drive current to achieve LVDS levels with a 50 ohm load.

The intended application of these devices is for loop-through and redundant channel switching for both point-to-point baseband (PI90LV044) and multipoint (PI90LVB044) data transmissions over controlled impedance media.

Block Diagram



Pin Configuration



MUX Truth Table

Input		Output		Function
S3, S1	S2, S0	1Y/1Z - 3Y/3Z	2T/2Z - 4Y/4Z	
0	0	1A/1B - 3A/3B	1A/1B - 3A/3B	Splitter
0	1	2A/2B - 4A/4B	2A/2B - 4A/4B	Splitter
1	0	1A/1B - 3A/3B	1A/1B - 3A/3B	Router
1	1	2A/2B - 4A/4B	2A/2B - 4A/4B	Router

Note:
1. Setting *n*DE to 0 will set Ouput *n*Y/*n*Z to High Impedance.

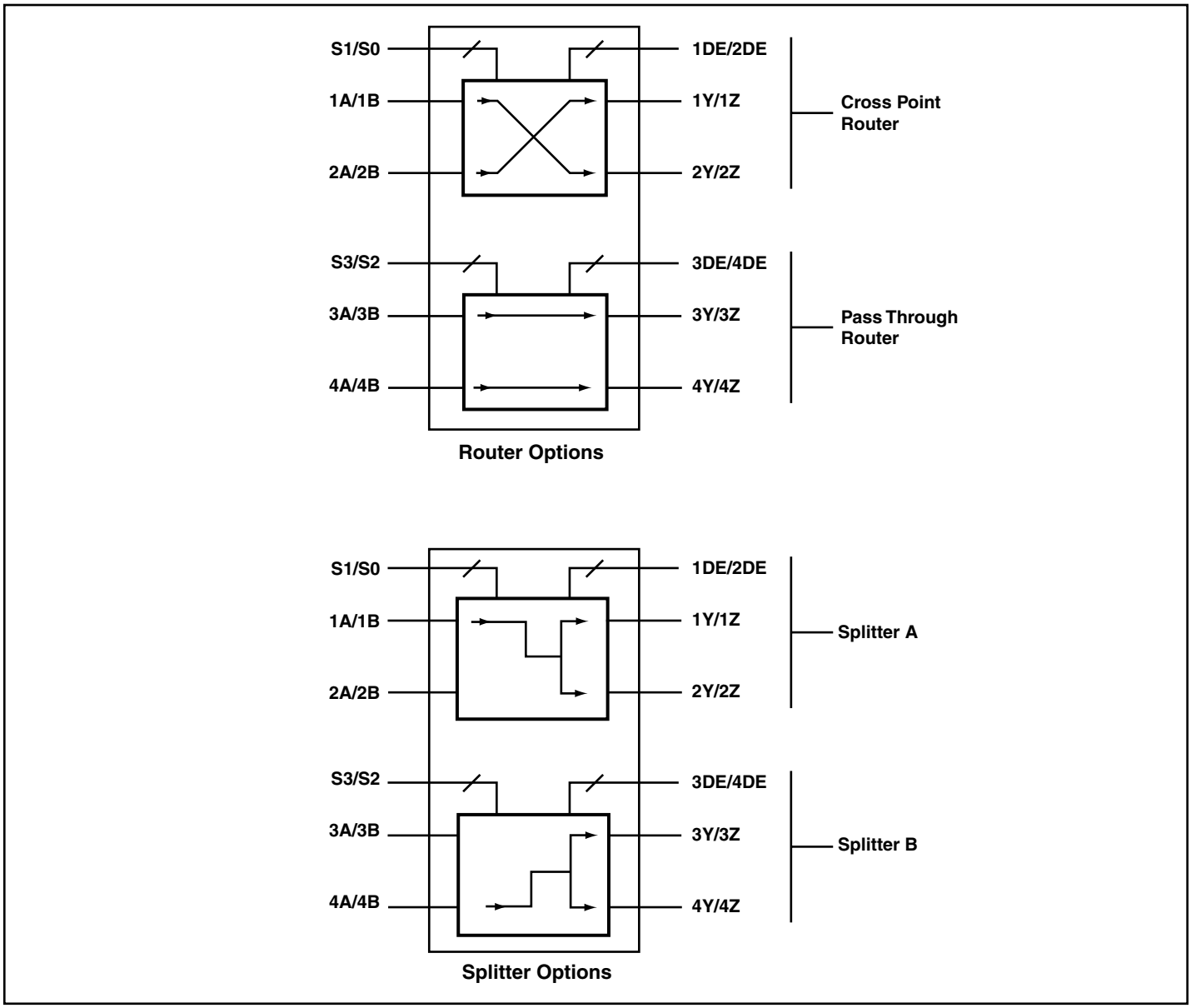


Figure 1. Possible Signal Routing

Absolute Maximum Ratings Over Operating Free-Air Temperature(1)

Supply Voltage Range, V_{CC}(1)	–0.5V to 4V
Voltage Range (DE, S0, S1)	–0.5 to 6V
Input Voltage Range, V_I (A or B)	–0.5V to V_{CC} + 0.5V
Electrostatic Discharge: A, B, Y, Z, and GND(2)	Class 3, A: 16kV, B:600V
All Pins	Class 3, A: 7kV, B:500V
Storage Temperature Range	–65°C to 150°C
Lead Temperature 1, 6 mm (1/16 inch) from case for 10 seconds	260°C

Notes:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.
2. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
3. Tested in accordance with MIL-STD-883C Method 3015.7

Recommended Operating Conditions

		Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}		3.0	3.3	3.6	V
High-Level input voltage, V_{IH}	S1 - S3, 1DE - 4DE	2			
Low-Level input voltage, V_{IL}				0.8	
Magnitude of Differential Input Voltage $\lvert V_{ID} \rvert$		0.1		0.6	
Common Mode input voltage, V_{IC} (see figure 2)		$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	
				V_{CC} - 0.8	
Operating free-air Temperature, T_A		-40		85	ºC

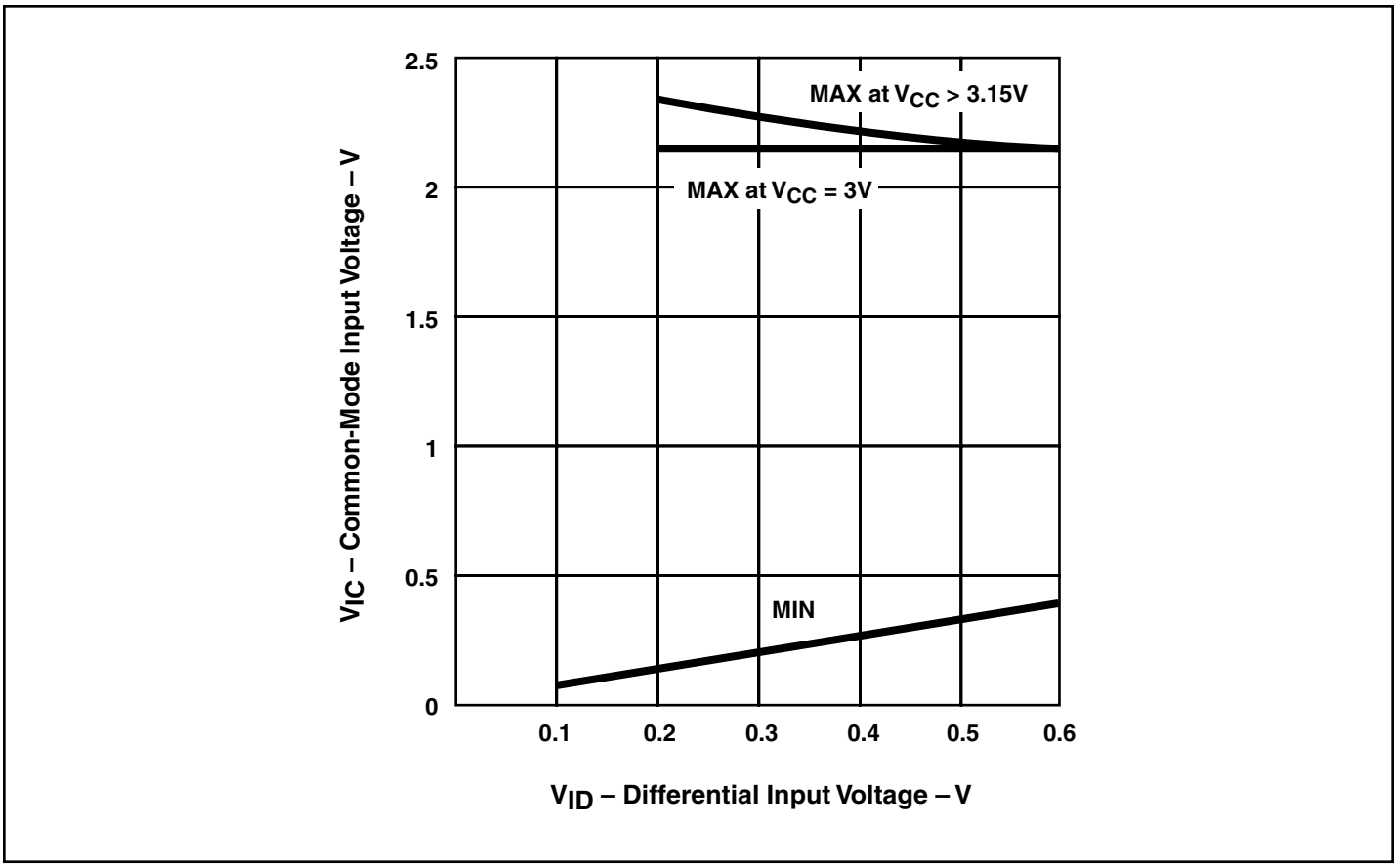


Figure 2. Common-Mode Input Voltage vs. Differential Voltage

Receiver Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{ITH+}	Positive going differential input voltage threshold	VCM = 1.2V			100	mV
V_{ITH-}	Negative going differential input voltage threshold		-100			
I_I	Input current (A or B inputs)	VI = 0V	-2		-20	µA
		VI = 2.4V	-1.2			
$I_{I\ (OFF)}$	Power-off input current (A or B inputs)	VCC = 0V			20	

Receiver/Driver Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Test Condition	Min.	Typ.(1)	Max.	Units
V_{OD}	Differential Output voltage magnitude		R_L = 100Ω (LV) R_L = 50Ω (LVB)	247	440	590	mV
ΔV_{OD}	Change in differential Output voltage magnitude between logic states			-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage			1.062		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			-50	3	50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage					150	
I_{CC}	Supply Current		No load		16	24	mA
			R_L = 100Ω (LV)		26	40	
			R_L = 50Ω (LVB)		42	54	
			All Channels Disabled		6	12	
I_{IH}	High level input current	DE	V_{IH} = 5			40	nA
		S1, S2, S3, S4				-3	µA
I_{IL}	Low level input current	DE	V_{IL} = 0.8V			-20	nA
		S1, S2, S3, S4				10	µA
I_{OS}	Short circuit output current		V_{OY} or V_{OZ} = 0V, V_{OD} = 0V			-10	mA
I_{OZ}	High impedence output current		V_{OD} = 600mV		1.5	±25	nA
			V_O - 0V or V_{CC}		1.5	±25	
$I_{O(OFF)}$	Power off output current		V_{CC} = 0V, V_O = 3.6V		1.5	±40	
C_{IN}	Input Capacitance		S0 - S3, 1DE - 4DE		3		pF
					8		

Note:
1. All typical values are at 25°C and with a 3.3 supply

Differential Receiver to Driver Switching Characteristics Over Recommended Operating Conditions

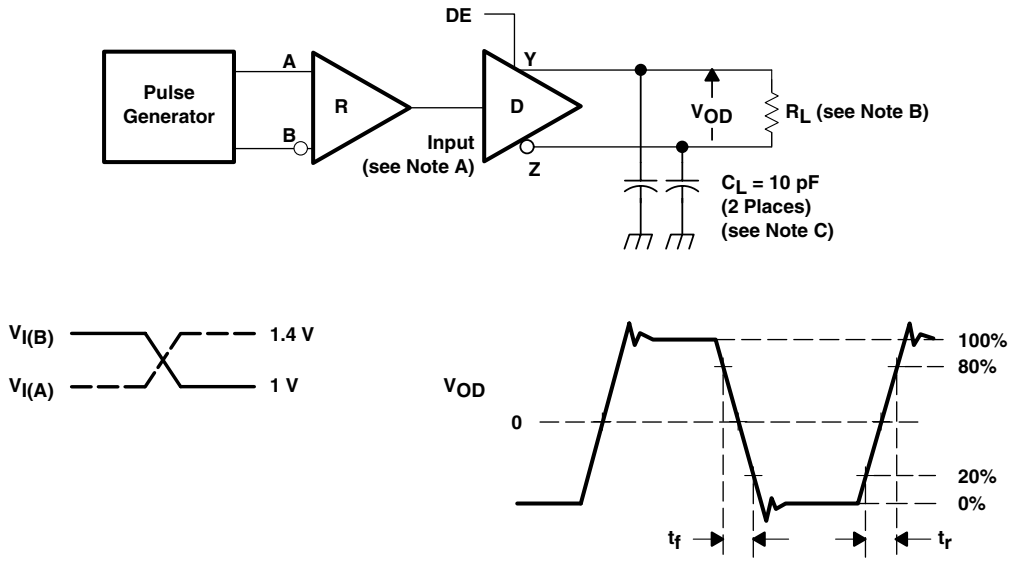
(unless otherwise noted)

Symbol	Parameter		Test Condition	Min.	Typ.(1)	Max.	Units
t_{PLH}	Differential propagation delay, low-to-high		C_L = 10pF		4.0	6.0	ns
t_{PHL}	Differential propagation delay, high-to-low				4.0	6.0	
$t_{sk(p)}$	Pulse skew (| $t_{PHL} - t_{PLH}$ |)				0.25	0.3	
t_r	Transition, low-to-high	LV044			1.0	1.5	
		LVB044			0.8	1.3	
t_f	Transition, high-to-low	LV044			1.0	1.5	
		LVB044			0.8	1.3	
t_{PHZ}	Propagation delay time, high-level-to-high-impedence output				4.0	10	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				4.3	10	
t_{PZH}	Propagation delay time, high-impedence to high-level output				3.0	10	
t_{PZL}	Propagation delay time, high-impdeence tolow-level output				2.0	10	
t_{PHL}_R1_Dx	Channel-tochannel skew, receiver to driver(2)				-	95	ps
t_{PLH}_R1_Dx					-	95	
t_{PHL}_R2_Dx					-	95	
t_{PLH}_R2_Dx					-	95	

Notes:

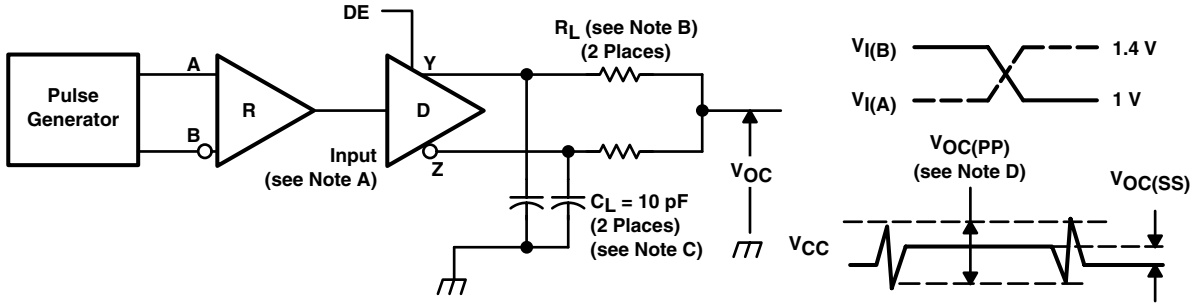
1. All typical values are at 25°C and with a 3.3 supply
2. These parametric values are measured over supply voltage and temperature ranges recommended for the device

Parameter Measurement Information



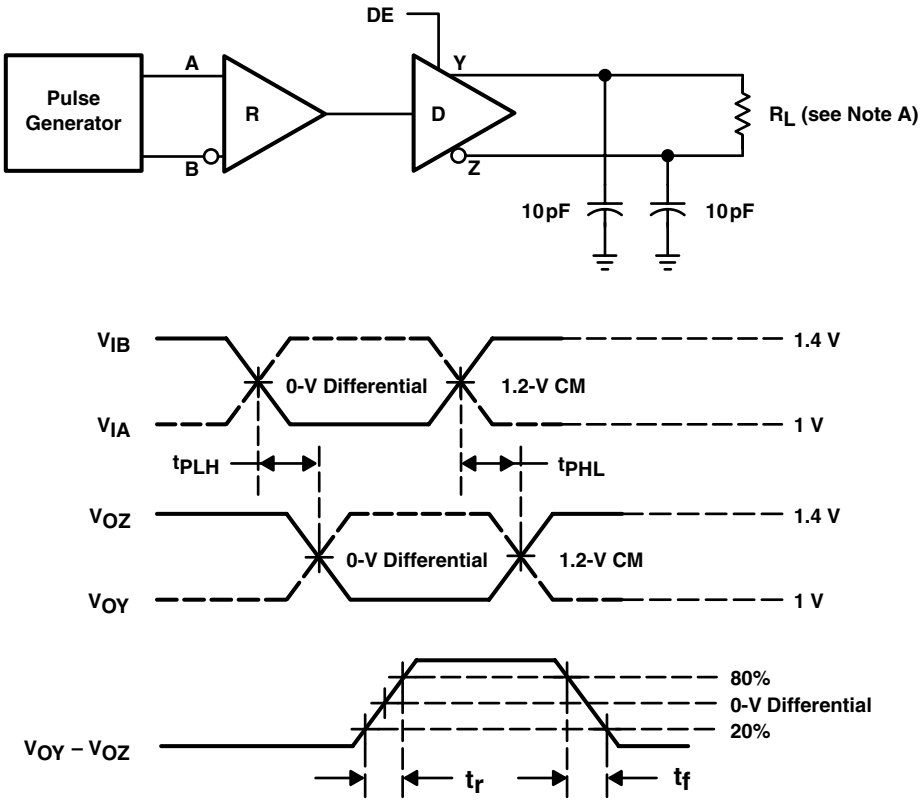
Notes: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, pulse repetition rate (PRR) - 50 Mpps, pulse width = 10 ±0.2ns.
B. R_L = 100Ω or 50Ω ±1%.
C. C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.
D. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Voltage Definitions for the Differential Output Signal



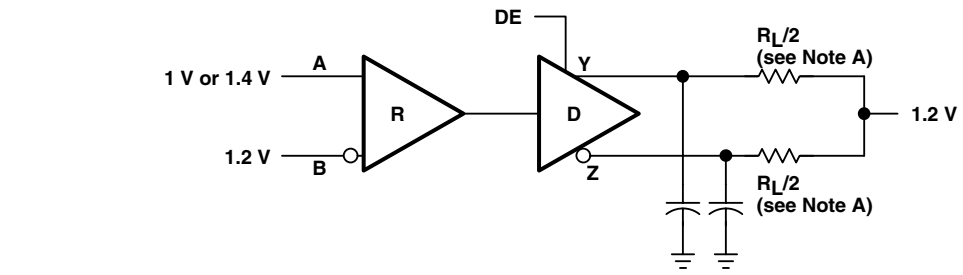
Notes: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, pulse repetition rate (PRR) - 50 Mpps, pulse width = 10 ±0.2ns.
B. R_L = 100Ω or 50Ω ±1%.
C. C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.
D. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3dB bandwidth of at least 300 MHz.

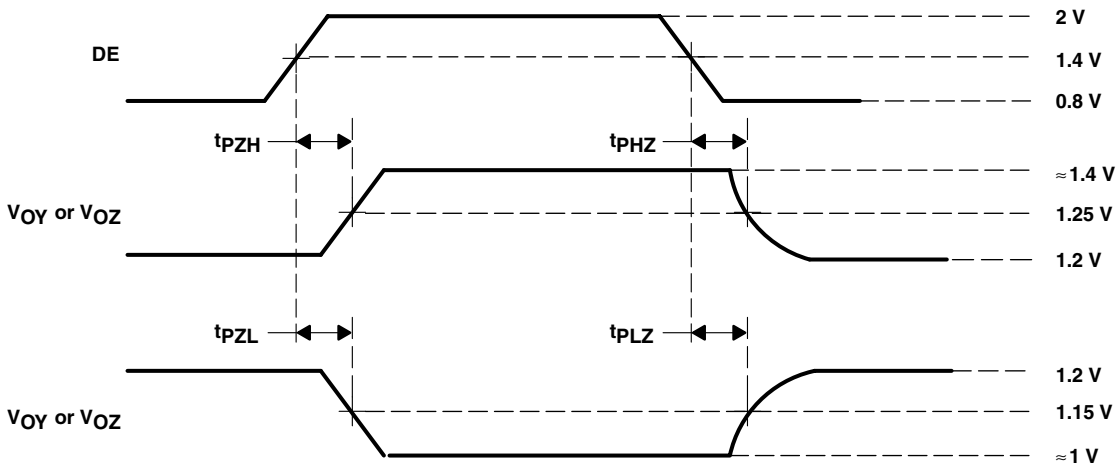
Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Notes: A. R_L = 100Ω or 50Ω ±1%
B. All input pulses are supplies by a generator having the following characteristics: pulse repetition rate (PPR) = 50 Mpps, pulse width = 10 ±0.2ns.

Figure 5. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms





Notes: A. R_L = 100Ω or 50Ω ±1%
B. All input pulses are supplied by a generator having the following characteristics: pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10ns.

Figure 6. Enable and Disable Timing Circuit

Typical Characteristics

PI90LV044
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

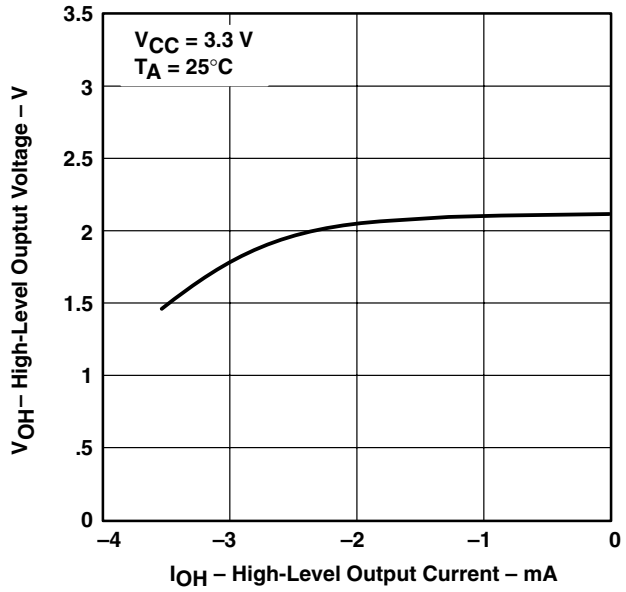


Figure 7

PI90LV044
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

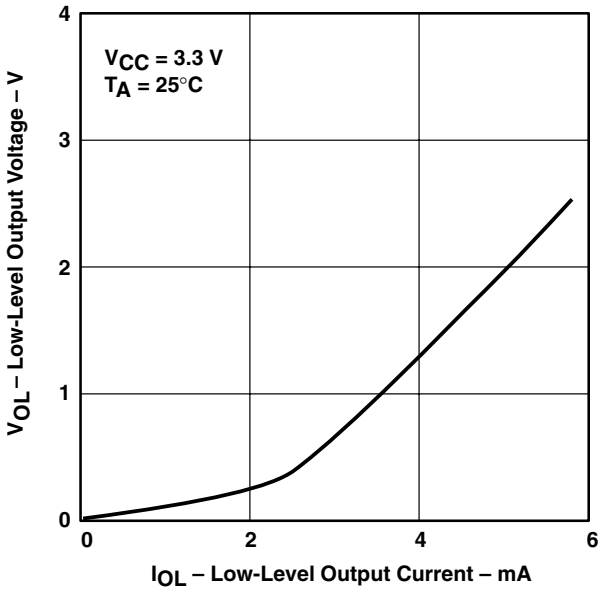


Figure 8

PI90LVB044
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

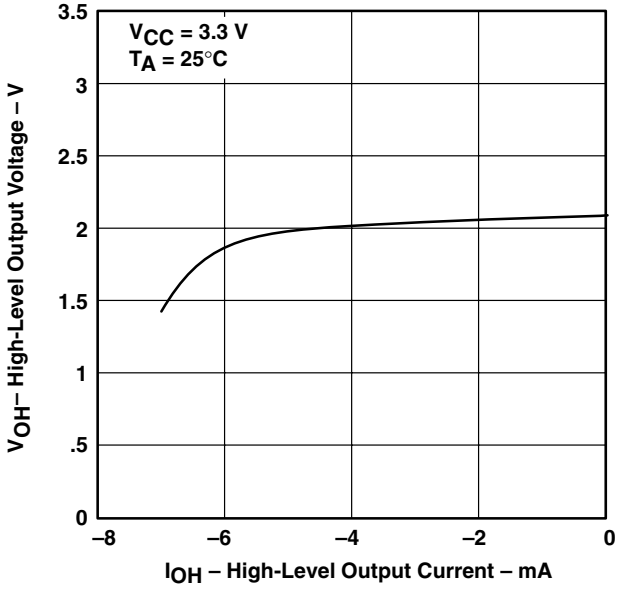


Figure 9

PI90LVB044
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

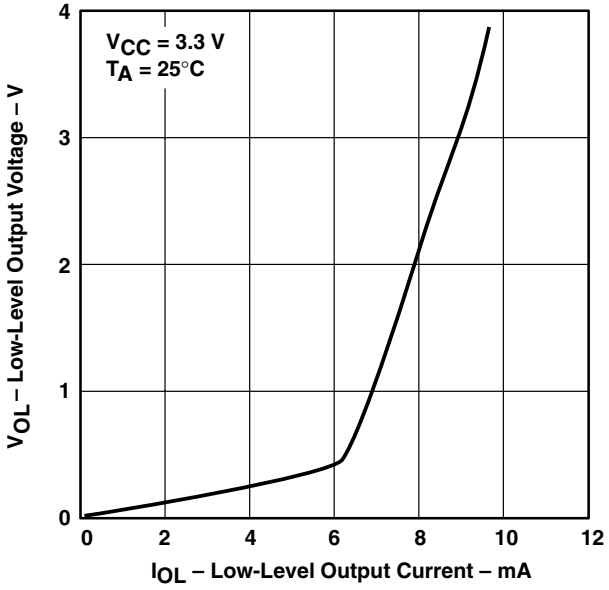
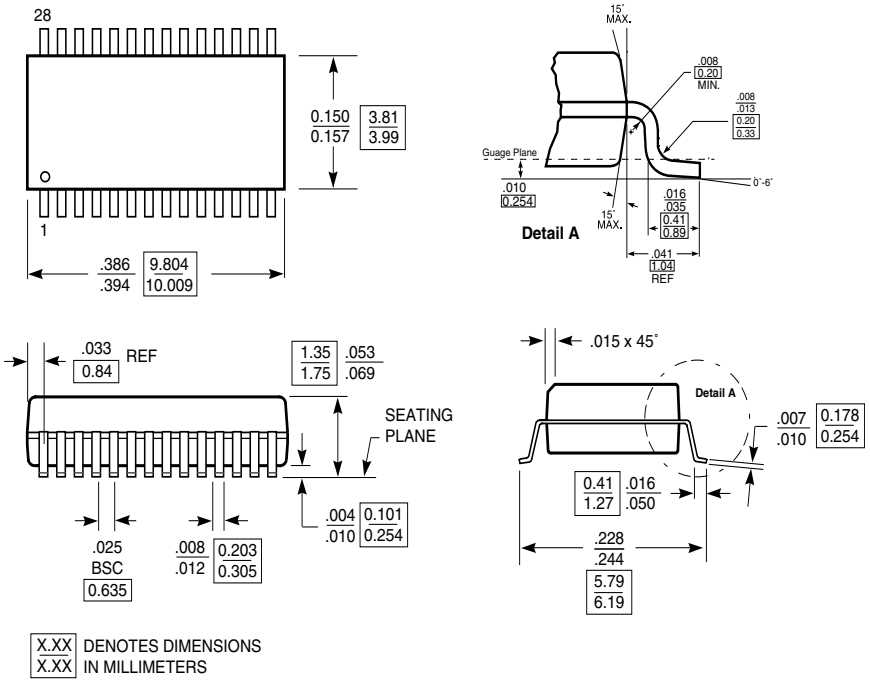
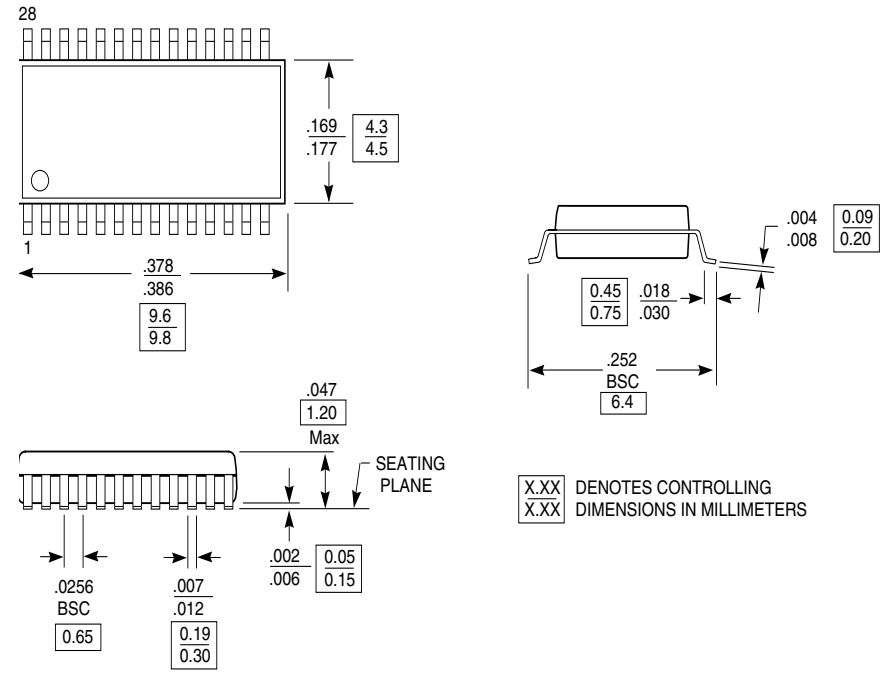


Figure 10

Packaging Mechanical: 28-Pin QSOP (Q)



Packaging Mechanical: 28-Pin TSSOP (L)



Ordering Information

Ordering Code	Package Code	Package Type
PI90LV044Q	Q	28-Pin 150-mil QSOP
PI90LV044QE	Q	Pb-free & Green, 28-Pin 150-mil QSOP
PI90LV044L	L	28-pin 170-mil TSSOP
PI90LV044LE	L	Pb-free & Green, 28-pin 170-mil TSSOP
PI90LVB044Q	Q	28-Pin 150-mil QSOP
PI90LVB044QE	Q	Pb-free & Green, 28-Pin 150-mil QSOP
PI90LVB044L	L	28-pin 170-mil TSSOP
PI90LVB044LE	L	Pb-free & Green, 28-pin 170-mil TSSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. Number of Transistors = TBD