

3.3V, Synchronous 16-Bit to 32-Bit FET Mux/Demux BusSwitch

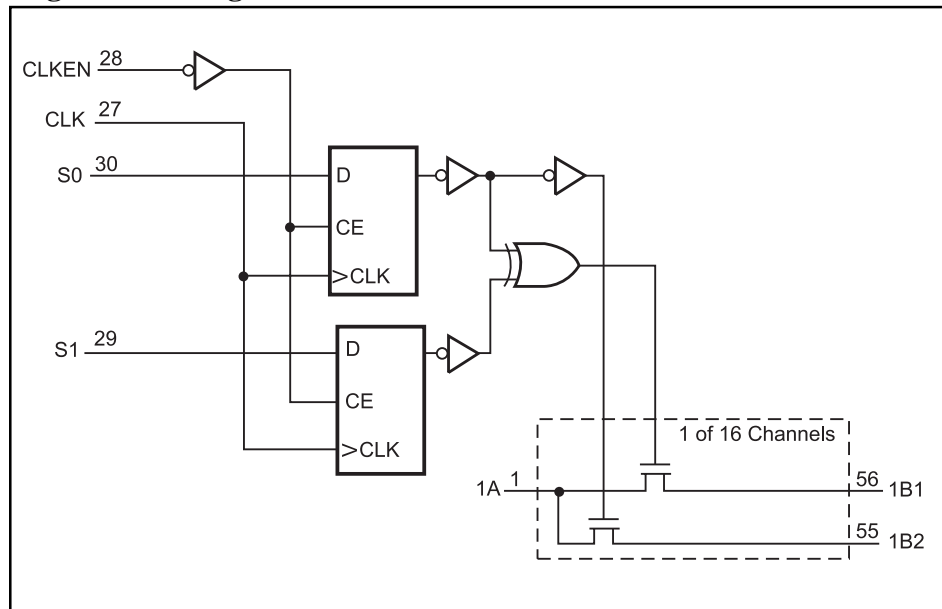
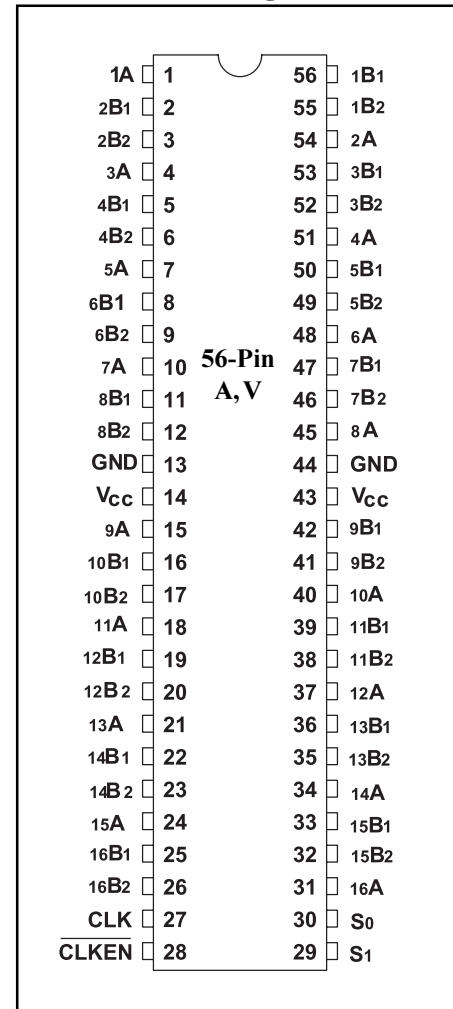
Product Features

- Near-Zero propagation delay.
- 5Ω Switches Connect Between Two Ports
- Packages Available :
 - 56-pin 240mil Wide Thin Plastic TSSOP(A)
 - 56-pin 300mil Wide Plastic SSOP(V)

Product Description

Pericom Semiconductor's PI3B series of logic circuits are produced using the company's advanced 0.35micron CMOS technology.

The PI3B16232 is a 3.3 volt, 16-bit to 32-bit synchronous switch. Two select inputs (S0 and S1) control the data flow. A clock (CLK) and a clock enable ($\overline{\text{CLKEN}}$) synchronize the device operation. When $\overline{\text{CLKEN}}$ is high, the bus switch remains in the last clocked function.

Logic Block Diagram

Product Pin Configuration

Truth Table

S1	S0	CLK	$\overline{\text{CLKEN}}$	Function
X	X	X	H	Last State
L	L	↑	L	Disconnect
L	H	↑	L	A = B1 and A = B2
H	L	↑	L	A = B1
H	H	↑	L	A = B2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage Range	-0.5V to +4.6V
DC Input Voltage	-0.5V to +4.6V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 3.0V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}	—	—	±1	µA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND	—	—	±1	µA
I _{OZH}	High Impedance Output Current	0 ≤ A, B ≤ V _{CC}	—	—	±1	µA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., V _{IN} = -18mA	—	-0.7	-1.2	V
R _{on}	Switch on Resistance ⁽³⁾	V _{CC} = Min., I _{IN} = 0.0V, I _{ON} = 48mA or 64mA	—	5	8	Ω
		V _{CC} = Min., V _{IN} = 2.4 V, I _{ON} = 15mA	—	10	15	Ω

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	3.0	pF
C _{ON}	A/B Capacitance, Switch On	V _{IN} = 0V	25.0	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, T_A = 25°C ambient and maximum loading.
3. Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = MAX.	V _{IN} = GND or V _{CC}	—	—	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = MAX.	V _{IN} = 3.0 V ⁽³⁾	—	—	750	μA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., A and B Pins Open BE = GND Control Input Toggling 50% Duty Cycling		—	—	0.25	mA/ MHz

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for applicable device.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input (control inputs only); A and B pins do not contribute to I_{CC}.
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameter	Description	Test Conditions ⁽¹⁾	V _{CC} = 3.0 to 3.6V		Units
			Min.	Max.	
f _{CLK}	Clock Frequency		0	150	MHz
t _w	Pulse Duration	CLK high or low	3.3		ns
t _s	Setup Time	S0, S1 before CLK↑	1.9		
		CLKEN before CLK↑	1.9		
t _h	Hold Time	S0, S1 after CLK↑	1		
		CLKEN after CLK↑	1.8		
t _{en}	Enable Time	CLK to B1, B2	1	5	
t _{dis}	Disable Time	CLK to B1, B2	1	6	
t _{pd1} ^(2,3)	Propagation Delay	A to B		0.25	
t _{pd2}	Propagation Delay	CLK to A	1	4.5	

Notes:

1. See Test Circuits and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagational delay other than the RC delay of ON resistance of the switch and the load capacitance.