

NC7SZ05 TinyLogic® UHS Inverter (Open Drain Output)

General Description

The NC7SZ05 is a single Inverter with open drain output stage from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The input and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage. The open drain output stage tolerates voltages up to 6V independent of V_{CC} when in the high impedance state.

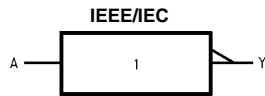
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- Open drain output for OR tied applications
- Ultra High Speed; t_{PD} 1.9 ns Typ into 50 pF at 5V V_{CC}
- High Output I_{OL} Drive; +24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage Tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ05M5X	MA05B	7Z05	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7SZ05P5X	MAA05A	Z05	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ05L6X	MAC06A	C6	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Logic Symbol



Pin Descriptions

Pin Names	Description
A	Input
Y	Output
NC	No Connect

Function Table

$$Y = \bar{A}$$

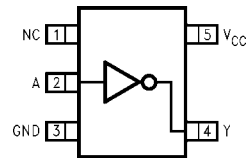
Input	Output
A	Y
L	*H
H	L

H = HIGH Logic Level L = LOW Logic Level
*H = HIGH Impedance output state (Open Drain)

TinyLogic® is a registered trademark of Fairchild Semiconductor Corporation.
MicroPak™ are trademarks of Fairchild Semiconductor Corporation.

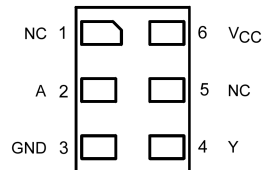
Connection Diagrams

Pin Assignments for SOT23 and SC70



(Top View)

Pad Assignments for MicroPak



(Top Thru View)

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +6V
DC Input Voltage (V_{IN})	-0.5V to +6V
DC Output Voltage (V_{OUT})	-0.5V to +6V
DC Input Diode Current (I_{IK})	
@ $V_{IN} < -0.5V$	-50 mA
@ $V_{IN} > 6V$	+20 mA
DC Output Diode Current (I_{OK})	
@ $V_{OUT} < -0.5V$	-50 mA
@ $V_{OUT} > 6V, V_{CC} = GND$	+20 mA
DC Output Current (I_{OUT})	+50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_1); (Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	
SOT23-5	200 mW
SC70-5	150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Operating Temperature (T_A)	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 ns/V to 20 ns/V
$V_{CC} = 3.3V \pm 0.3V$	0 ns/V to 10 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/W
SC70-5	425°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specification should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

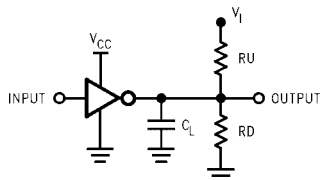
DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Unit	Conditions
			Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V	
V_{IL}	LOW Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.25 V_{CC} 0.3 V_{CC}			0.25 V_{CC} 0.3 V_{CC}		V	
I_{LKG}	HIGH Level Output Leakage Current	1.65 to 5.5	± 5			± 10		μA	$V_{IN} = V_{IL}$ $V_{OUT} = V_{CC}$ or GND
V_{OL}	LOW Level Output Voltage	1.65 1.8 2.3 3.0 4.5	0.0 0.0 0.0 0.0 0.0			0.1 0.1 0.1 0.1 0.1		V	$V_{IN} = V_{IH}$ $I_{OL} = 100 \mu A$
		1.65 2.3 3.0 4.5	0.08 0.10 0.15 0.22 0.22			0.24 0.3 0.4 0.55 0.55		V	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ $I_{OL} = 16 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 32 \text{ mA}$
I_{IN}	Input Leakage Current	0 to 5.5	± 1			± 10		μA	$0 \leq V_{IN} \leq 5.5V$
I_{OFF}	Power Off Leakage Current	0.0	1			10		μA	V_{IN} or $V_{OUT} = 5.5V$
I_{CC}	Quiescent Supply Current	1.65 to 5.5	2.0			20		μA	$V_{IN} = 5.5V, GND$

AC Electrical Characteristics										
Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = 40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t _{PZL}	Propagation Delay	1.65	1.5	5.5	12.9	1.5	13.4	ns	C _L = 50 pF R _U = 500Ω R _D = 500Ω V _I = 2 × V _{CC}	Figures 1, 3
		1.8	1.5	4.6	10.5	1.5	11.0			
		2.5 ± 0.2	0.8	3.0	7.0	0.8	7.5			
		3.3 ± 0.3	0.8	2.4	5.0	0.8	5.2			
		5.0 ± 0.5	0.5	1.9	4.3	0.5	4.5			
t _{PLZ}	Propagation Delay	1.65	1.5	5.0	12.9	1.5	13.4	ns	C _L = 50 pF R _U = 500Ω R _D = 500Ω V _I = 2 × V _{CC}	Figures 1, 3
		1.8	1.5	4.1	10.5	1.5	11.0			
		2.5 ± 0.2	0.8	2.5	7.0	0.8	7.5			
		3.3 ± 0.3	0.8	2.1	5.0	0.8	5.2			
		5.0 ± 0.5	0.5	1.2	4.3	0.5	4.5			
C _{IN}	Input Capacitance	0	4					pF		
C _{OUT}	Output Capacitance	0	6					pF		
C _{PD}	Power Dissipation	3.3	3.6					pF	(Note 3)	Figure 2
	Capacitance	5.0	6.5							

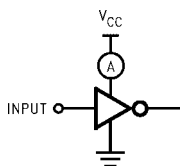
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC} \text{ static})$

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; t_r = t_f = 1.8 ns
 PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. AC Test Circuit

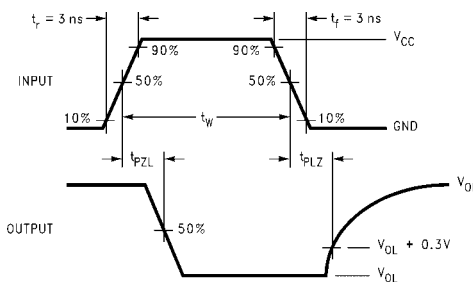


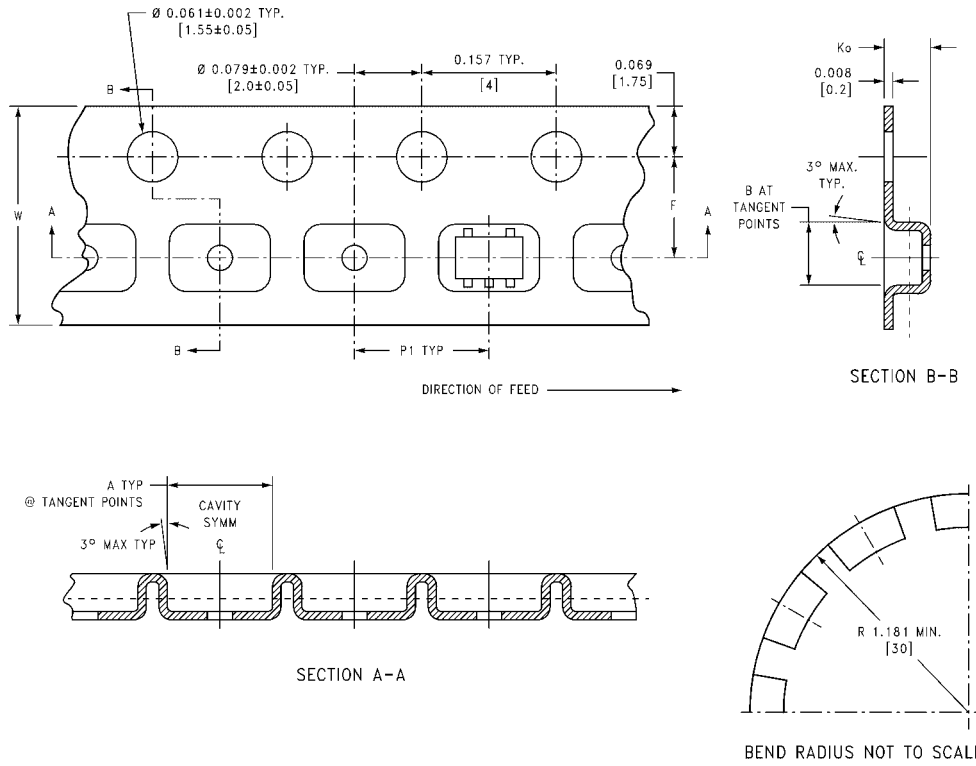
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for SOT23 and SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

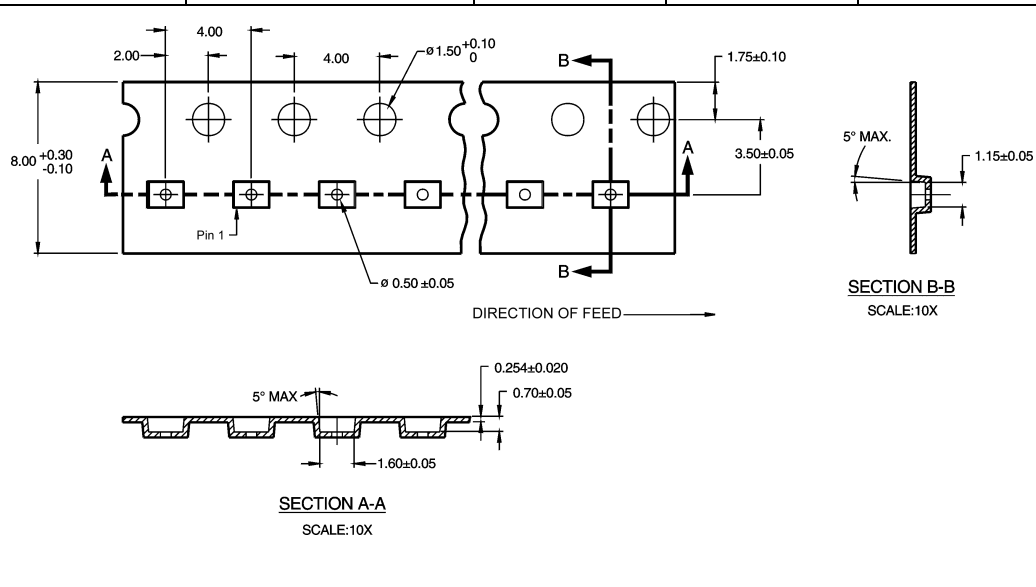


Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

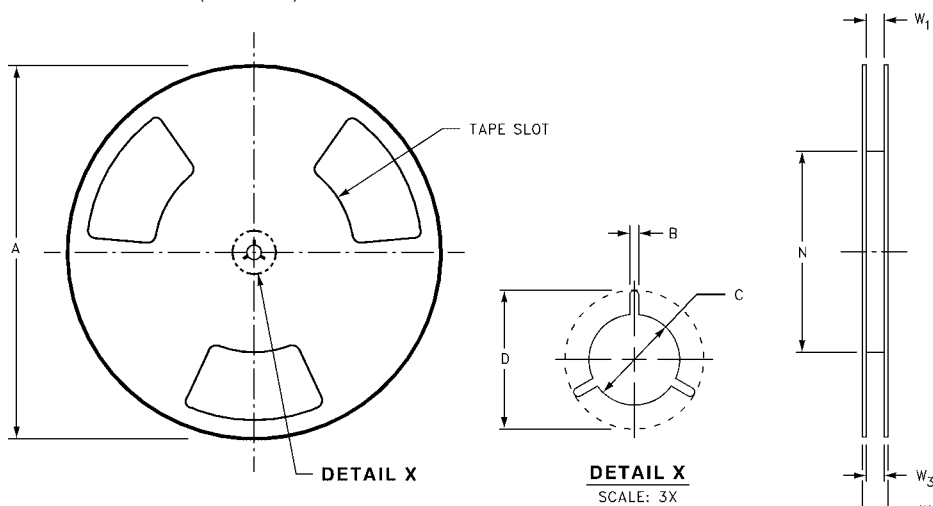
Tape and Reel Specification (Continued)

TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

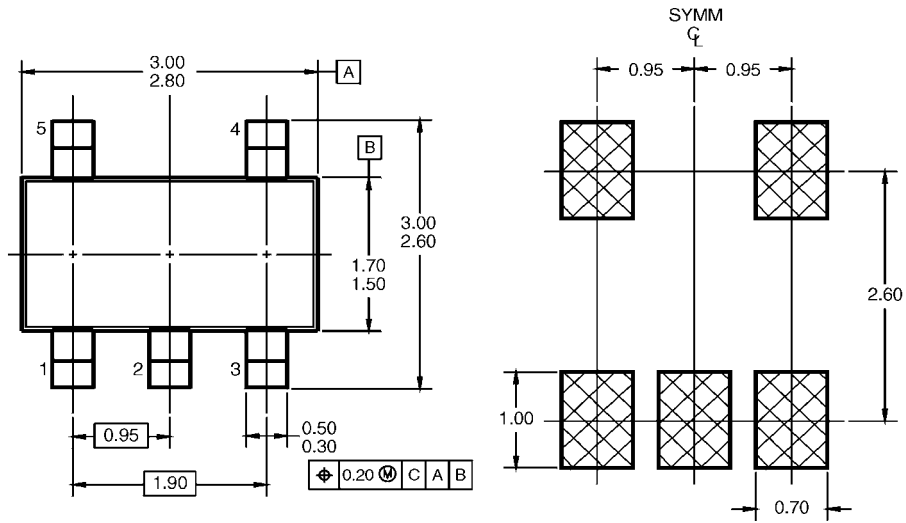


REEL DIMENSIONS inches (millimeters)

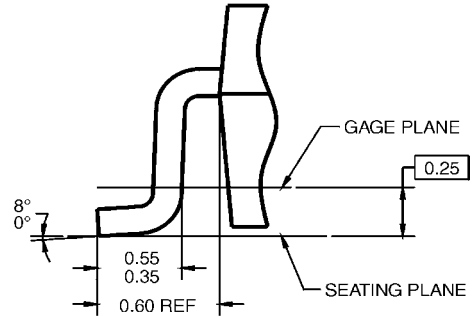
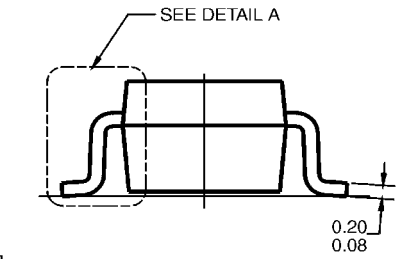


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION

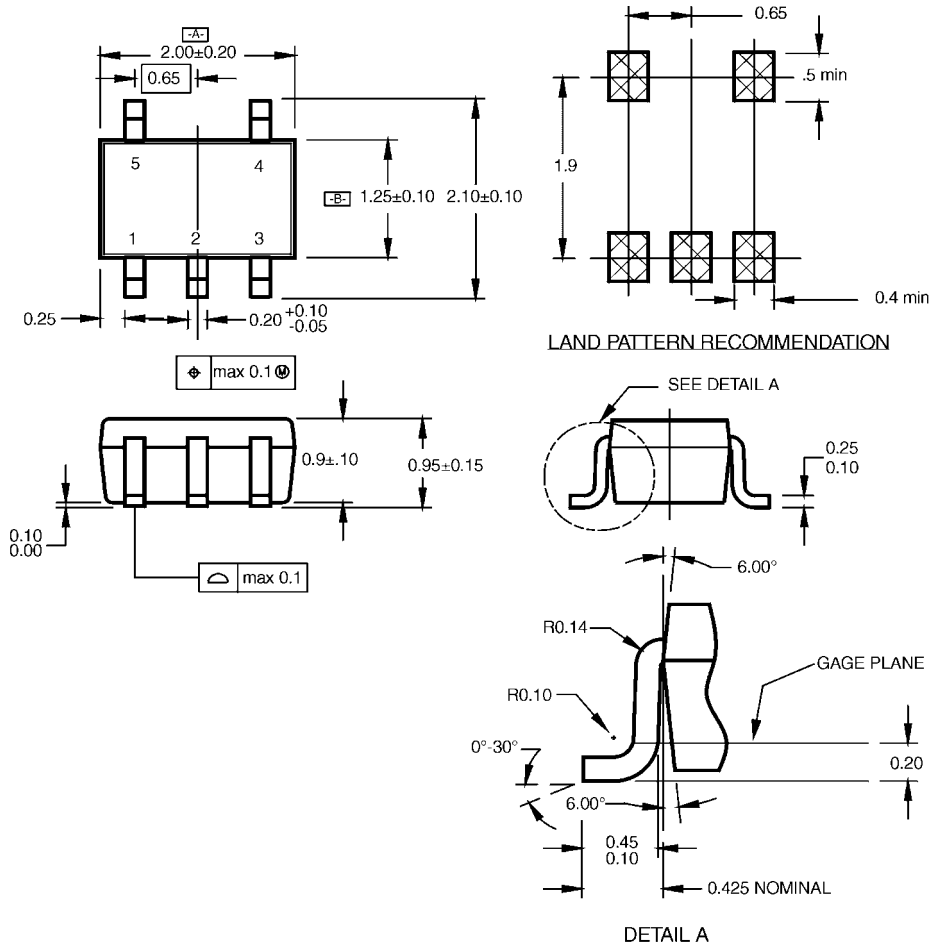


- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA, DATED JANUARY 1999.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.

MA05BRevC

**5-Lead SOT23, JEDEC MO-178, 1.6mm
Package Number MA05B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



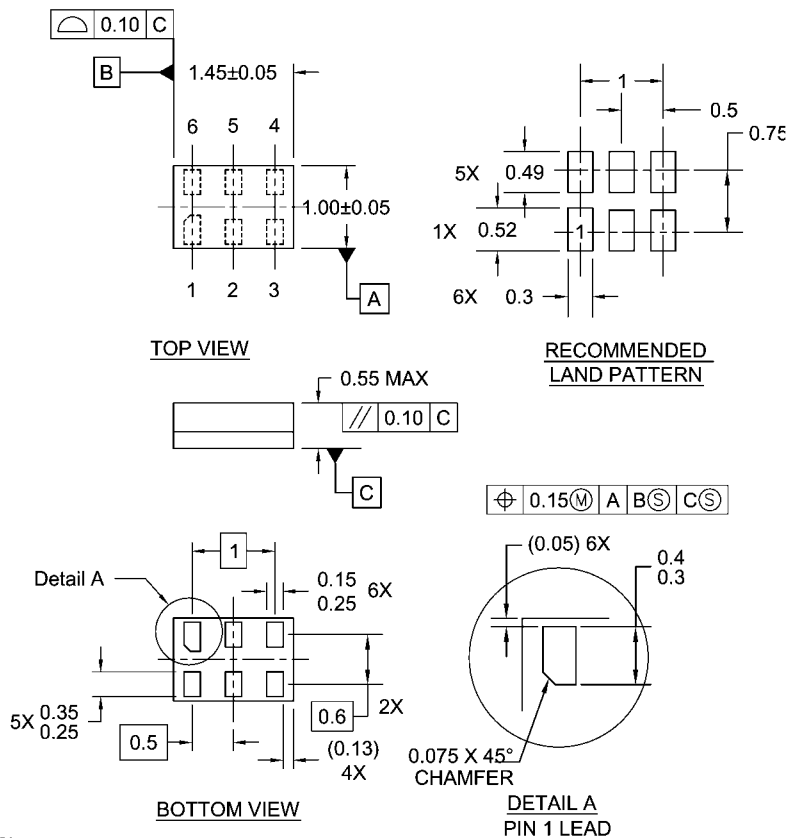
NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA05ARevC

**5-Lead SC70, EIAJ SC-88a, 1.25mm Wide
Package Number MAA05A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com