FEDL70Q5110LA-01
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OKI Semiconductor
ML70Q5110LA

Bluetooth Baseband Controller IC

GENERAL DESCRIPTION

The ML70Q5110LA is a CMOS digital IC for use in 2.4 GHz band Bluetooth™ systems. This IC incorporates the ARM7TDMI® as the CPU core, features a highly expandable architecture, and supports the interfaces for a variety of applications. Used in conjunction with the ML7050LA (Bluetooth RF Transceiver IC) and the OKI Bluetooth Protocol Stack Software, data/voice communications are possible while maintaining interconnectivity with other Bluetooth systems. Also this IC is equiped with 2 Mbit Flash ROM to reduce the external parts.

FEATURES

- Compliant to Bluetooth Specification (Ver. 1.1)
- The ARM7TDMI® is installed as the CPU (operation at a maximum of 32 MHz in this LSI)
- 1-Ch, 16-bit auto-reload timer
- 3-Ch, 18-bit auto-reload timer
- Interrupt controller (17 causes)
- Built-in 8 kbyte, 4-Way Unified Cache
- Built-in 32 kbyte
- Up to a total of 2 Mbyte of SRAM, ROM, and Flash ROM can be connected to the external memory bus.
- Built-in 2Mbit Flash ROM
  - Endurance 10^4 cycles
- Selectable master clock (12/13/16 MHz).
- PCM-CVSD transcoder is installed.
- Installed interfaces:
  - UART(*) interface (Up to 921.6 Kbps)
  - USB(*) interface (conforms to USB1.1)
  - UART/synchronous serial port interface
  - General-purpose I/O interface (programmable interrupts)
  - PCM interface (PCMLinear/A-law/μ-law can be selected)
  - JTAG interface

  (*) This mark indicates interfaces that support the HCI command.
- Built-in Regulator and Power-on-Reset
- Single power supply voltage: 3.0 to 3.6 V
- Package: 144-pin BGA (P-LFBGA144-1111-0.80-MC)
  (Dimensions: 11 mm × 11 mm × 1.5 mm; pin pitch: 0.8 mm)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	—	–0.3 to +4.5	V
Input voltage	V_I	—	–0.3 to +4.5	V
Allowable power dissipation	P_d	—	1.35	W
Storage temperature	T_{stg}	—	–55 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	—	3.0	3.3	3.6	V
“H” level input voltage	Vih	—	2.2	—	3.6	V
“L” level input voltage	Vil	—	0	—	0.8	V
Operating temperature	Ta	—	–40	—	85	°C

INTERNAL FLASH ROM PROGRAMMING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	—	3.0	3.3	3.6	V
Operating temperature	Ta	During Read	–40	—	85	°C
		During Programming	0	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics(1) (Except USB port)

(V_{DD} = 3.3 V ±0.3 V, Ta = –40 to 85°C)

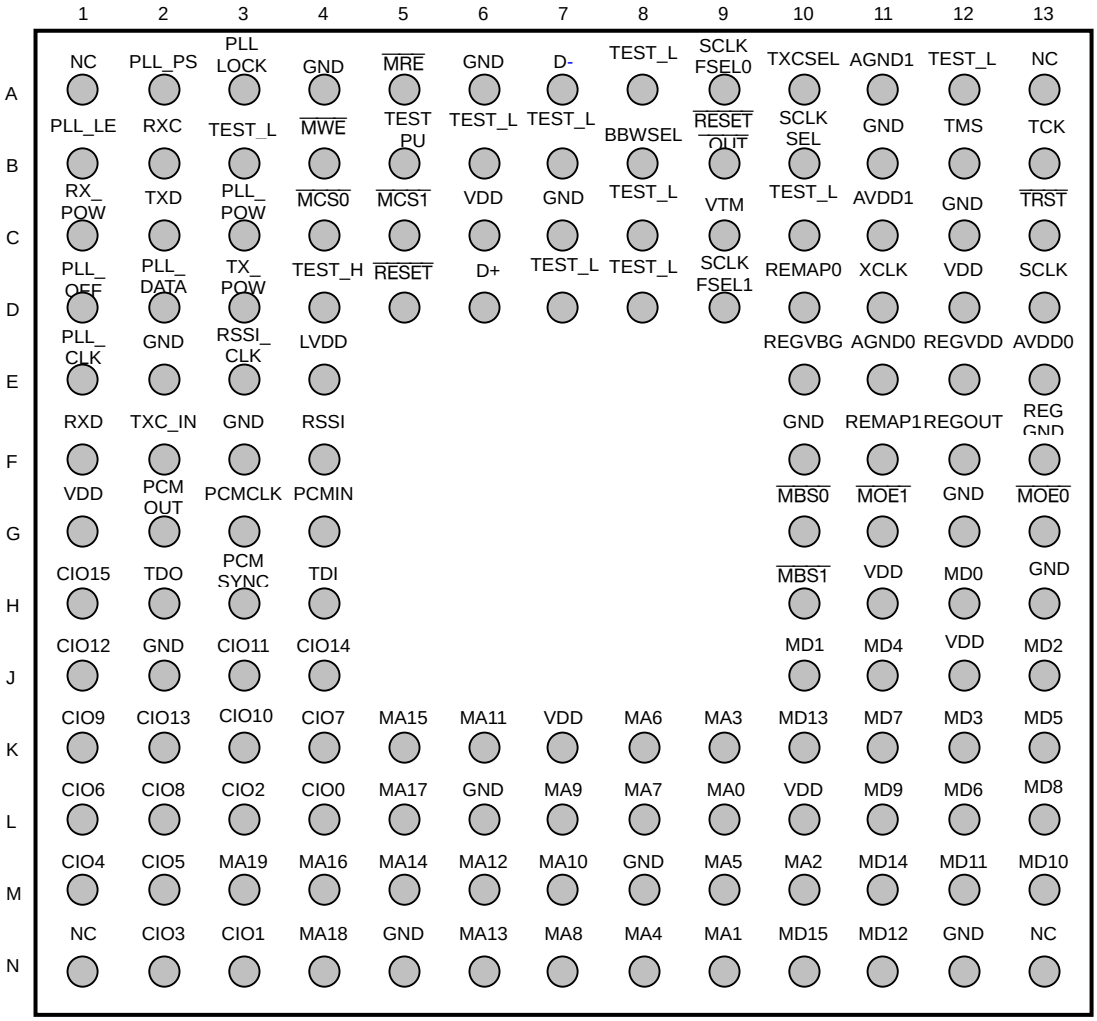
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
“H” level output voltage	Voh	Ioh = –2 mA	2.4	—	—	V
“L” level output voltage	Vol	Iol = 2mA	—	—	0.4	V
Input leak current	Ii	Vi = GND to 3.6 V	–10	—	10	µA
Output leak current	Io	Vo = GND to V_{DD}	–10	—	10	µA
Power supply current (during operation)	Iddo	During 32 MHz operation	0	70	90	mA
Power supply current (during stand-by)	Idds	CLK Stopped	—	200	800	µA

DC Characteristics(2) USB port (D+, D–)

(V_{DD} = 3.3 V ±0.3 V, Ta = –40 to 85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Differential input sensitivity	V_{DI}	{(D+) – (D–)}	0.2	—	—	V
Differential common mode range	V_{CM}	Includes VDI	0.8	—	2.5	V
Single ended receiver threshold	V_{SE}	—	0.8	—	2.0	V
“H” output voltage	V_{OH}	15 KΩ to GND	2.8	—	3.6	V
“L” output voltage	V_{OL}	1.5 KΩ to 3.6 V	—	—	0.3	V
Output leakage current	I_{LO}	0 V < V_{IN} < V_{DD}	–10	—	+10	µA

PIN PLACEMENT



TOP VIEW

PIN DESCRIPTIONS

RF I/F

Pin Name	Direction [*0]	Internal Pull Up/Down	Initial Value	Pin Placement	Description
TXD	O	—	L	C2	Transmit data output (To ML7050LA Pin# A8)
RXD	I	—	—	F1	Receive data input (To ML7050LA Pin# H5)
PLL_DATA	O	—	L	D2	PLL setting data output (To ML7050LA Pin# H3)
PLL_CLK	O	—	L	E1	PLL setting clock output (To ML7050LA Pin# G3)
PLL_LE	O	—	L	B1	PLL setting load enable output (To ML7050LA Pin# H4)
PLL_OFF	O	—	L	D1	PLL Open-loop/Closed-loop control signal output (To ML7050LA Pin# G8)
PLL_POW	O	—	H	C3	Local transmit circuit power control signal output (To ML7050LA Pin# A7)
TX_POW	O	—	H	D3	Transmit power control signal output (To ML7050LA Pin# B6)
RX_POW	O	—	H	C1	Receive power control signal output (To ML7050LA Pin# B3)
RSSI	I	Pull down	—	F4	Receive field strength data input
RSSI_CLK	O	—	H	E3	RSSI transfer clock
PLL_PS	O	—	L	A2	PLL power control signal output
PLLLOCK	I	Pull down	—	A3	PLL lock signal input
RXC	O	—	L	B2	Bluetooth receive clock output (1 MHz)
TXC_IN	I	Pull down	—	F2	Bluetooth transmit clock input (1 MHz) When the transmit clock is used by a clock (RXC) that is generated from the receive data, set TXCSEL(Pin# A10) to H and connect to RXC(Pin# B2).
TXCSEL	I	Pull down	—	A10	Bluetooth transmit clock setting pin L: Select 1 MHz divided by internal PLL. H: Select TXC_IN input signal.

[*0] "I" = Input, "O" = Output, "I/O" = Input/Output, "Oc" = Open Collector

CLK and Configuration

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
SCLK	I	—	—	D13	Master clock (12, 13 or 16 MHz) input pin (Power level: CMOS level)
XCLK	I	—	—	D11	User clock input pin
SCLKSEL	I	Pull down	—	B10	System clock select pin L: Select CLK divided by internal PLL H: Select XCLK input signal
SCLKFSEL0	I	Pull down	—	A9	Master clock select pin SCLKFSEL[1:0] = "00" : 12 MHz "01" : 13 MHz "10" : 16 MHz "11" : Forbidden
SCLKFSEL1	I	Pull down	—	D9	
$\overline{\text{RESET}}$	I	—	—	D5	Hardware reset pin (Reset = L)
$\overline{\text{RESET\_OUT}}$	O	—	—	B9	Hardware reset pin (Reset = L), Output
BBWSEL	I	Pull down	—	B8	BANK0 region bit width select pin L: 8-bit H: 16-bit
REMAP0	I	—	—	D10	REMAP select pin during boot up REMAP[1:0] = "00" Forbidden "01" Stacked Flash ROM "10" External $\overline{\text{MCS1}}$ device "11" External $\overline{\text{MCS0}}$ device
REMAP1	I	—	—	F11	

Memory I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
MA[19:0]	O	—	L	[*1]	External address bus
MD[15:0]	I/O	Pull up	—	[*2]	External data bus
$\overline{\text{MWE}}$	O	—	H	B4	External write enable signal output
$\overline{\text{MRE}}$	O	—	H	A5	External read enable signal output
$\overline{\text{MCS0}}$	O	—	H	C4	External space 0 chip select
$\overline{\text{MCS1}}$	O	—	H	C5	External space 1 chip select
$\overline{\text{MBS0}}$	O	—	H	G10	External lower byte select
$\overline{\text{MBS1}}$	O	—	H	H10	External upper byte select
$\overline{\text{MOE0}}$	O	—	H	G13	External $\overline{\text{MCS0}}$ device output enable ($\overline{\text{MCS0}}$ and $\overline{\text{MRE}}$ OR output)
$\overline{\text{MOE1}}$	O	—	H	G11	External $\overline{\text{MCS1}}$ device output enable ($\overline{\text{MCS1}}$ and $\overline{\text{MRE}}$ OR output)

[*1] MA19: M3; MA18: N4; MA17: L5; MA16: M4; MA15: K5; MA14: M5
MA13: N6; MA12: M6; MA11: K6; MA10: M7; MA9: L7; MA8: N7; MA7: L8
MA6: K8; MA5: M9; MA4: N8; MA3: K9; MA2: M10; MA1: N9; MA0: L9

[*2] MD15: N10; MD14: M11; MD13: K10; MD12: N11; MD11: M12; MD10: M13
MD9: L11; MD8: L13; MD7: K11; MD6: L12; MD5: K13; MD4: J11; MD3: K12;
MD2: J13; MD1: J10; MD0: H12

USB I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
D+	I/O	—	Z	D6	USB data
D–	I/O	—	Z	A7	USB data

UART I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
SOUT	O	—	H	H1	ACE transmit serial data (Pin shared with GPIO15)
SIN	I	—	—	J4	ACE receive serial data (Pin shared with GPIO14)
DCD	I	—	—	K2	Data carrier detection (Pin shared with GPIO13)
RTS	O	—	H	J1	ACE transmit data ready (Pin shared with GPIO12)
CTS	I	—	—	J3	ACE transmit ready (Pin shared with GPIO11)
DSR	I	—	—	K3	Receive data ready (Pin shared with GPIO10)
DTR	O	—	H	K1	Receive ready (Pin shared with GPIO9)
RI	I	—	—	L2	Ring indicator (Pin shared with GPIO8)

SIO I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
STXD	O	—	H	K4	Serial data output (Pin shared with GPIO7)
SRXD	I	—	—	L1	Serial data input (Pin shared with GPIO6)
STDXCLK	I/O	—	—	M2	Clock for serial data output (Pin shared with GPIO5) During initialization: input
SRDXCLK	I/O	—	—	M1	Clock for serial data input (Pin shared with GPIO4) During initialization: input

µPLAT_SIO I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
UTXD	O	—	H	N2	Serial data output (Pin shared with GPIO3)
URXD	I	—	—	L3	Serial data input (Pin shared with GPIO2)

GPIO I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
GPIO[15:0]	I/O	—	—	[*3]	Parallel I/O data During initialization: input

JTAG I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
TDI	I	Pull down	—	H4	Serial data input
TDO	O	—	L	H2	Serial data output
$\overline{\text{TRST}}$	I	Pull down	—	C13	Reset pin
TMS	I	Pull down	—	B12	Mode setting pin
TCK	I	Pull down	—	B13	Serial data clock

PCM I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
PCMOUT	O	—	L	G2	PCM data output
PCMIN	I	Pull down	—	G4	PCM data input
PCMSYNC	I/O	Pull down	—	H3	PCM sync signal (8 kHz) During initialization: input (can be switched by an internal register)
PCMCLK	I/O	Pull down	—	G3	PCM clock (64 kHz/128 kHz) During initialization: input (can be switched by an internal register)

[*3] CIO15: H1 GPIO15/SOUT (UART I/F)
CIO14: J4 GPIO14/SIN (UART I/F)
CIO13: K2 GPIO13/DCD (UART I/F)
CIO12: J1 GPIO12/RTS (UART I/F)
CIO11: J3 GPIO11/CTS (UART I/F)
CIO10: K3 GPIO10/DSR (UART I/F)
CIO9: K1 GPIO9/DTR (UART I/F)
CIO8: L2 GPIO8/RI (UART I/F)
CIO7: K4 GPIO7/STXD (SIO I/F)
CIO6: L1 GPIO6/SRXD (SIO I/F)
CIO5: M2 GPIO5/STXDCLK (SIO I/F)
CIO4: M1 GPIO4/SRXDCLK (SIO I/F)
CIO3: N2 GPIO3/UTXD (µPLAT_SIO I/F)
CIO2: L3 GPIO2/URXD (µPLAT_SIO I/F)
CIO1: N3 GPIO1
CIO0: L4 GPIO0

TEST I/F

Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
TEST_L	I	Pull down	—	[*4]	Test pin (input)
TEST_H	I	—	—	D4	Test pin (input)
TEST_PU	Oc	—	L	B5	Test monitor pin
VTM	I	—	—	C9	Test pin
NC	—	—	—	A1, A13, N1, N13	No Connection

Power, GND

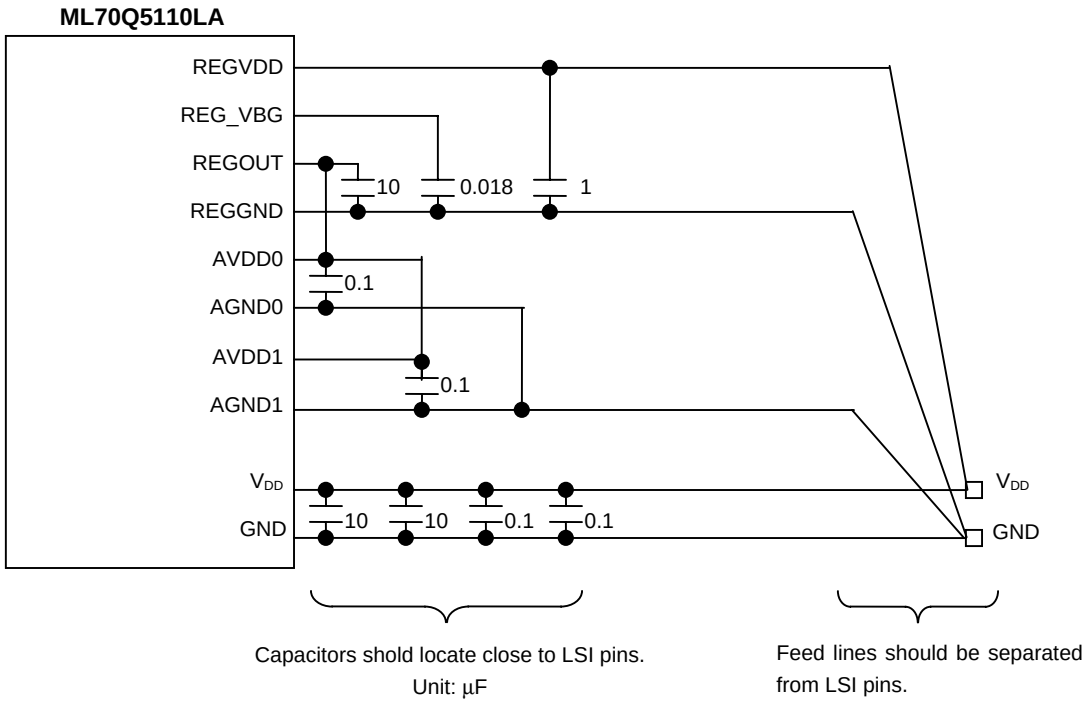
Pin Name	Direction	Internal Pull Up/Down	Initial Value	Pin Placement	Description
V_{DD}	—	—	—	[*5]	I/O power pin 3.3 V ±0.3 V
LVDD	—	—	—	E4	I/O power pin 3.3 V ±0.3 V (Same voltage to the V_{DD} for ML7050LA)
GND	—	—	—	[*6]	Digital block ground pin
AVDD0	—	—	—	E13	Analog block power pin 2.5 V ±0.25 V (Connect to REGOUT pin: F12)
AVDD1	—	—	—	C11	
AGND0	—	—	—	E11	Analog block ground pin (Connect to REGGND pin: F13)
AGND1	—	—	—	A11	
REGVDD	—	—	—	E12	Regulator power pin (3.0 to 3.6 V)
REGGND	—	—	—	F13	Regulator ground pin
REGOUT	—	—	—	F12	Regulator output
REGVBG	—	—	—	E10	Regulator reference voltage tuning

[*4] TEST_L (TEST5): A8
TEST_L (TEST4): D8
TEST_L (TEST3): C8
TEST_L (TEST2): B7
TEST_L (TEST1): D7
TEST_L (TEST0): B6
TEST_L (PLLSEL): C10
TSET_L (PLLEN): A12
TSET_L (SVCO1): B3

[*5] C6, G1, K7, J12, H11, D12, L10

[*6] B11, C7, A6, A4, E2, F3, J2, N5, L6, M8, N12, H13, G12, F10, C12

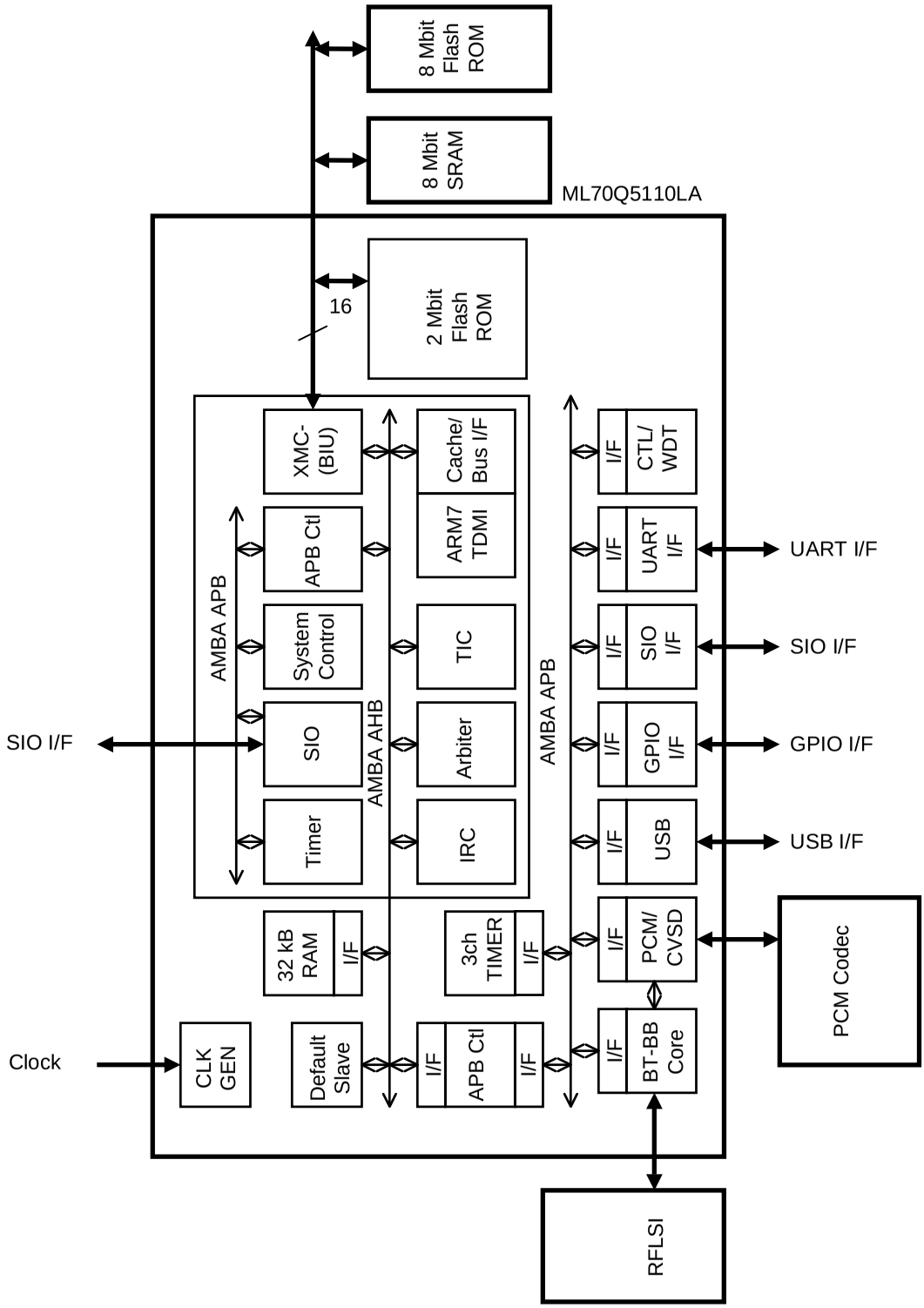
REFERENCE FOR VOLTAGE SUPPLY CIRCUIT



Example for ML70Q5110LA voltage supply circuit

The circuit is subject to change according to the specific LSI board design. Please contact Oki Electric Industry Co., Ltd. for detailed information.

BLOCK DIAGRAM



DESCRIPTION OF INTERNAL BLOCKS

CLKGEN Block

- Generates from the SCLK (12/13/16 MHz) clock that is supplied to each block
- STOP/HALT function
- External clock selection function

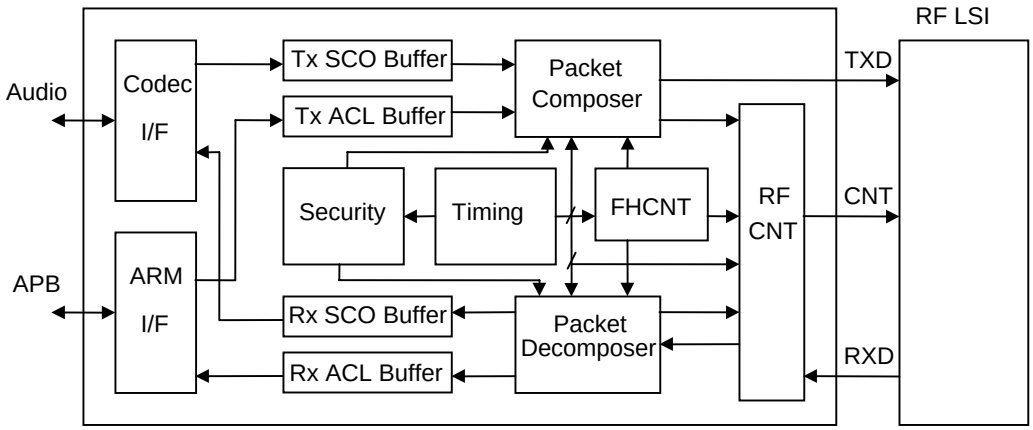
CTL/WDT Block

- Control of the frequency division function of the internal main clock
- Control of clock supplied to each peripheral
- Control of reset of each peripheral
- STOP/HALT control
- External clock selection control
- CIO switching function
- Watchdog timer function (interrupt/reset)
- 3 types of count stop functions

Timer Block

- 3 channels
- 18 bit timer counter for each channel
- Iterrupt at counter overflow
- Independent mode for each channel (one shot/interval/free run)

Baseband Core Block



- RF Controller
  - RF power supply control (PLL, TX, RX)
  - Local PLL frequency division ratio setting
  - Receive clock regeneration function
  - Synchronization detection (synchronizing within the permissable error limit of SyncWord)
  - Receive clock re-timing function
- FH Controller hopping
  - Sequence control
  - Frequency hopping selection function
  - CRC computation's initial value selection function
- Timing Generator
  - Bluetooth clock generation
  - Operation interrupts depend on mode (slot, scan, sniff, hold, park)
  - Sync detection timing generation (sync window ±10 μs)
  - PLL setting timing generation
  - Transmit/Receive timing generation
  - Multi-master timing management function
- Packet Composer
  - Access code generation (SyncWord generation, appending PR*TRAILER)
  - Packet header generation (HEC generation, scrambling, FEC encoding)
  - Payload generation (CRC generation, encryption, scrambling, FEC encoding)
  - Packet synthesis
- Packet Decomposer
  - Packet decomposition (separating the packet header and the payload)
  - Packet header processing (FEC decoding, descrambling, HEC error detection, header information separation)
  - Payload processing (FEC decoding, descrambling, encryption decoding, CRC judgement, payload separation)
- Security
  - Various key generation functions (initialization, link key, encryption key)
  - Certification function
  - Encryption function

USB Block

- Conforms to USB standard Ver. 1.1.
- Supports 12 Mbps transfer
- Supports 4 data transfer types (control transfer, bulk transfer, interrupt transfer, and isochronous transfer)
- Built-in USB transceiver circuit
- 5 or 6 built-in end points, and built-in FIFO for data storage
- 8-, 16-, 32-bit read/write is possible for the FIFOs of EP0 to EP5 (with byte control)

UART Block

- Full-duplex buffering method
- All status reporting function
- Built-in 64-byte transmit/receive FIFO
- Modem control based on CTS, DCD, and DSR
- Programmable serial interface
- 5-, 6-, 7-, 8-bit characters
- Generation and verification of odd parity, even parity, or no parity
- 1, 1.5, or 2 stop bits
- Programmable Baud Rate Generator (1200 bps to 921.6 kbps)
- Error servicing for parity, overrun, and framing errors

SIO Block

- UART/Synchronous type serial port interface
- UART Mode:
  - Data length: can be selected as 7 or 8 bits
  - Supports odd parity, even parity, or no parity
  - Error servicing for parity, overrun, and framing errors
  - Supports 1 or 2 stop bits
  - Full-duplex communication is possible
- Clock synchronization mode:
  - Data length: can be selected as 7 or 8 bits
  - Error servicing for overrun errors
  - Full-duplex communication is possible

µPLAT-SIO Block

- Start-stop synchronization type serial port interface
- Built-in dedicated baud rate generator
- Data length of 7 or 8 bits can be selected
- 1 or 2 stop bits can be selected.
- Supports odd or even parity
- Error servicing for parity, overrun, and framing errors
- Full-duplex communication is possible

PCM-CVSD Transcoder Block

- Application side I/O:
  - PCM Codec
  - APB-Bus (USB)
- Application-side format:
  - PCM linear (8, 16 bits/sample, 64 kHz sampling frequency)/A-law/µ-law
- Bluetooth-side format:
  - CVSD/A-law/µ-law
- All combinations of the above conversions are supported
- PCMSYMC/PCMCLK I/O can be switched (in the input state after initialization)

GPIO Block

- All 16 bits
- Input/Output selection possible for each bit
- Interrupts can be used for all bits
- Interrupt masks and interrupt modes can be set for all bits
- In the input state immediately after a reset

APPLICATION NOTES

Operation During Boot Up

- Remapping during boot up is performed according to external pins REMAP[1:0].

REMAP1	REMAP0		
L	L	:	Forbidden
L	H	:	Stack Flash ROM
H	L	:	Devices connected to external $\overline{\text{MCS1}}$
H	H	:	Devices connected to external $\overline{\text{MCS0}}$

- Bit width that corresponds to BANK0 during boot up is set according to external pin BBWSEL.

  BBWSEL = L : 8-bit
  BBWSEL = H : 16-bit

Clock Selection

- The CPU clock supply source is selected according to external pin SCLKSEL.

  SCLKSEL = L : Use 32/16/8/4 MHz clock that was divided down from the internal PLL output of 192 MHz that was generated from external pin SCLK. (Initial value is 32 MHz.)
  SCLKSEL = H : Use external pin XCLK.

  Note: The clock supply source can also be set by the CLKCNT register in the CTL/WDT block.

- Bluetooth transmission clock is selected according to external pin TXCSEL.

  TXCSEL = L : Use 1 MHz clock that was divided down from the internal PLL output (192 MHz).
  TXCSEL = H : Use external pin TXC_IN.

  Note: This clock can also be set by the CLKCNT register in the CTL/WDT block.

- SCLK selection (12/13/16 MHz).
  SCLKFSEL[1:0] = "00" : 12 MHz
  "01" : 13 MHz
  "10" : 16 MHz
  "11" : Forbidden

HCI Transport Selection

- HCI is selected (USB/UART) according to the logical value of GPIO0 at initial powerup of ML70Q5110LA.

  GPIO0 = L : UART is used as HCI.
  GPIO0 = H : USB is used as HCI.

USB Peripheral Circuit

- Please contact Oki Electric Industry Co., Ltd. when using USB.

Setting the UART Baud Rate

- Use the HCI_VS_Set_LC_Parameters command of the Vendor Specific Commands to set the UART baud rate.

  Available baud rate settings:
  1200/2400/4800/7200/9600/19.2K/38.4K/56K/57.6K/115.2K/230.4K/345.6K/460.8K/921.6K
  (Initial value is 115.2 kbps.)

Setting the PCM-CVSD Transcoder

- Please use the HCI_VS_Set_LC_Parameters command of the Vendor Specific Commands in HCI to set the PCM-CVSD transcoder parameters.

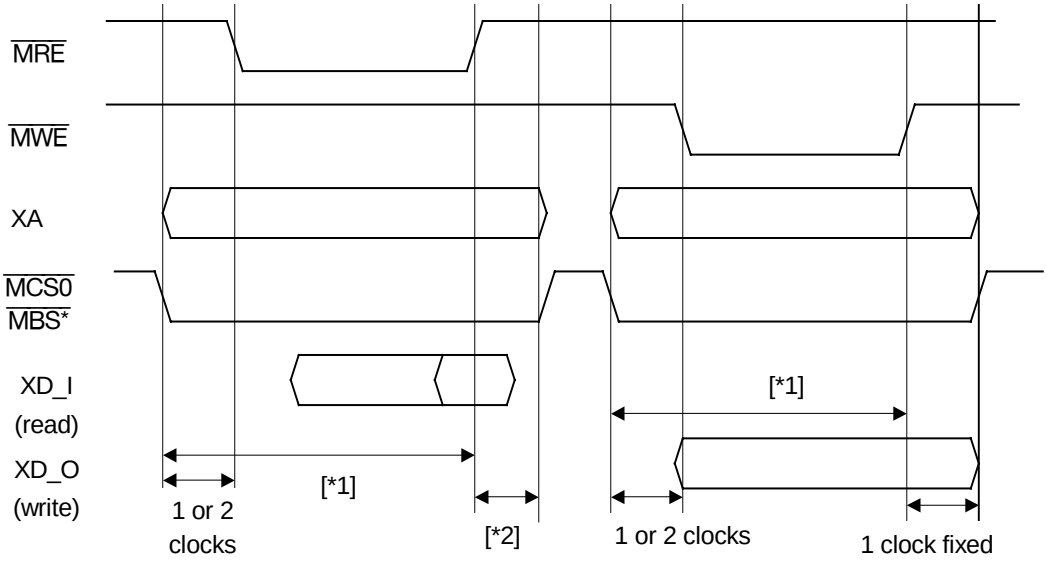
- It is possible to set the following parameters using the VCCTL command:
  - PCMSYNC/PCMCLK mode (in the input state after initialization)
  - Mute reception (initial setting: OFF)
  - Air coding
    CVSD (initial setting)/μ-law/A-law
  - Interface coding
    Linear (initial setting)/μ-law/A-law
  - PCM format (data width of one PCM Linear sample)
    8-bit (initial setting)/14-bit/16-bit
  - Serial interface format
    Short frame (initial setting)/long frame
  - Application interface mode
    PCM Codec I/F (initial setting)/APB I/F

External Memory

- ML70Q5110LA specifications for the devices that are connected to $\overline{MCS0}$ and $\overline{MCS1}$ are explained below.

- When the device is connected to $\overline{MCS0}$:
  - 1 memory bank
  - Bus width: 8 or 16 bits
  - Byte access control: $\overline{MBS*}$/$\overline{MWE}$
  - Supported devices:
    Normal SRAM, Flash Memory, Page mode Flash memory

Bus timing to the device connected to $\overline{MCS0}$



[*1] Access time:
3, 4, 5, 6, 7, 8 clock cycles (including 1 clock cycle for set-up)
6, 8, 10, 12, 14, 16 clock cycles (including 2 clock cycles for set-up)

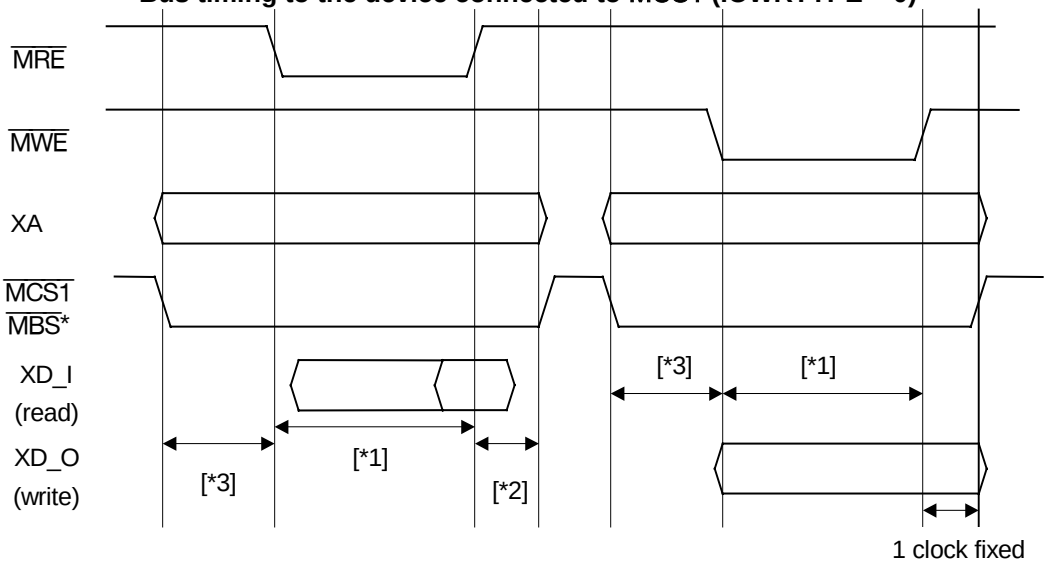
[*2] Data OFF time:
1, 2, 3, 4 clock cycles

Note: Oki software settings:
- Insert the maximum wait immediately after reset.
- Page mode: OFF
- During operation (32 MHz operation),
  Access time: 3 clock cycles
  Data OFF time: 1 clock cycle

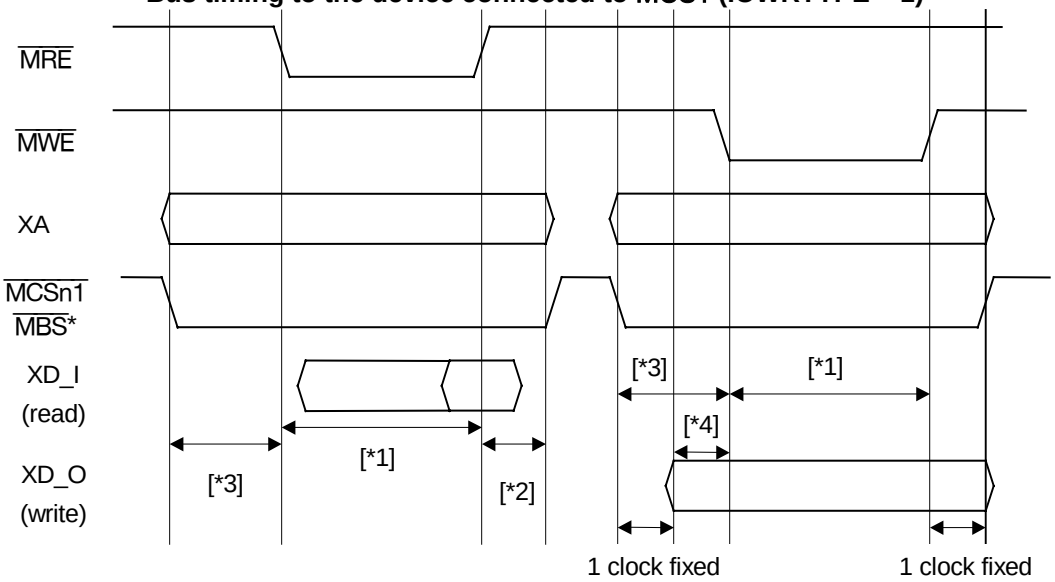
Note: A device with an access time of 120 nsec or less is recommended.

- When the device is connected to $\overline{\text{MCS1}}$:
  - 1 memory bank
  - Bus width: 8-bit or 16-bit
  - Byte access control: $\overline{\text{MBS}}$*/$\overline{\text{MWE}}$

Bus timing to the device connected to $\overline{\text{MCS1}}$ (IOWRTYPE = 0)



Bus timing to the device connected to $\overline{\text{MCS1}}$ (IOWRTYPE = 1)



[*1] Access time:
2, 4, 8, 16, 32 clock cycles (including 1 clock cycle for set-up)

[*2] Data OFF time:
1, 2, 3, 4 clock cycles

[*3] Address set-up time:
1, 2, 3, 4 clock cycles

[*4] Write data set-up time:
0 clock cycles (IOWRTYPE = 0)
0, 1, 2, 3 clock cycles (IOWRTYPE = 1)

Relationship between address set-up time and write data set-up time (when IOWRTYPE = 1)

- Address set-up time:
  1 clock cycle (write data set-up: 0 clock cycles)
  2 clock cycles (write data set-up: 1 clock cycle)
  3 clock cycles (write data set-up: 2 clock cycles)
  4 clock cycles (write data set-up: 3 clock cycles)

Note: Oki software settings:
- Insert the maximum wait immediately after reset.
- IOWRTYPE = 0
- During operation (32 MHz operation),
  Access time: 2 clock cycles
  Data OFF time: 1 clock cycle
  Address set-up time: 1 clock cycle

  Note: A device with an access time of 120 nsec or less is recommended.

- Miscellaneous
  - MA0 is not used with devices that have a 16-bit data bus.
    Connect MA1 to device A0. (MA0 is Open.)
  - Connect MA0 to device A0 for devices that have an 8-bit data bus.
  - $\overline{\text{MOE0}}$ is the AND signal for $\overline{\text{MCS0}}$ and $\overline{\text{MRE}}$.
    Perform an open process when this is not in use.
  - $\overline{\text{MOE1}}$ is the AND signal for $\overline{\text{MCS1}}$ and $\overline{\text{MRE}}$.
    Perform an open process when this is not in use.

Process when interface pins are unused

- The following tables show the processes that are performed when interface pins are not used.

RF I/F

Pin Name	Process When Pin Not Used	Comments
PLL_DATA	Open	
PLL_CLK	Open	
PLL_LE	Open	
PLL_OFF	Open	
PLL_POW	Open	
TX_POW	Open	
RX_POW	Open	
RSSI	Pull down or GND	
RSSI_CLK	Open	
PLL_PS	Open	
PLLLOCK	Pull down or GND	
RXC	Open	
TXC_IN	Pull down or GND	
TXCSEL	Pull down or GND	

Port I/F

Pin Name	Process When Pin Not Used	Comments
GPIO0	Pull up or V_{DD}	
GPIO1	Pull down or GND	
GPIO2/URXD	Pull down or GND	
GPIO3/UTXD	Pull up or V_{DD}	
GPIO4/SRDXCLK	Pull down or GND	
GPIO5/STDXCLK	Pull down or GND	
GPIO6/SRXD	Pull up or V_{DD}	
GPIO7/STXD	Pull up or V_{DD}	
GPIO8/RI	Pull up or V_{DD}	
GPIO9/DTR	Pull up or V_{DD}	
GPIO10/DSR	Pull down or GND	
GPIO11/CTS	Pull down or GND	
GPIO12/RTS	Pull up or V_{DD}	
GPIO13/DCD	Pull down or GND	
GPIO14/SIN	Pull up or V_{DD}	
GPIO15/SOUT	Pull up or V_{DD}	

[Note] These ports have multiple functions. When these ports are not used, they hold initial direction:input. So,these terminals need to be pullup or pulldown following the above table (not to be opened).

Memory I/F

Pin Name	Process When Pin Not Used	Comments
MA[19:0]	Open	When connected For 16-bit devices: • Open MA0. • Connect from MA1 in order from A0 of the connected device. For 8-bit devices: • Connect to each corresponding address.
MD[15:0]	Open	
$\overline{\text{MWE}}$	Open	
$\overline{\text{MRE}}$	Open	
$\overline{\text{MCS0}}$	Open	
$\overline{\text{MCS1}}$	Open	
$\overline{\text{MBS0}}$	Open	
$\overline{\text{MBS1}}$	Open	
$\overline{\text{MOE0}}$	Open	Only use when connecting to a device that has only one, but not both of $\overline{\text{MCS*}}$ or $\overline{\text{MRE}}$.
$\overline{\text{MOE1}}$	Open	

USB I/F

Pin Name	Process When Pin Not Used	Comments
D+	Open	
D–	Open	

JTAG I/F

Pin Name	Process When Pin Not Used	Comments
TDI	Open	
TDO	Open	
$\overline{\text{TRST}}$	Open	
TMS	Open	
TCK	Open	

PCM I/F

Pin Name	Process When Pin Not Used	Comments
PCMOUT	Open	
PCMIN	Open	
PCMSYNC	Open	
PCMCLK	Open	

Processes of Other Pins

TEST I/F, etc.

Pin Name	Process When Pin Not Used	Comments
TEST_L	Pull down or GND	
TEST_H	Pull up or V_{DD}	
TEST_PU	Open	
VTM	Open	
$\overline{\text{RESET}}$	Pull up or V_{DD}	
$\overline{\text{RESET\_OUT}}$	Open	
NC	Open	

- The unused pin configurations are subject to change according to the specific application. Please contact Oki Electric Industry Co., Ltd. for detailed board layout information.

ABOUT BLUETOOTH SOFTWARE

- At Oki Electric Industry Co., Ltd., we have made available as Pack 1 the software protocol stack of the lower layer up to HCI that conforms to the Bluetooth Specification Ver. 1.1 for external Flash memory and internal Flash memory.Pack 1 contents: Baseband Controller, LMP, HCI.

- Please contact Oki Electric Industry about upper software protocol stack above HCI.

- Please contact Oki Electric Industry Co., Ltd. for more information regarding software contents, pricing, etc.

VENDOR SPECIFICCOMMANDS

- Parameters can be set with the Pack 1 software by using the following Vendor Specific Commands.
- Please contact Oki Electric Industry Co., Ltd. for more information.

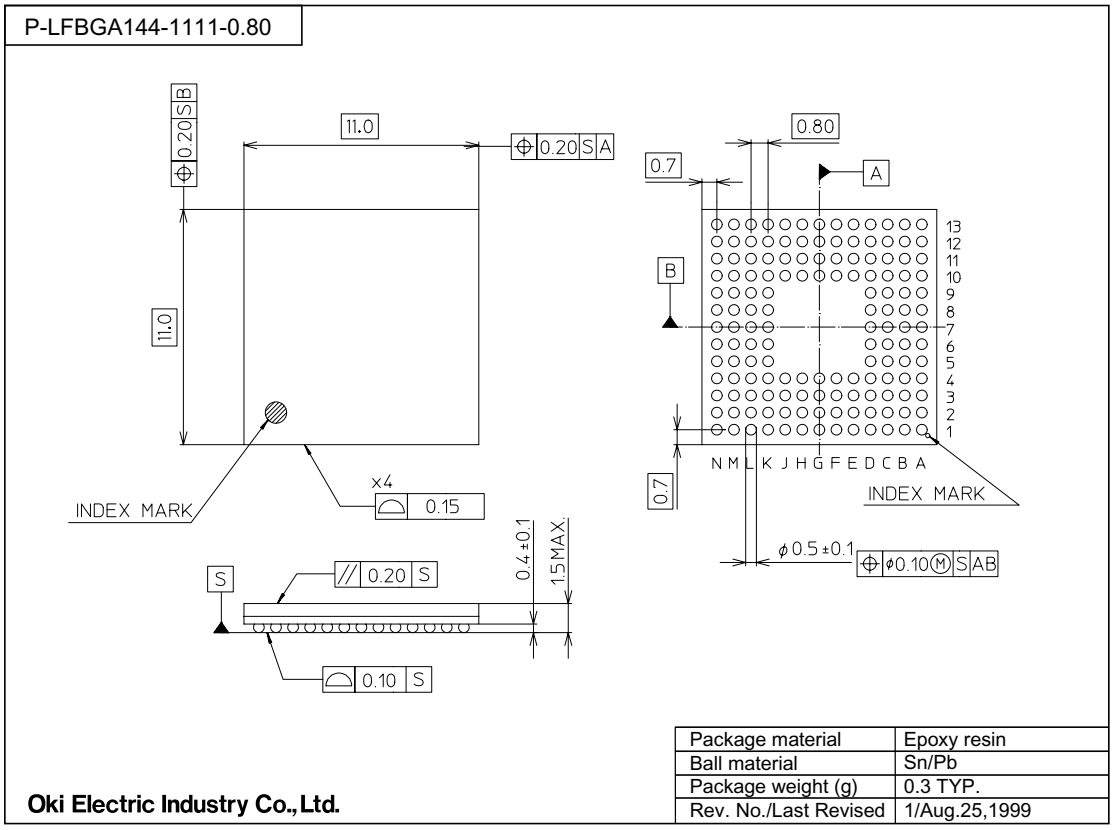
(Command example) HCI_VS_Set_LC_Parameters: Sets the link control information.

The following table shows the link control information that can be set.

Link Control Information	Comments
PCM for SCO Link	0: μ-law, 1: A-law, 2: Linear
UART baud rate	0: 9600 bps 1: 19.2 kbps 2: 38.4 kbps 3: 56 kbps 4: 115.2 kbps 5: 230.4 kbps 6: 345.6 kbps 7: 57.6 kbps 8: 460.8 kbps 9: 921.6 kbps
Poling rate	Unit: 625 μsec
Master clock setting for ML7050LA	12: 12 MHz 13: 13 MHz 16: 16 MHz

PACKAGE DIMENSIONS

(Unit: mm)



Caution regarding the installation of surface mounted type packages:

Surface mounted type packages are very susceptible to heat during reflow mounting and package moisture content when in storage. Therefore, please contact your Oki Electric Industry Co., Ltd. sales representative when considering reflow experiments and let us know the product name, package name, pin count, package code, the desired mounting conditions (reflow method, temperature, count), storage conditions, etc.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL70Q5110LA-01	Sep.2, 2002	–	–	Final edition 1

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