

## HEXFET® POWER MOSFET

## IRFNG50

### N-CHANNEL

#### 1000 Volt, 2.0Ω HEXFET

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry achieves very low on-state resistance combined with high transconductance.

HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

The Surface Mount Device (SMD-1) package represents another step in the continual evolution of surface mount technology. The SMD-1 will give designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the SMD-1 package to meet the specific needs of the power market by increasing the size of the termination pads, thereby enhancing thermal and electrical performance.

#### Product Summary

Part Number	BV <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
IRFNG50	1000V	2.0Ω	5.5A

#### Features:

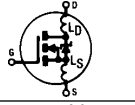
- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light-weight

#### Absolute Maximum Ratings

	Parameter	IRFNG50	Units
I <sub>D</sub> @ V <sub>GS</sub> = 10V, T <sub>C</sub> = 25°C	Continuous Drain Current	5.5	A
I <sub>D</sub> @ V <sub>GS</sub> = 10V, T <sub>C</sub> = 100°C	Continuous Drain Current	3.5	
I <sub>DM</sub>	Pulsed Drain Current ①	22	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	150	W
	Linear Derating Factor	1.2	W/K ⑤
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	860	mJ
I <sub>AR</sub>	Avalanche Current ①	5.5	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	15.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.0	V/ns
T <sub>J</sub>	Operating Junction	-55 to 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Package Mounting Surface Temperature	300 (for 5 seconds)	
	Weight	2.6 (typical)	g

## IRFNG50 Device

### Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	1000	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0 mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	1.4	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0 mA
RDS(on)	Static Drain-to-Source	—	—	2.0	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.5A
	On-State Resistance	—	—	2.25		
VGS(th)	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	5.2	—	—	S (r)	V <sub>DS</sub> > 15V, I <sub>DS</sub> = 3.5A ④
IDSS	Zero Gate Voltage Drain Current	—	—	25	μA	V <sub>DS</sub> = 0.8 x Max Rating, V <sub>GS</sub> = 0V
		—	—	250		
IGSS	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
IGSS	Gate-to-Source Leakage Reverse	—	—	-100	nA	V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	87	—	200	nC	V <sub>GS</sub> = 10V, I <sub>D</sub> = 5.5A V <sub>DS</sub> = Max. Rating x 0.5 see figures 6 and 13
Q <sub>gs</sub>	Gate-to-Source Charge	8.7	—	20		
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	49	—	110		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	30	ns	V <sub>DD</sub> = 500V, I <sub>D</sub> = 5.5A, R <sub>G</sub> = 2.35Ω, V <sub>GS</sub> = 10V  see figure 10
t <sub>r</sub>	Rise Time	—	—	44		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	210		
t <sub>f</sub>	Fall Time	—	—	60		
LD	Internal Drain Inductance	—	2.0	—	nH	<p>Measured from the drain lead, 6mm (0.25 in.) from package to center of die.</p> <p>Modified MOSFET symbol showing the internal inductances.</p> 
LS	Internal Source Inductance	—	6.5	—		
C <sub>iss</sub>	Input Capacitance	—	2400	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0 MHz see figure 5
C <sub>oss</sub>	Output Capacitance	—	240	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	80	—		

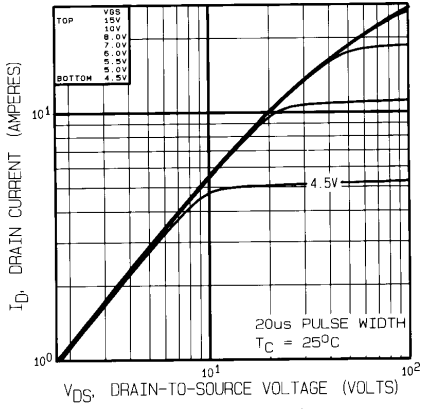
### Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	22		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.8	V	T <sub>j</sub> = 25°C, I <sub>S</sub> = 5.5A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	1200	ns	T <sub>j</sub> = 25°C, I <sub>F</sub> = 5.5A, di/dt ≤ 100A/μs
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	8.4	μC	V <sub>DD</sub> ≤ 50V ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

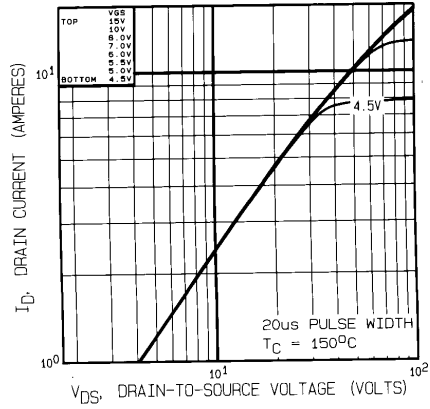
### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	0.83	K/W	Soldered to a copper clad PC board
R <sub>thJPCB</sub>	Junction-to-PC Board	—	TBD	—		

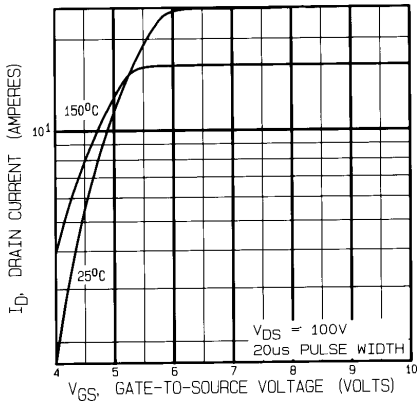
# IRFNG50 Device



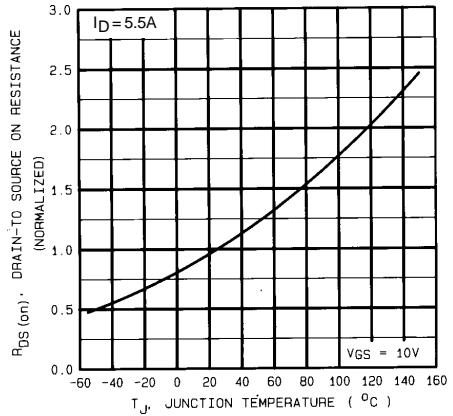
**Fig. 1 — Typical Output Characteristics**  
 $T_C = 25^\circ\text{C}$



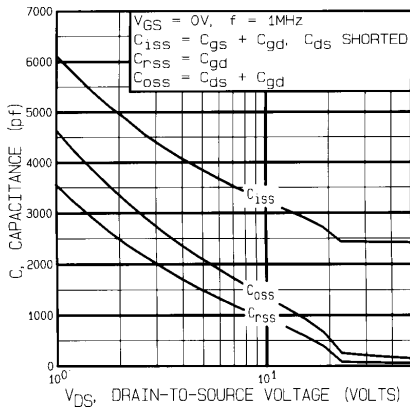
**Fig. 2 — Typical Output Characteristics**  
 $T_C = 150^\circ\text{C}$



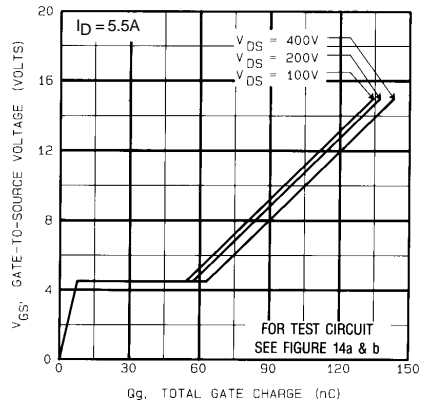
**Fig. 3 — Typical Transfer Characteristics**



**Fig. 4 — Normalized On-Resistance Vs. Temperature**

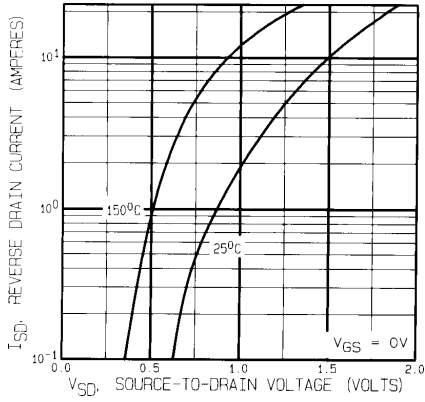


**Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage**

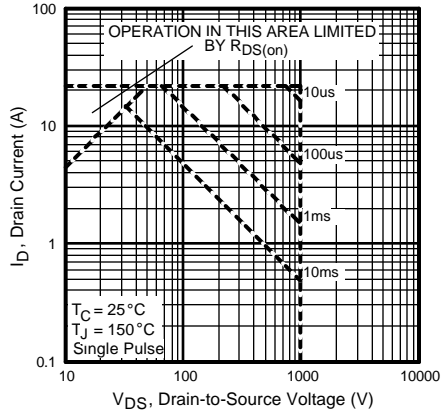


**Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage**

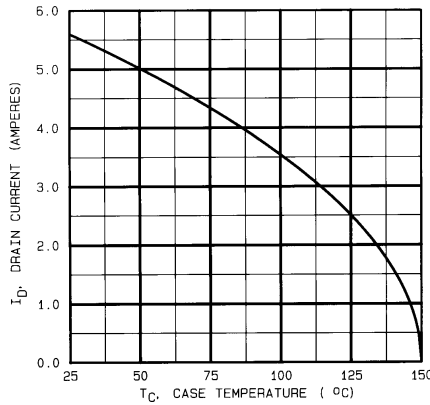
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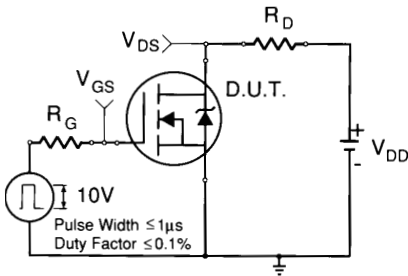
**Fig. 7 — Typical Source-to-Drain Diode Forward Voltage**



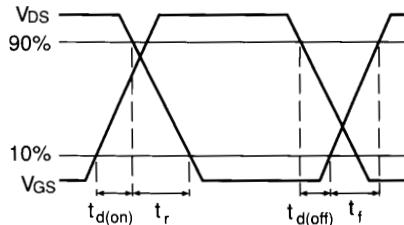
**Fig. 8 — Maximum Safe Operating Area**



**Fig. 9 — Maximum Drain Current Vs. Case Temperature**

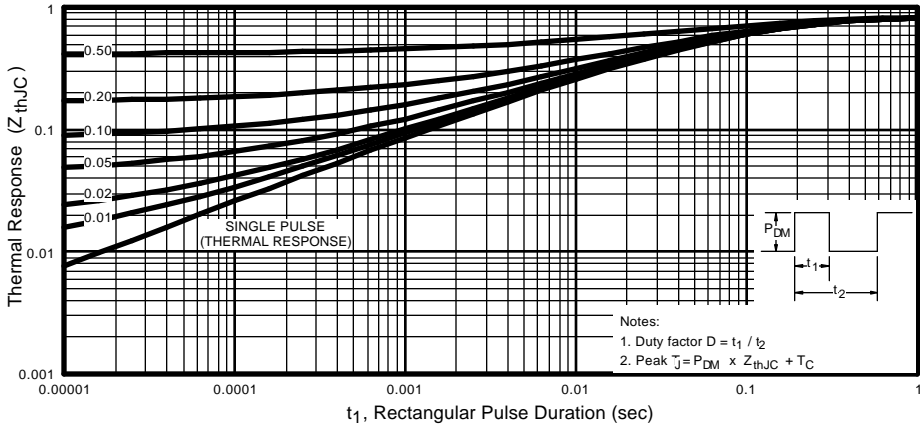


**Fig. 10a — Switching Time Test Circuit**

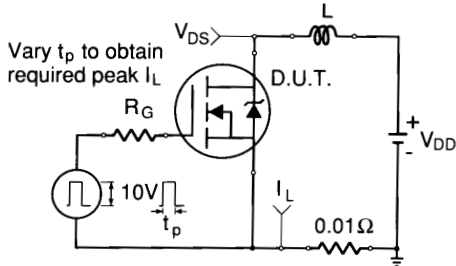


**Fig. 10b — Switching Time Waveforms**

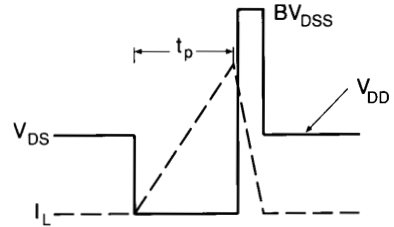
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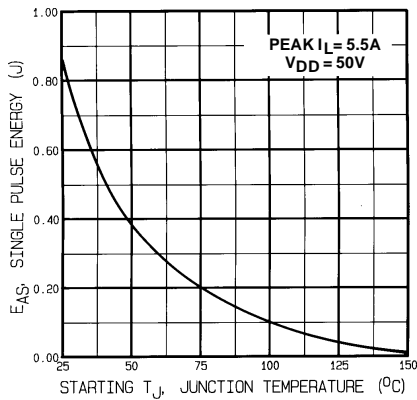
**Fig. 11 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration**



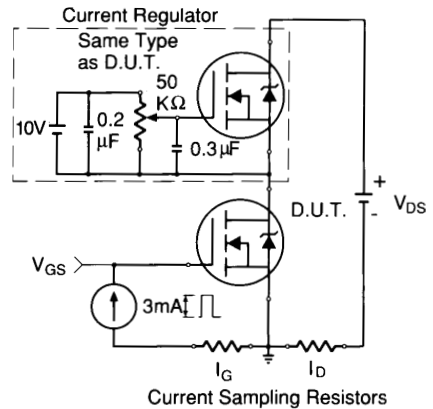
**Fig. 12a — Unclamped Inductive Test Circuit**



**Fig. 12b — Unclamped Inductive Waveforms**



**Fig. 12c — Max. Avalanche Energy vs. Current**



**Fig. 13a — Gate Charge Test Circuit**

# IRFNG50 Device

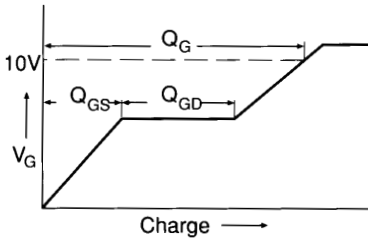
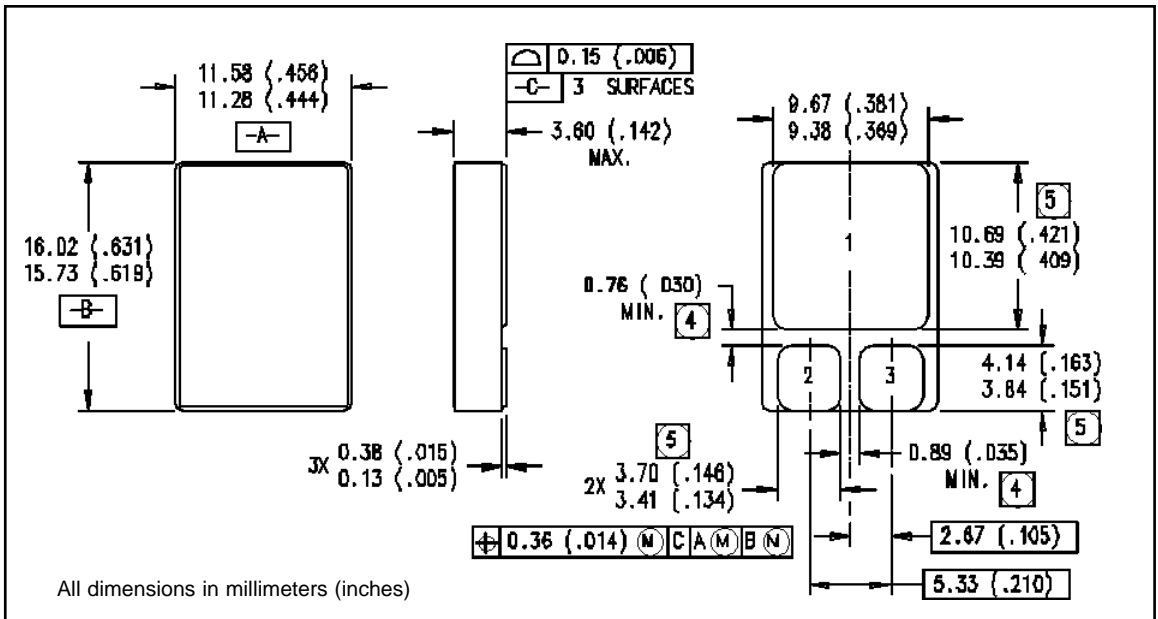


Fig. 13b — Basic Gate Charge Waveform

- ① Repetitive Rating; Pulse width limited by maximum junction temperature. (see figure 11)
- ② @  $V_{DD} = 50V$ , Starting  $T_J = 25^\circ C$ ,  
 $EAS = [0.5 * L * (I_L^2) * [BV_{DSS}/(BV_{DSS}-V_{DD})]$   
 Peak  $I_L = 5.5A$ ,  $V_{GS} = 10V$ ,  $25 \leq R_G \leq 200\Omega$
- ③  $I_{SD} \leq 5.5A$ ,  $di/dt \leq 120A/\mu s$ ,  
 $V_{DD} \leq BV_{DSS}$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤  $K/W = ^\circ C/W$   
 $W/K = W/^\circ C$

## Case Outline and Dimensions — SMD-1



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