

# FQG4904

## 400V Dual N & P-Channel MOSFET

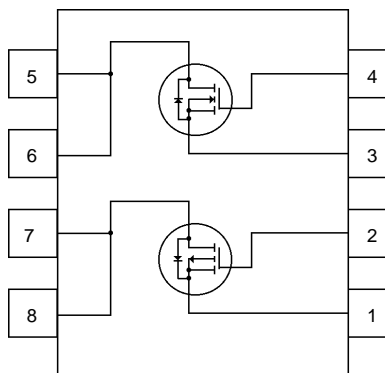
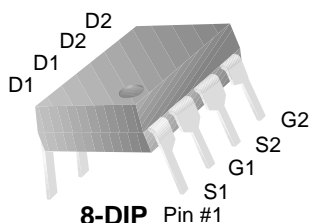
### General Description

These dual N and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on half bridge.

### Features

- N-Channel 0.46A, 400V,  $R_{DS(on)} = 3.0 \Omega @ V_{GS} = 10 V$   
P-Channel -0.46A, -400V,  $R_{DS(on)} = 3.0 \Omega @ V_{GS} = -10 V$
- Low gate charge ( typical N-Channel 7.6 nC)  
( typical P-Channel 20.0 nC)
- Fast switching
- Improved dv/dt capability



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
$V_{DSS}$	Drain-Source Voltage	400	-400	V
$I_D$	Drain Current - Continuous ( $T_A = 25^\circ\text{C}$ ) - Continuous ( $T_A = 100^\circ\text{C}$ )	0.46	-0.46	A
		0.29	-0.29	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	3.68	-3.68	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
dv/dt	Peak Diode Recovery dv/dt (Note 2)	4.5	-4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	1.6		W
		0.013		W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 5a)	--	78	$^\circ\text{C/W}$

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Off Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	400	--	--	V
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-400	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	N-Ch	--	0.47	--	$\text{V}/^\circ\text{C}$
		$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	P-Ch	--	-0.3	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	N-Ch	--	--	10	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, T_A = 125^\circ\text{C}$		--	--	100	$\mu\text{A}$
		$V_{DS} = -400\text{ V}, V_{GS} = 0\text{ V}$	P-Ch	--	--	-10	$\mu\text{A}$
		$V_{DS} = -320\text{ V}, T_A = 125^\circ\text{C}$		--	--	-100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	All	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	All	--	--	-100	nA

## On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	2.0	--	4.0	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.23\text{ A}$	N-Ch	--	2.0	3.0	$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -0.23\text{ A}$	P-Ch	--	2.2	3.0	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 0.23\text{ A}$	N-Ch	--	0.8	--	S
		$V_{DS} = -40\text{ V}, I_D = -0.23\text{ A}$	P-Ch	--	1.1	--	S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	N-Channel $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$	N-Ch	--	235	300	pF
			P-Ch	--	500	645	pF
$C_{oss}$	Output Capacitance	f = 1.0 MHz P-Channel	N-Ch	--	40	55	pF
			P-Ch	--	85	110	pF
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}$ , f = 1.0 MHz	N-Ch	--	6.5	8.5	pF
			P-Ch	--	14	18.5	pF

## Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	N-Channel $V_{DD} = 200\text{ V}, I_D = 0.46\text{ A}$ , $R_G = 25\ \Omega$	N-Ch	--	6.5	25	ns
			P-Ch	--	10	30	ns
$t_r$	Turn-On Rise Time	P-Channel $V_{DD} = -200\text{ V}, I_D = -0.46\text{ A}$ , $R_G = 25\ \Omega$	N-Ch	--	16	40	ns
			P-Ch	--	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time	N-Channel $V_{DD} = 200\text{ V}, I_D = 0.46\text{ A}$ , $R_G = 25\ \Omega$	N-Ch	--	28	65	ns
			P-Ch	--	85	180	ns
$t_f$	Turn-Off Fall Time	P-Channel $V_{DD} = -200\text{ V}, I_D = -0.46\text{ A}$ , $R_G = 25\ \Omega$	N-Ch	--	34	80	ns
			P-Ch	--	56	120	ns
$Q_g$	Total Gate Charge	N-Channel $V_{DS} = 320\text{ V}, I_D = 0.46\text{ A}$ , $V_{GS} = 10\text{ V}$	N-Ch	--	7.6	10	nC
			P-Ch	--	20	26	nC
$Q_{gs}$	Gate-Source Charge	P-Channel $V_{DS} = -320\text{ V}, I_D = -0.46\text{ A}$ , $V_{GS} = -10\text{ V}$	N-Ch	--	1.2	--	nC
			P-Ch	--	2.7	--	nC
$Q_{gd}$	Gate-Drain Charge	N-Channel $V_{DS} = 320\text{ V}, I_D = 0.46\text{ A}$ , $V_{GS} = 10\text{ V}$	N-Ch	--	3.3	--	nC
			P-Ch	--	9.9	--	nC

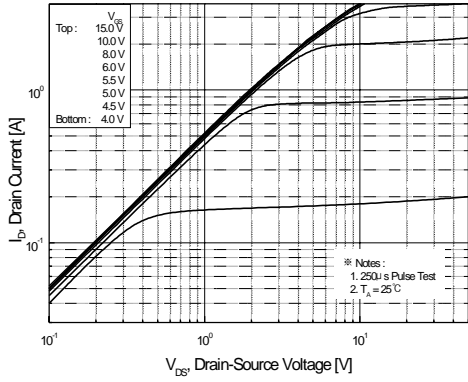
## Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>							
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		N-Ch	--	--	0.46	A
			P-Ch	--	--	-0.46	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		N-Ch	--	--	3.68	A
			P-Ch	--	--	-3.68	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.46\text{ A}$	N-Ch	--	--	1.4	V
		$V_{GS} = 0\text{ V}, I_S = -0.46\text{ A}$	P-Ch	--	--	-5.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 0.46\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 3)	N-Ch	--	104	--	ns
$Q_{rr}$	Reverse Recovery Charge			--	248	--	nC
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -0.46\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 3)	P-Ch	--	117	--	ns
$Q_{rr}$	Reverse Recovery Charge			--	497	--	nC

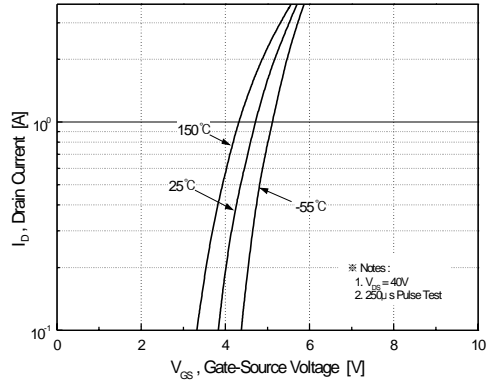
**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $I_{SD} \leq 0.46\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
3. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature
5.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance.  $R_{\theta CA}$  is determined by the user's board design  
Maximum  $R_{\theta JA}$  using the different board layouts on 3"x4.5" FR-4 PCB in a still air environment :
  - a.  $78^\circ\text{C}/\text{W}$  when mounted without any pad copper
  - b.  $60^\circ\text{C}/\text{W}$  when mounted on a  $4.5\text{ in}^2$  pad of 2oz copper. In such an environment, the power dissipation can be enhanced up to 2.1W

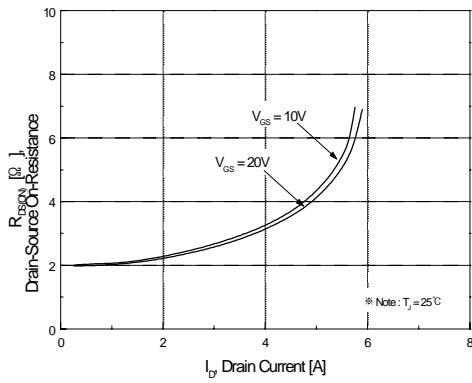
**Typical Characteristics : N-Channel**



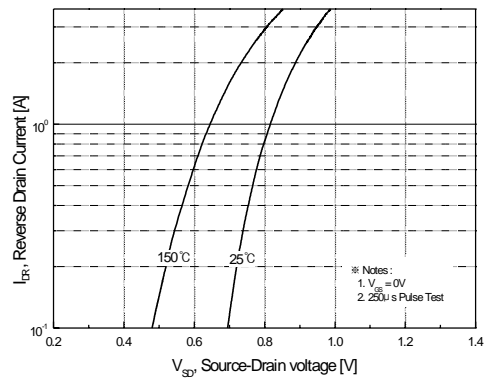
**Figure 1. On-Region Characteristics**



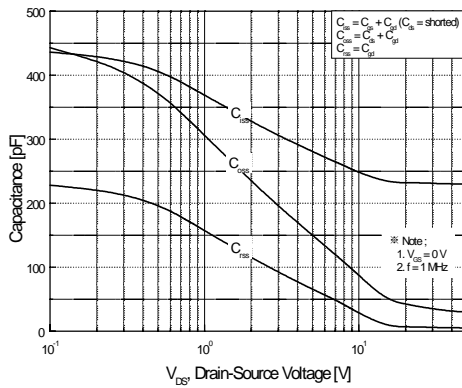
**Figure 2. Transfer Characteristics**



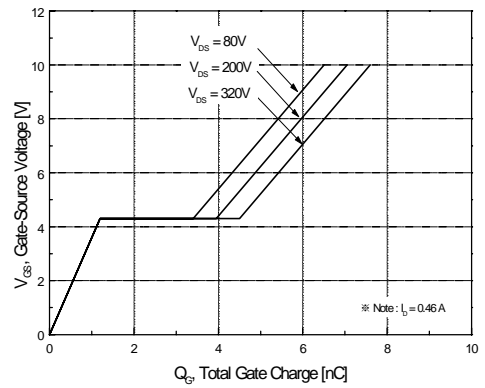
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

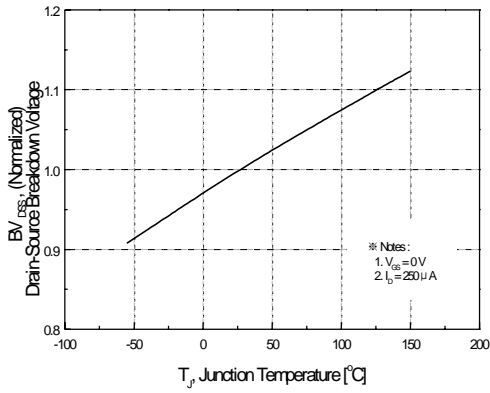


**Figure 5. Capacitance Characteristics**

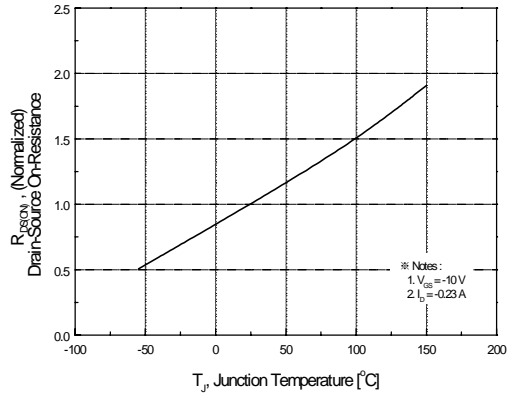


**Figure 6. Gate Charge Characteristics**

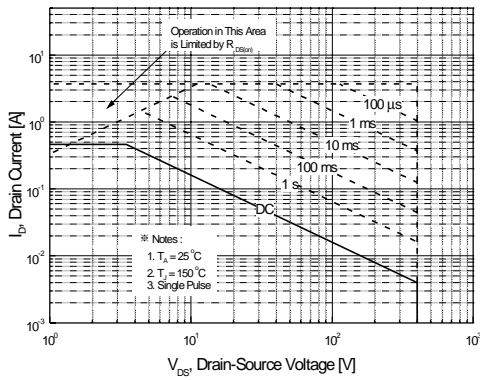
**Typical Characteristics : N-Channel** (Continued)



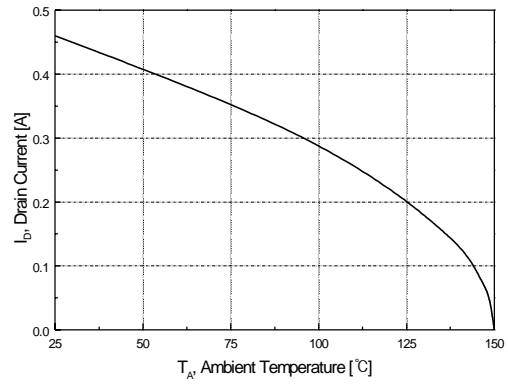
**Figure 7. Breakdown Voltage Variation vs. Temperature**



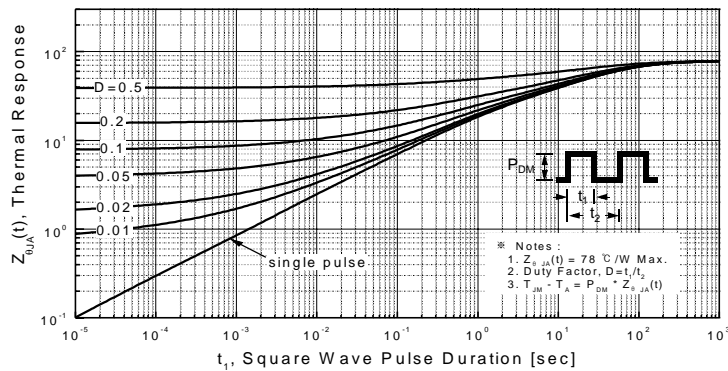
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Ambient Temperature**



**Figure 11. Transient Thermal Response Curve**

Typical Characteristics : P-Channel

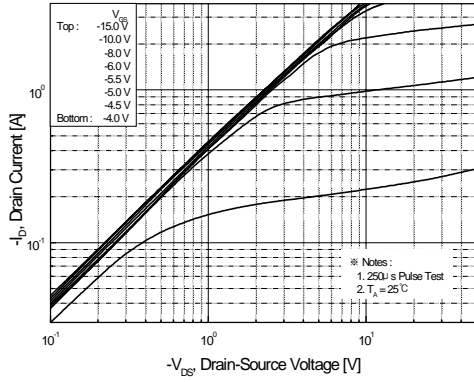


Figure 1. On-Region Characteristics

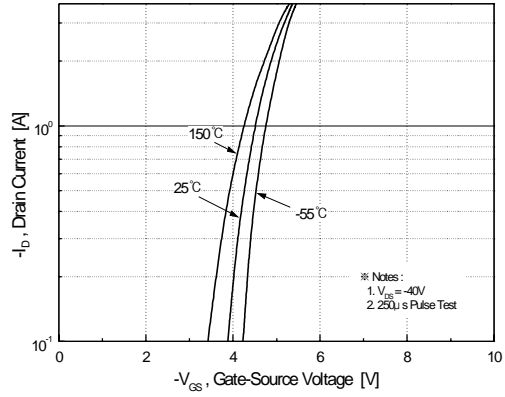


Figure 2. Transfer Characteristics

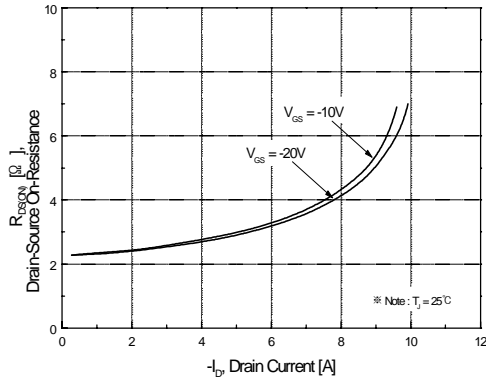


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

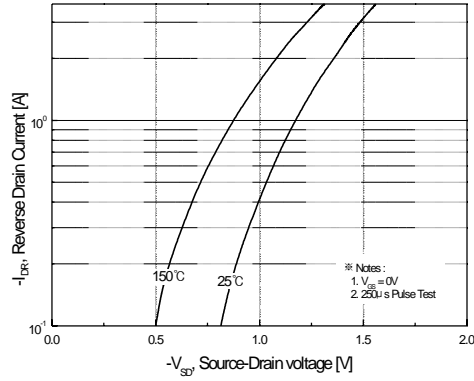


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

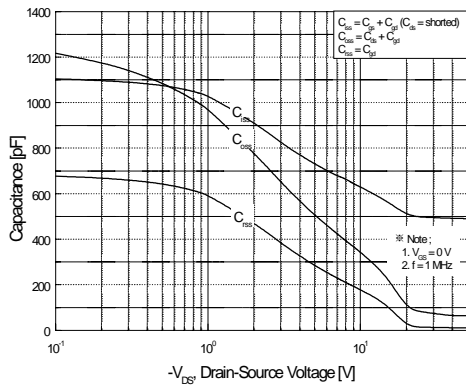


Figure 5. Capacitance Characteristics

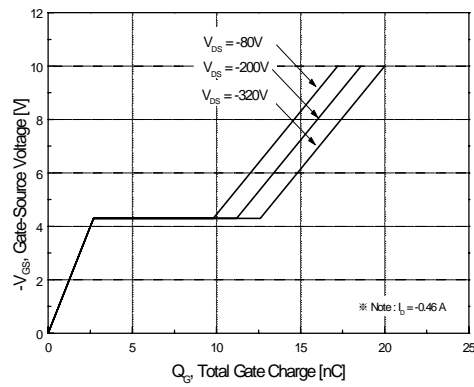


Figure 6. Gate Charge Characteristics

Typical Characteristics : P-Channel (Continued)

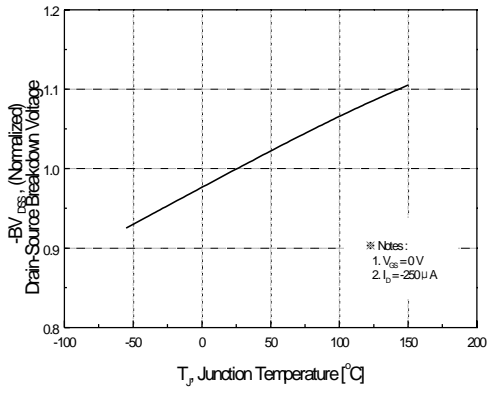


Figure 7. Breakdown Voltage Variation vs. Temperature

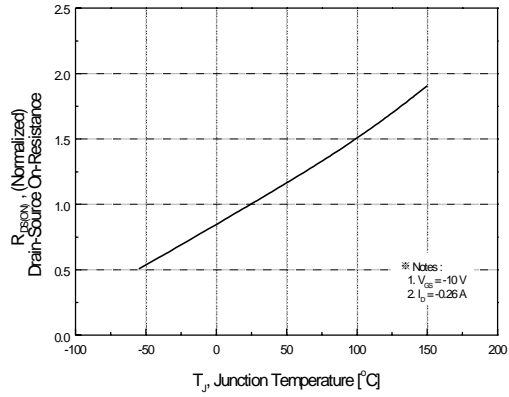


Figure 8. On-Resistance Variation vs. Temperature

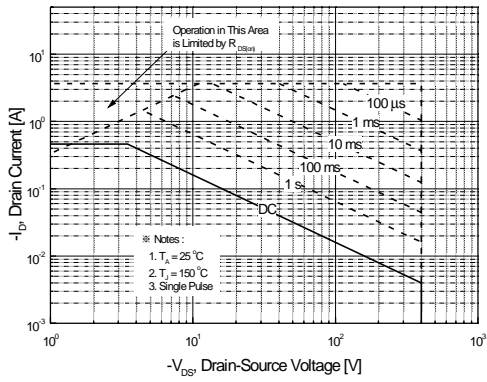


Figure 9. Maximum Safe Operating Area

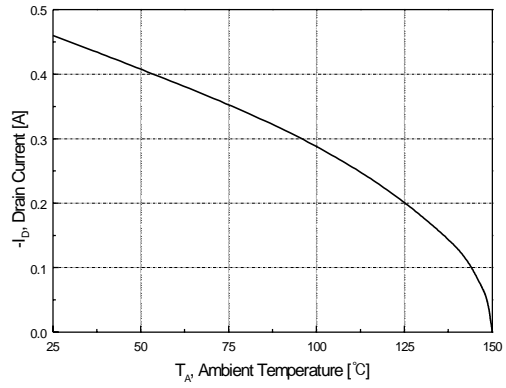


Figure 10. Maximum Drain Current vs. Ambient Temperature

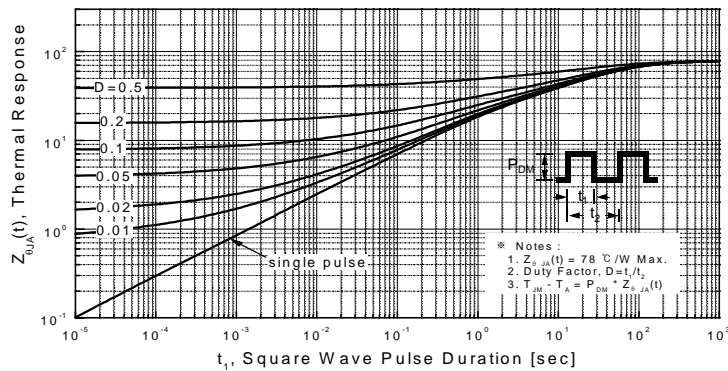
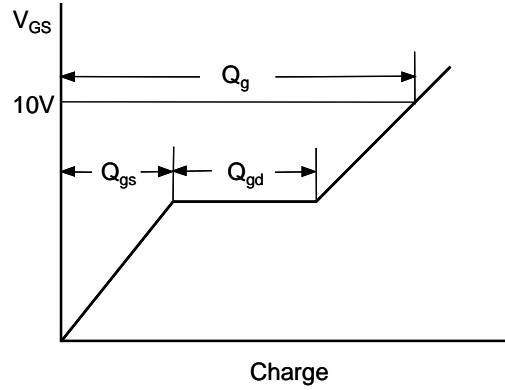
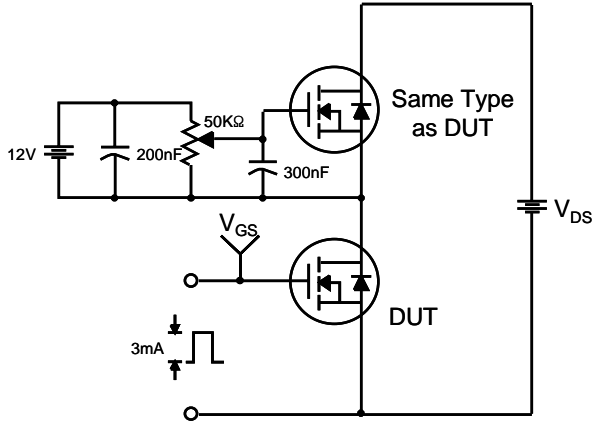
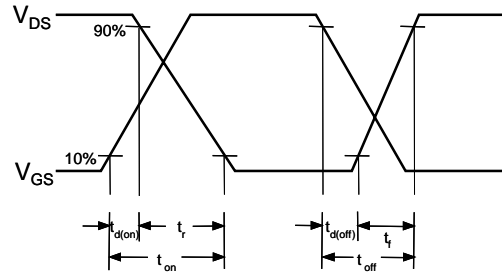
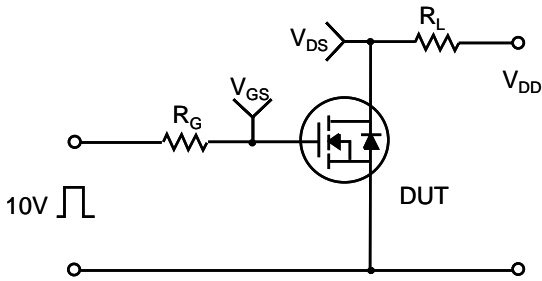


Figure 11. Transient Thermal Response Curve

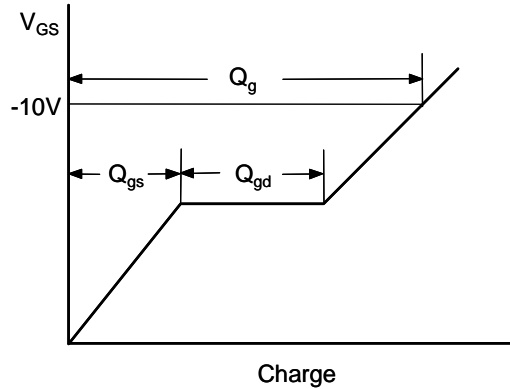
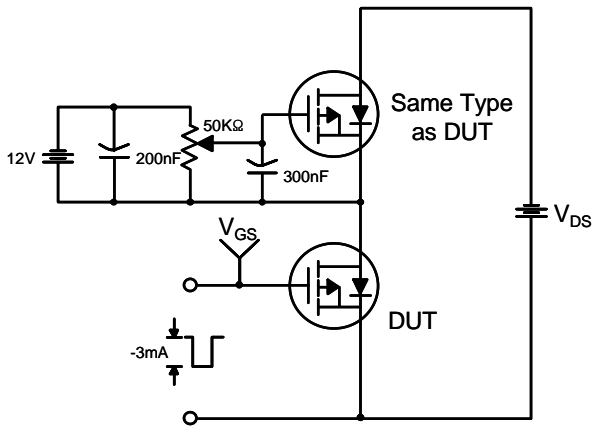
**Gate Charge Test Circuit & Waveform (N-Channel)**



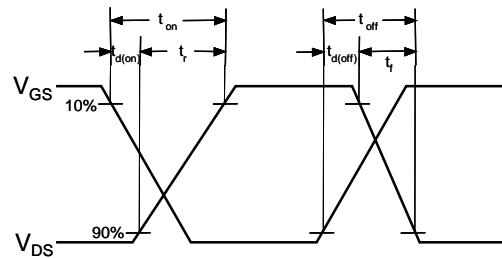
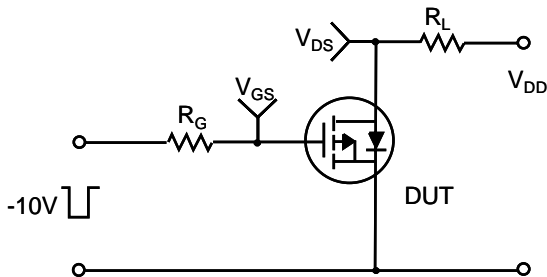
**Resistive Switching Test Circuit & Waveforms (N-Channel)**



**Gate Charge Test Circuit & Waveform (P-Channel)**

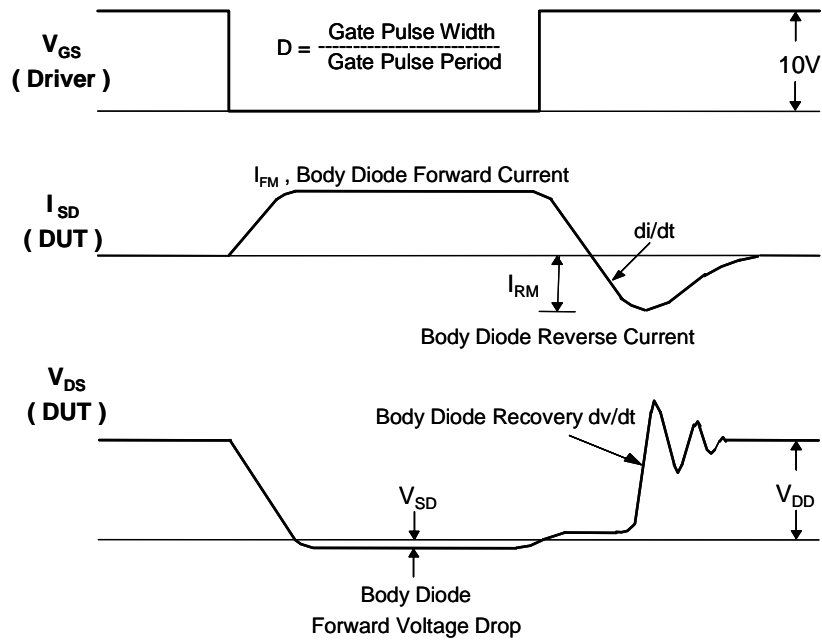
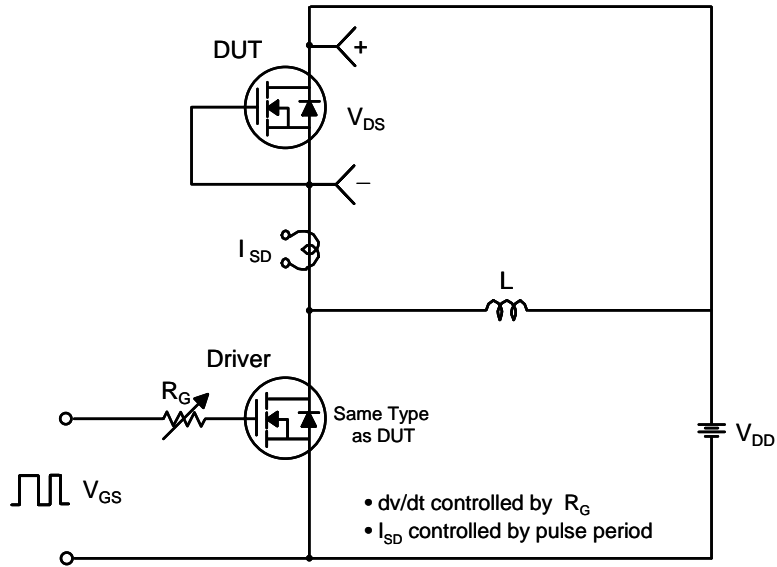


**Resistive Switching Test Circuit & Waveforms (P-Channel)**





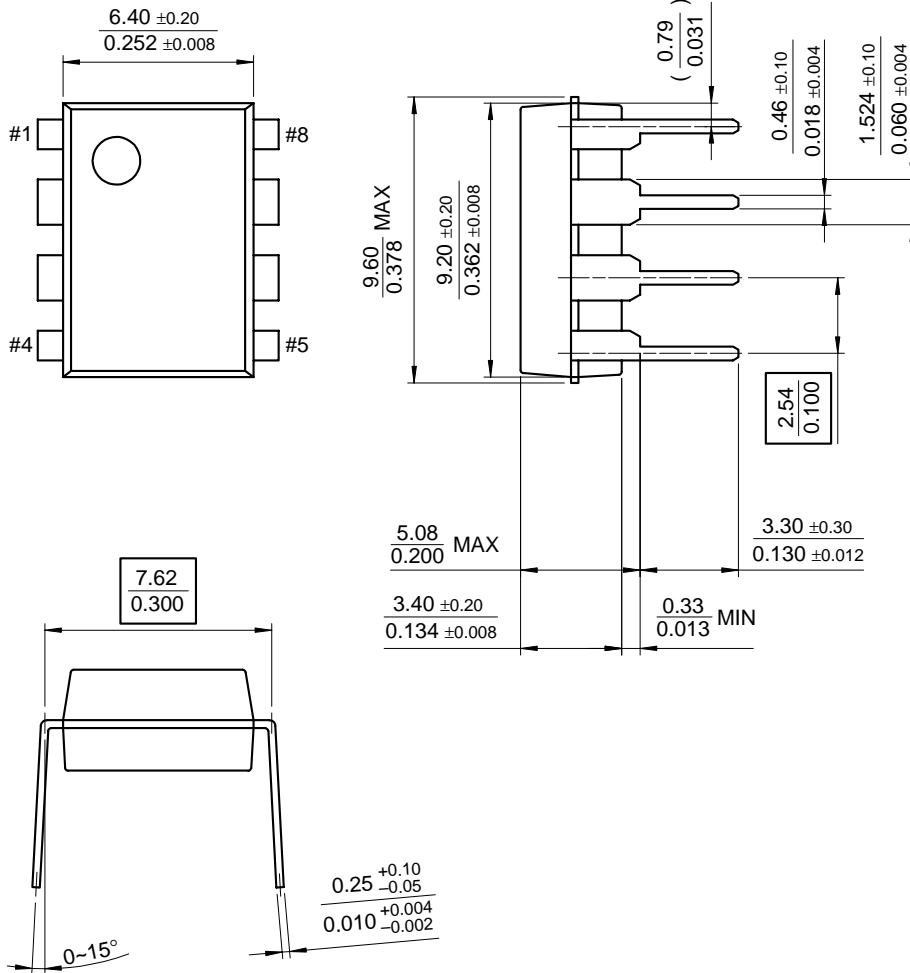
Peak Diode Recovery dv/dt Test Circuit & Waveforms (N-Channel)





Package Dimensions

8-DIP



Dimensions in Millimeters

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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