ACT–E128K32 High Speed 4 Megabit EEPROM Multichip Module

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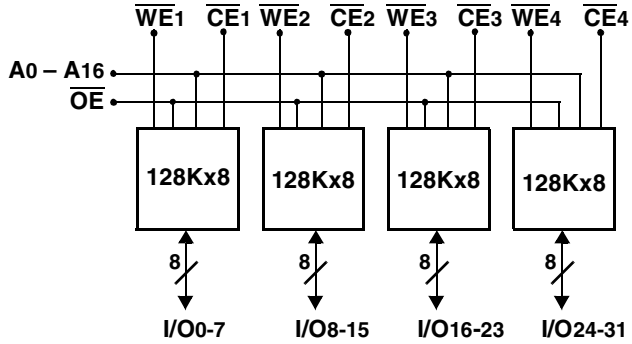
Features

- 4 Low Power 128K x 8 EEPROM Die in One MCM Package
- Organized as 128K x 32
  - User Configurable to 256K x 16 or 512K x 8
- CMOS and TTL Compatible Inputs and Outputs
- Access Times of 120, 140, 150, 200, 250 & 300ns
- +5V ±10% Supply
- Automatic Page Write Operation
- Page Write Cycle Time: 10ms Max
- Data Retention Ten Years Minimum
- Low Power CMOS
- Data Polling for End of Write Detection
- Industry Standard Pinouts
- Packaging – Hermetic Ceramic
  - 66 Pin, 1.08" x 1.08" x .160" PGA Type, No Shoulder, Aeroflex code# "P3"
  - 66 Pin, 1.08" x 1.08" x .185" PGA Type, With Shoulder, Aeroflex code# "P7"
  - 68 Lead, .88" x .88" x .200" Dual-Cavity Small Outline Gull Wing, Aeroflex code# "F2" *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
- MIL-PRF-38534 Compliant MCMs Available
- Hardware and Software Data Protection
- Internal Decoupling Capacitors for Low Noise Operation
- Commercial, Industrial and Military Temperature Ranges
- SMD# 5962–94585 Released (P7 & F2)

Block Diagram – PGA Type Package (P3,P7) & CQFP (F2)



Pin Description

I/O0-31	Data I/O
A0–16	Address Inputs
$\overline{WE}$1-4	Write Enables
$\overline{OE}$	Output Enable
$\overline{CE}$1-4	Chip Enables
Vcc	Power Supply
GND	Ground

General Description

The ACT–E128K32 is a high speed, 4 megabit, CMOS EEPROM multichip module (MCM) designed for full temperature range military, space, or high reliability applications. The MCM can be organized as a 256K x 16 bits or 512K x 8 bits device and is input and output CMOS and TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low and output enable ($\overline{OE}$) is high. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are both low. Access times grades of 120, 140, 150, 200, 250 & 300ns are standard.

The ACT–E128K32 is packaged in a choice of hermetically sealed co-fired ceramic packages, a 66 pin, 1.08" sq PGA or a 68 lead, .88" sq gullwing CQFP. The device operates over the temperature range of -55°C to +125°C and military environment.

Absolute Maximum Ratings

Parameter	Symbol	Range	Units
Operating Temperature	T_C	-55 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
All Input Voltages with respect to Ground	V_G	-0.6 to +6.25	V
All Output Voltages with respect to Ground	-	-0.6 to V_{CC}+0.6	V
Voltage on $\overline{OE}$ and A9 with respect to Ground	-	-0.6 to +13.5	V

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.0	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V
T_C	Case Operating Temperature (Military)	-55	+125	°C

Capacitance

(V_{IN} = 0V, f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A_0 – A_{16} Capacitance	50	pF
C_{OE}	Output Enable Capacitance	50	pF
$C_{WE(1-4)}$	Write Enable Capacitance	20	pF
$C_{CE(1-4)}$	Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O0 – I/O31 Capacitance	20	pF

DC Characteristics

(V_{CC} = 5.0V, Vss = 0V, T_C = -55°C to +125°C, unless otherwise specified)

Parameter	Sym	Conditions	Minimum	Maximum	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	I_{CCx32}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5Mhz		250	mA
Operating Supply Current	I_{SB}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5Mhz		5	mA
Output Low Voltage	V_{OL}	I_{OL} = +2.1mA, V_{CC} = 4.5V		0.45	V
Output High Voltage	V_{OH}	I_{OH} = –400µA, V_{CC} = 4.5V	2.4		V

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z
X	X	H	Write Inhibit	-
X	L	X		-

AC Write Characteristics

(V_{CC} = 5V, V_{SS} = 0V, T_C = -55°C to +125°C)

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{WC}		10	ms
Address Set-up Time	t_{AS}	10		ns
Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	t_{WP}	150		ns
Chip Enable Set-up Time	t_{CE}	0		ns
Address Hold Time	t_{AH}	100		ns
Data Hold Time	t_{DH}	10		ns
Chip Enable Hold Time	t_{CEH}	0		ns
Data Set-up Time	t_{DS}	100		ns
Output Enable Set-up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns

AC Read Characteristics

(V_{CC} = 5V, V_{SS} = 0V, T_C = -55°C to +125°C)

Read Cycle Parameter	Symbol	–120		–140		–150		–200		–250		–300		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		140		150		200		250		300		ns
Address Access Time	t_{ACC}		120		140		150		200		250		300	ns
Chip Enable Access Time	t_{ACE}		120		140		150		200		250		300	ns
Output Hold From Address Change, $\overline{OE}$ or $\overline{CE}$	t_{OH}	0		0		0		0		0		0		ns
Output Enable to Output Valid	t_{OE}	0	55	0	55	0	55	0	55	0	85	0	85	ns
Chip Enable or $\overline{OE}$ to High Z Output	t_{DF}		70		70		70		70		70		70	ns

Page Write Characteristics

(V_{CC} = 5V, V_{SS} = 0V, T_C = -55°C to +125°C)

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t_{WC}		10	ms
Address Set-up Time	t_{AS}	10		ns
Address Hold Time , See Note 1	t_{AH}	100		ns
Data Set-up Time	t_{DS}	100		ns
Data Hold Time	t_{DH}	10		ns
Write Pulse Width	t_{WP}	150		ns
Byte Load Cycle Time	t_{BLC}		150	µs
Write Pulse Width High	t_{WPH}	50		ns

Note 1 – Page Address must remain valid for duration of write cycle.

Device Operation

The ACT-E128K32 is a high-performance Electrically Erasable and Programmable Read Only Memory. It is composed of four 1 megabit memory chips and is organized as 131,072 by 32 bits. The device offers access times of 120 to 300ns with power dissipation of 1.375W. When the device is deselected, the CMOS standby current is less than 5 mA.

The ACT-E128K32 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Aeroflex's ACT-E128K32 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

WRITE

A write cycle is initiated when $\overline{OE}$ is high and a low pulse is on $\overline{WE}$ or $\overline{CE}$ with $\overline{CE}$ or $\overline{WE}$ low. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever occurs last. The data is latched by the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 2 and 3 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip enable. Chip enable is accomplished by placing the $\overline{CE}$ line low. Write enable consists of setting the $\overline{WE}$ line low. The write cycle begins when the last of either $\overline{CE}$ or $\overline{WE}$ goes low.

The $\overline{WE}$ line transition from high to low also initiates an internal delay timer to permit page mode operation. Each subsequent $\overline{WE}$ transition from high to low that occurs before the completion of the t_{BLC} time out will restart the timer from zero. The operation of the timer is the same as a retriggable one-shot.

READ

The ACT-E128K32 stores data at the memory location determined by the address pins. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, this data is present on the outputs. When $\overline{CE}$ and $\overline{OE}$ are high, the outputs are in a high impedance state. This two line control prevents bus contention.

$\overline{DATA}$ POLLING

The ACT-E128K32 offers a data polling feature which allows a faster method of writing to the device. Figure 5 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on I/O7 (For each Chip). Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

PAGE WRITE OPERATION

The ACT-E128K32 has a page write operation that allows one to 128 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within t_{BLC} or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the t_{BLC} time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by Aeroflex Microelectronics, the ACT-E128K32 has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K byte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the ACT-E128K32. These are included to improve reliability during normal operation:

A) Vcc Sense
While below 3.8V typical write cycles are inhibited.

B) Write inhibiting
Holding $\overline{OE}$ low and either $\overline{CE}$ or $\overline{WE}$ high inhibits write cycles.

C) Noise filter
Pulses of <10ns (TYP) on $\overline{WE}$ or $\overline{CE}$ will not initiate a write cycle.

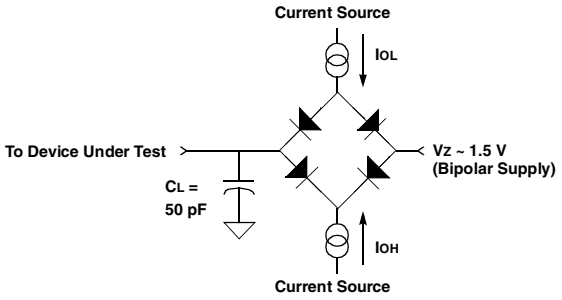
$\overline{\text{Data}}$ Polling Characteristics

(V_{CC} = 5V, V_{SS} = 0V, T_C = -55°C to +125°C)

Parameter	Symbol	Min	Max	Units
Data Hold Time	t_{DH}	10		ns
$\overline{OE}$ Hold Time	t_{OEH}	10		ns
$\overline{OE}$ to Output Valid	t_{OE}		55	ns
Write Recovery Time	t_{WR}	0		ns

Guaranteed. But not tested.

Figure 1
AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V
Output Lead Capacitance	50	pF

Notes:
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance Z_O = 75Ω. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Figure 2
Write Waveforms – $\overline{WE}$ Controlled

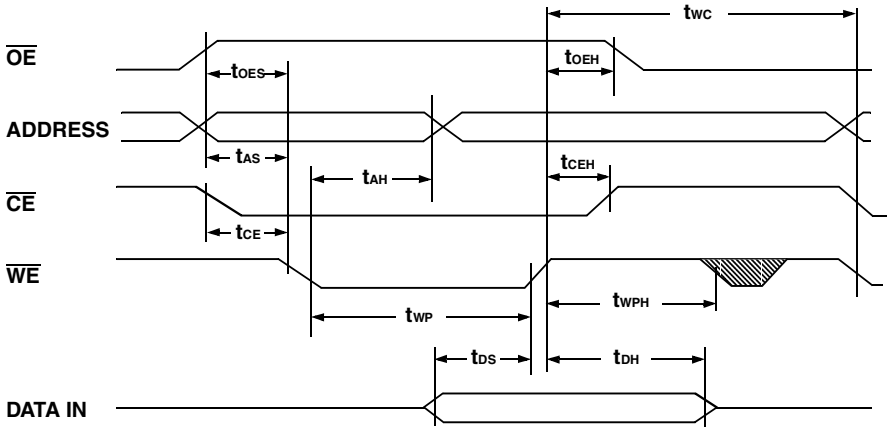


Figure 3
Write Waveforms – $\overline{CE}$ Controlled

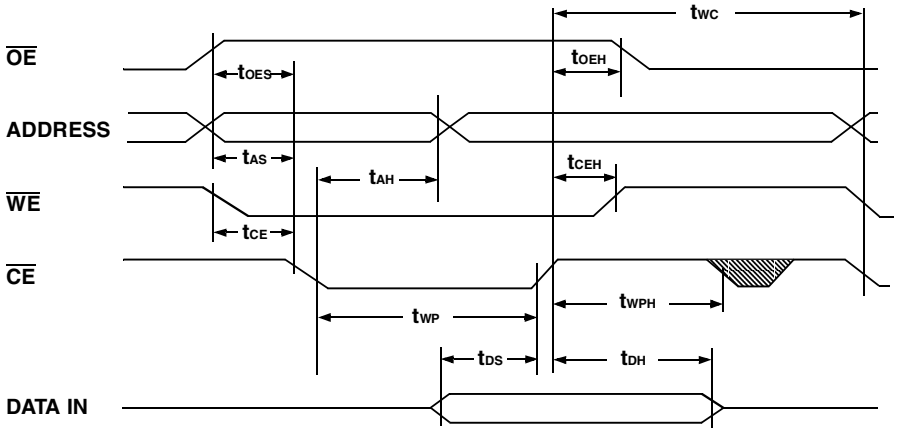
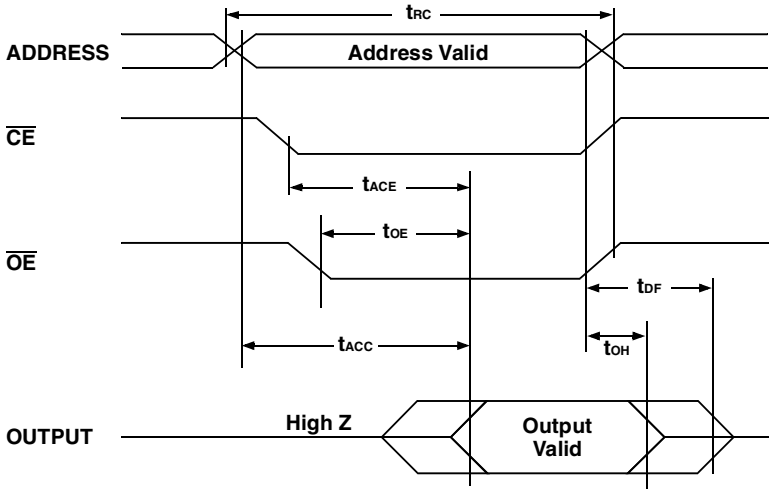


Figure 4
Read Waveforms



Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACS} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{OE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.

Figure 5
Data Polling Waveform

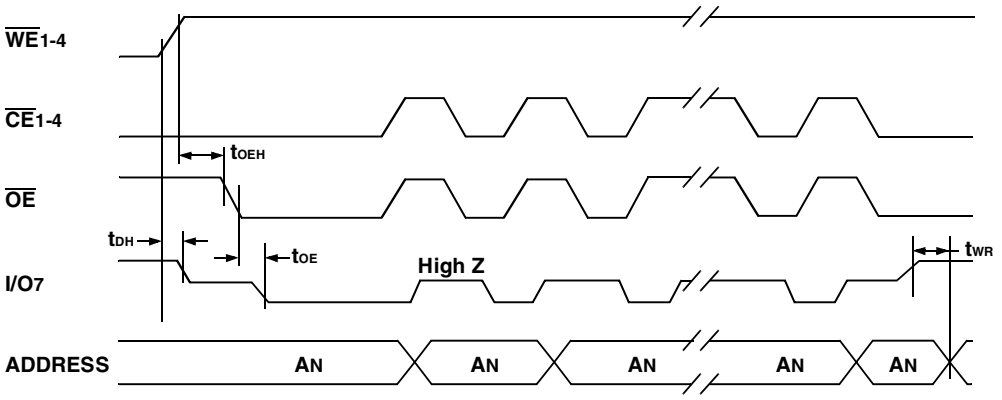
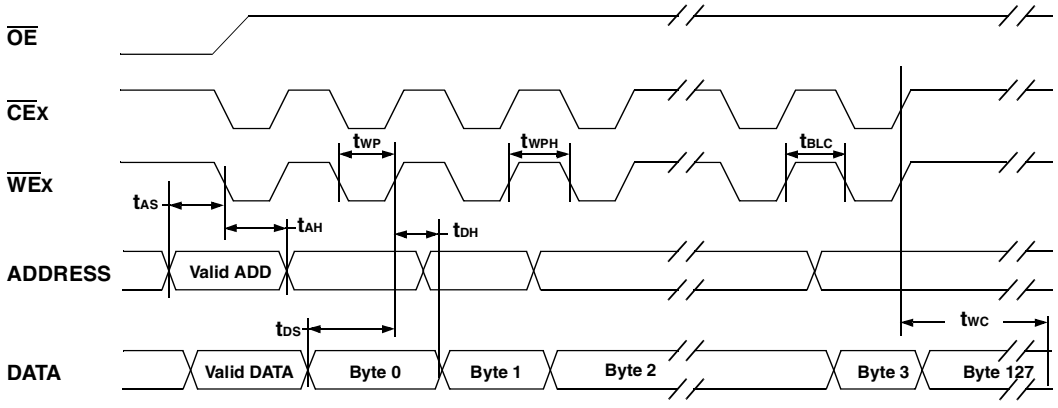


Figure 6
Page Mode Write Waveforms



Notes:
1. A7 through A16 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software codes have been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.

Figure 7
Software Data
Protection Enable Algorithm (1)

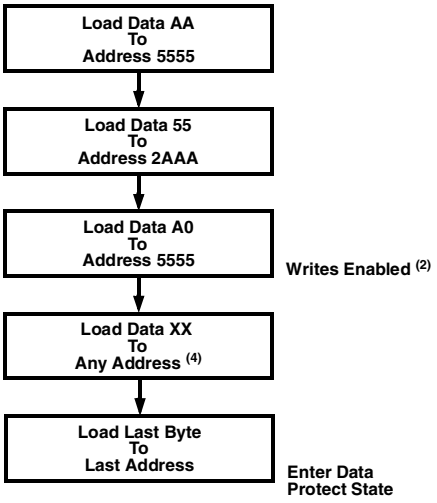
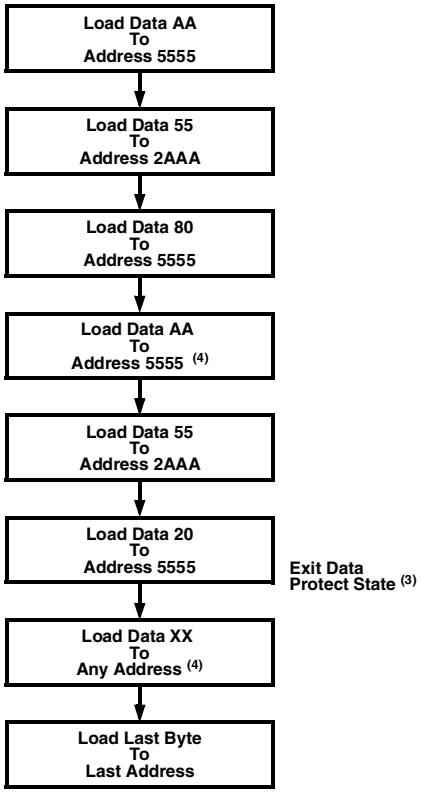


Figure 8
Software Data
Protection Disable Algorithm (1)



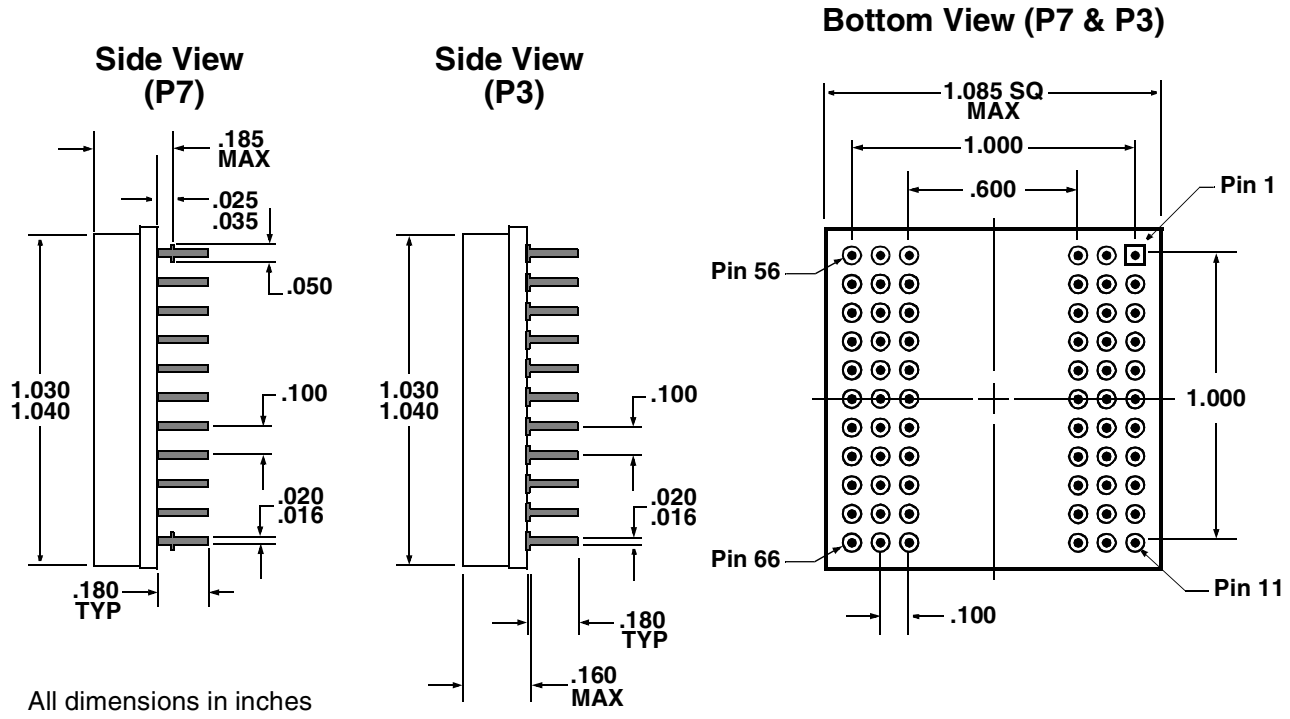
NOTES:
1. Data Format: I/O0 - I/O7 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end ot write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

Pin Numbers & Functions

66 Pins — PGA Type Package							
Pin #	**Function**	**Pin #**	**Function**	**Pin #**	**Function**	**Pin #**	**Function**
1	I/O_8	18	A_{12}	35	I/O_{25}	52	$\overline{WE}_3$
2	I/O_9	19	V_{CC}	36	I/O_{26}	53	$\overline{CE}_3$
3	I/O_{10}	20	$\overline{CE}_1$	37	A_6	54	GND
4	A_{13}	21	NC	38	A_7	55	I/O_{19}
5	A_{14}	22	I/O_3	39	NC	56	I/O_{31}
6	A_{15}	23	I/O_{15}	40	A_8	57	I/O_{30}
7	A_{16}	24	I/O_{14}	41	A_9	58	I/O_{29}
8	NC	25	I/O_{13}	42	I/O_{16}	59	I/O_{28}
9	I/O_0	26	I/O_{12}	43	I/O_{17}	60	A_0
10	I/O_1	27	$\overline{OE}$	44	I/O_{18}	61	A_1
11	I/O_2	28	NC	45	V_{CC}	62	A_2
12	$\overline{WE}_2$	29	$\overline{WE}_1$	46	$\overline{CE}_4$	63	I/O_{23}
13	$\overline{CE}_2$	30	I/O_7	47	$\overline{WE}_4$	64	I/O_{22}
14	GND	31	I/O_6	48	I/O_{27}	65	I/O_{21}
15	I/O_{11}	32	I/O_5	49	A_3	66	I/O_{20}
16	A_{10}	33	I/O_4	50	A_4		
17	A_{11}	34	I/O_{24}	51	A_5		

Note: Pins 8, 21, 28 & 39 can be connected to ground by specifing Option "C".

"P3" — 1.08" SQ PGA Type (without shoulder) Package
"P7" — 1.08" SQ PGA Type (with shoulder) Package



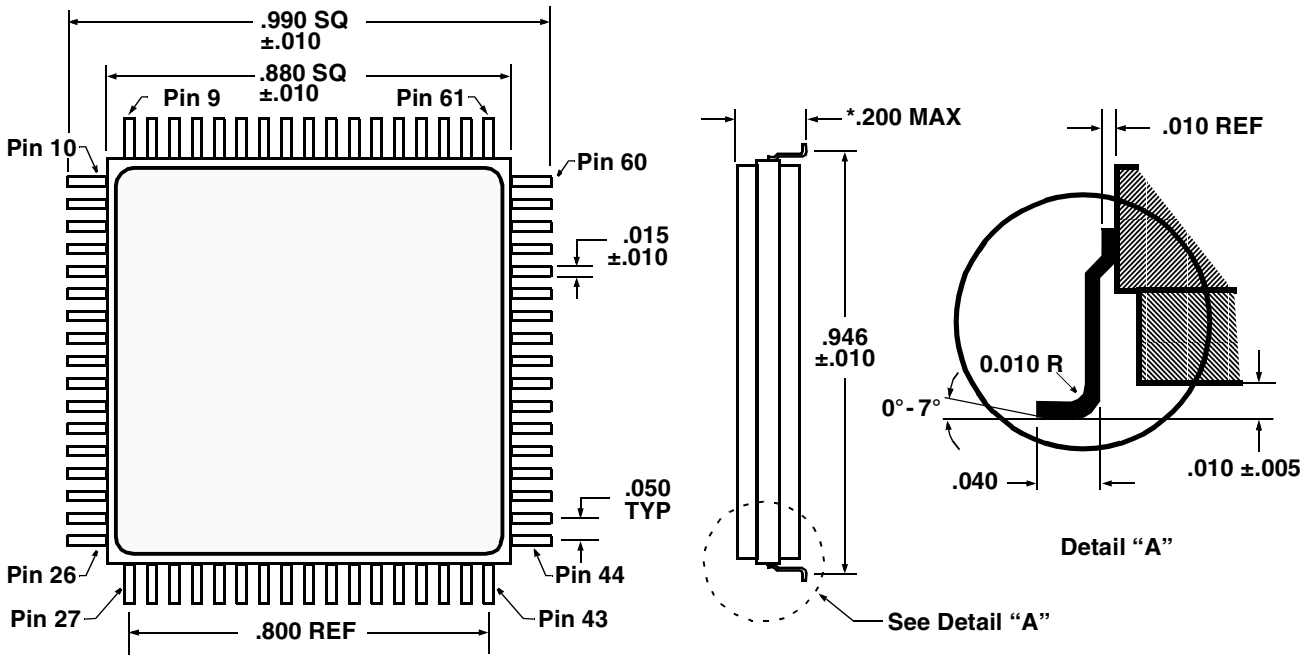
All dimensions in inches

Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	NC	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WE}_2$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	$\overline{WE}_3$	56	I/O_{20}
6	A_2	23	I/O_{12}	40	$\overline{WE}_4$	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE1}$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Package Outline — Dual-Cavity CQFP "F2"

Top View



***.180 MAX available, call factory for details**

All dimensions in inches

AEROFLEX
CIRCUIT TECHNOLOGY

Ordering Information

Model Number	DESC Drawing Number	Speed	Package
ACT-E128K32N-120P7Q	5962-9458506H4X	120ns	PGA Type
ACT-E128K32C-120P7Q	5962-9458506H5X	120ns	PGA Type
ACT-E128K32N-140P7Q	5962-9458505H4X	140ns	PGA Type
ACT-E128K32C-140P7Q	5962-9458505H5X	140ns	PGA Type
ACT-E128K32N-150P7Q	5962-9458504H4X	150ns	PGA Type
ACT-E128K32C-150P7Q	5962-9458504H5X	150ns	PGA Type
ACT-E128K32N-200P7Q	5962-9458503H4X	200ns	PGA Type
ACT-E128K32C-200P7Q	5962-9458503H5X	200ns	PGA Type
ACT-E128K32N-250P7Q	5962-9458502H4X	250ns	PGA Type
ACT-E128K32C-250P7Q	5962-9458502H5X	250ns	PGA Type
ACT-E128K32N-300P7Q	5962-9458501H4X	300ns	PGA Type
ACT-E128K32C-300P7Q	5962-9458501H5X	300ns	PGA Type
ACT-E128K32N-120F2Q	5962-9458506HMX	120ns	CQFP
ACT-E128K32N-140F2Q	5962-9458505HMX	140ns	CQFP
ACT-E128K32N-150F2Q	5962-9458504HMX	150ns	CQFP
ACT-E128K32N-200F2Q	5962-9458503HMX	200ns	CQFP
ACT-E128K32N-250F2Q	5962-9458502HMX	250ns	CQFP
ACT-E128K32N-300F2Q	5962-9458501HMX	300ns	CQFP

Part Number Breakdown

ACT– E 128K 32 N– 200 P7 M

Aeroflex Circuit Technology

Memory Type
E = EEPROM

Memory Depth

Memory Width, Bits

Options
N = None
C = Connect to GND – Pins 8,21,28,39 (P3 & P7 Pkg only)

Memory Speed, ns

Screening
C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screening *
Q = MIL-PRF-38534 Compliant / SMD

Package Type & Size

Surface Mount Packages
F2 = .88"SQ 68 Lead Dual-Cavity CQFP

Thru-Hole Packages
P3 = 1.085"SQ PGA 66 Pins without shoulder
P7 = 1.085"SQ PGA 66 Pins with shoulder

*** Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice.

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