82C425

T-52-33-45

CGA LCD/CRT Controller

Data Sheet

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P R E L I M I N A R Y

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CHIPS®

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T-52-33-45

82C425
CGA LCD/CRT
Controller

- Single chip 100% IBM CGA compatible LCD/CRT controller
- Very low power 100-pin CMOS device
- Supports all CGA modes
- Supports up to eight gray scales
- Intelligent memory arbitration
- Supports two fonts
- Built-in CPU interface
- Interfaces directly to SRAMs used for display and font memory
- Ideal for laptop computers

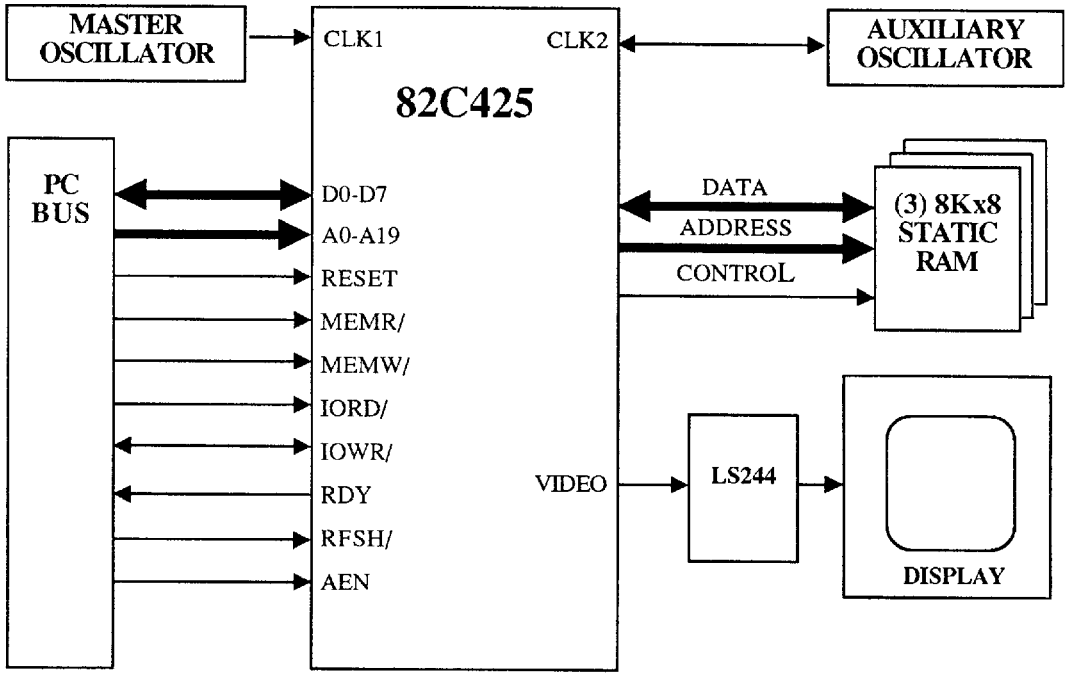

Figure 1: 82C425 System Block Diagram

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Revision History

Revision	Date	By	Comment
1.1*	1/14/91	TDC	Reformatted Document
2.2	5/15/91	JS	Final Revisions

* = Internal Release

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Introduction

The 82C425 is a display controller for Liquid Crystal Displays (LCDs) and CRTs. It is ideal for portable, laptop and palm top IBM-compatible computers. The device is designed to drive a single-panel, single-drive LCD with 4 bits of parallel data. LCDs having 200 dot vertical resolution and panel duty cycles of 1/200 are supported. The 82C425 also supports CGA-compatible CRTs and is fully compatible with applications designed for the IBM Color Graphics Adapter.

CPU/82C425 Interface

The 82C425 interfaces directly to the PC I/O bus with no "glue" logic, using separate data and address buses. Two external clock inputs are supported; either can be selected under software control. Direct connection to display and font SRAMs is supported; a buffer is used for driving each display. Figure 1 depicts a graphics sub-system using the 82C425.

OPERATING MODES

The 82C425 supports all CGA modes. These include:

80x25 and 40x25 text modes and 640x200 monochrome graphics and 320x200 four color graphics modes. A mode is selected by writing the appropriate value to the Mode Control register at I/O address 3D8h, and initializing other registers as necessary.

TEXT MODES

80 x 25 Text Mode

This mode is compatible with applications developed for CGA 80-column text mode. Up to 4 text pages can be stored in display memory, starting at address B8000h. Each page occupies 4 Kbytes.

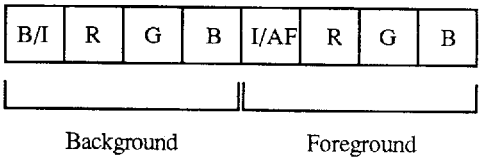
Text is normally displayed in an 8 by 8 pixel character cell. Fonts are stored in and accessed from an external static RAM. Either the default system font (loaded by the BIOS during initialization) or an optional user-defined font may be used.

40 x 25 Text Mode

This mode is compatible with 40-column CGA applications. Only 2K bytes are required per text page, so up to 8 pages can be stored in the display memory starting at B8000h. The same font(s) are used as with 80 column mode; each pixel is doubled in the horizontal direction to yield a character cell which is 16 pixels wide by 8 pixels high.

Text Mode Attribute Byte Processing

Every character on the screen is defined by two bytes in the display buffer. The byte at the even CPU address (starting at B8000h) contains the character code while that at the odd address (starting at B8001h) contains the attribute byte for that character code. The first two bytes in the display memory buffer define the character at the upper left corner of the screen. The bits in the attribute byte are defined as follows:



Definition of the bits in the attribute byte is identical for both CRT displays and LCDs; color information is, however, treated differently when using an LCD as colors are mapped to gray scales. See below for further details.

The upper four bits define the background color of a character while the lower 4 bits define the foreground color. Bit 7 (B/I) can be defined as either the background color intensity bit or the blinking attribute bit. Bit 5 of the Mode Control register (I/O Address 3D8h) determines the function of bit 7. If blink is enabled with bit 5 of the Mode Control register, it is enabled for the entire screen.

Bit 3 (I/AF) is defined as either the foreground intensity bit or the alternate font selection bit depending on the state of bit 6 of the Function Control register (RDF) as follows:

RDF bit 6	I/AF Function
0	Foreground color intensity bit
1	Alternate font selection bit

Note that I/AF can be used to select either of the two RAM-resident character sets on a character by character basis. This selection can be done on-the-fly. If intensified font is desired, it must be loaded as the primary font, in order to use intensity bit.

CRT Display Attribute Byte Processing

With an IBM CGA-compatible CRT attached, the 82C425 operates in a fashion identical to the IBM

CGA. All CGA-compatible applications software will operate without modification.

LCD Attribute Byte Processing

For LCD displays, bit definitions of the attribute byte are identical to those used with a CRT. This means that all CGA-compatible applications software will run without modification. Since colors are not available, however, the 82C425 maps foreground and background colors of characters to one of either four or eight different gray values. This proprietary mapping technique is based on weighting the R, G, B, I bits such that R is the most significant bit and I the least. To maximize the contrast of the values generated with this mapping scheme, an optional proprietary technique called SMARTMAP™ (explained below) is available on chip.

SMARTMAP™

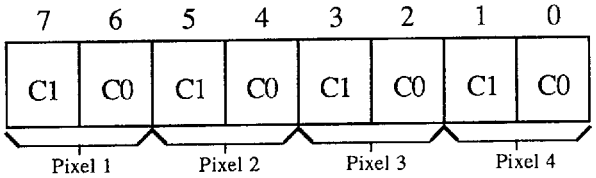
As mentioned above, when an LCD is used with a CGA text mode, the SMARTMAP scheme can be invoked to intelligently map colors to gray scale values. This scheme works by first comparing and then suitably adjusting the foreground and background values to produce adequate display contrast on LCD screens. The minimum contrast level is determined by a value programmed in the Threshold register (RDAh). The contrast enhancement value used to adjust the foreground and background values is stored in the Shift Parameter register (RDBh). The SMARTMAP technique uses these values to enhance the legibility of CGA text on LCD panels.

GRAPHICS MODES

The 82C425 supports both graphics modes provided by the CGA. Each is described below. In both modes, display memory organization is identical to the IBM CGA meaning that CGA applications software will run without modification. This is the case for both CRT displays and LCDs.

320 x 200 Four Color Graphics Mode

In this mode, each pixel is represented by two bits called C0 and C1. For each scan line, C0 and C1 are stored in display memory as follows:



When stored in display memory, all bits (C0, C1) associated with even scan lines (0,2,4,...198) are stored beginning at hex address B8000. Odd scan lines are stored beginning at BA000h. This arrangement is depicted below in Figure 2.

When displayed on the screen, the pixels appear as shown in Figure 3 below.

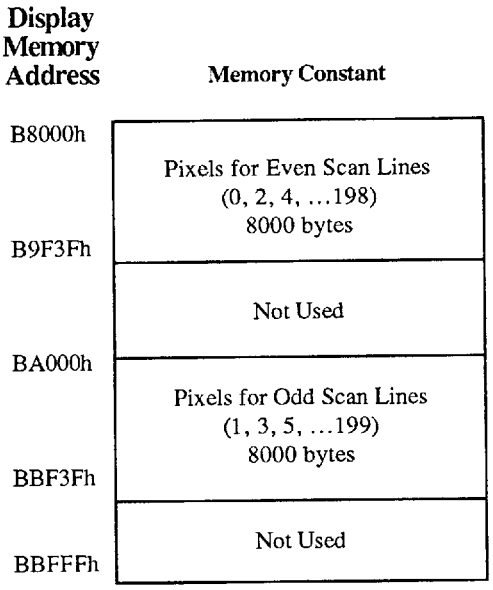


Figure 2: Graphics Mode Pixel Storage in Display memory

When displayed on the screen, the pixels appear as shown in Figure 3 below.

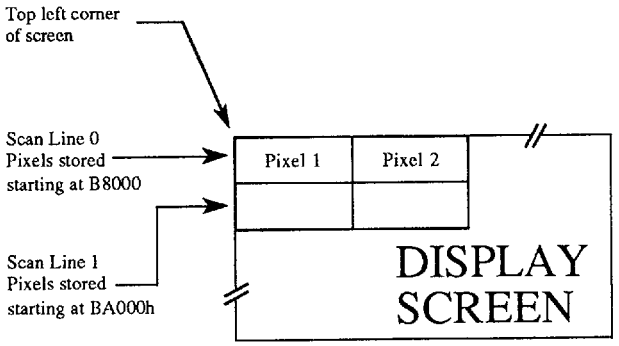


Figure 3: Correspondence of Display RAM Addresses to Screen Locations in Graphics Modes

With two bits per pixel, each pixel can be displayed as any one of 4 different colors. When a CGA compatible

CRT display is used, operation is identical to the IBM CGA. When an LCD is used, the 320 x 200 4-color (2 bits/pixel) mode is displayed on a 640-pixel panel by mapping each pixel in memory to 2 pixels on the panel. This is depicted in Figure 4. The two pixels on the panel, however, are individually controlled depending on the color of the corresponding pixel in memory and the frame number.

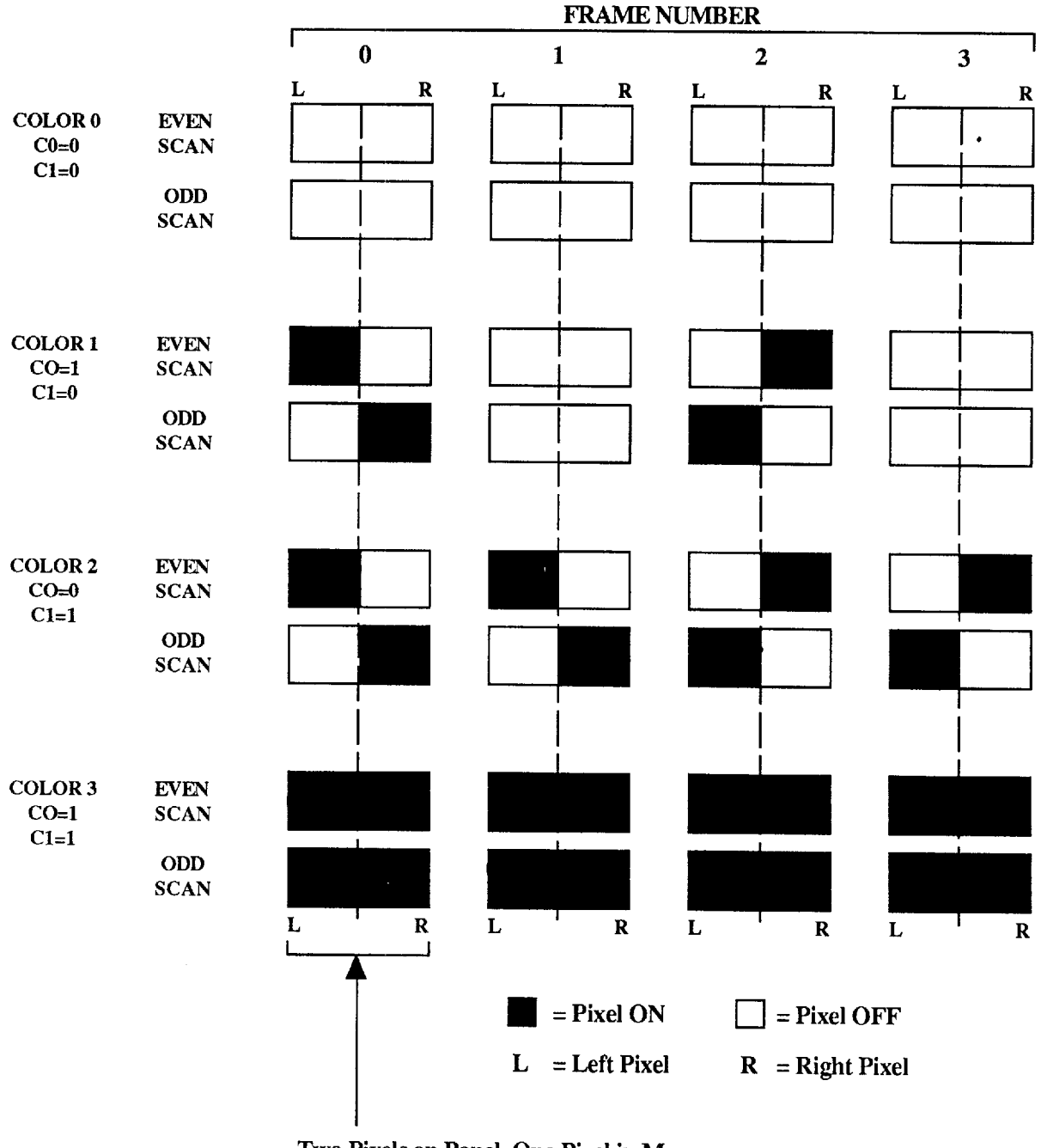


Figure 4: 320 Pixel/Line 4-Level Gray Scale Scheme Displayed on 640 Pixel/Line Panel

640 x 200 Monochrome Mode

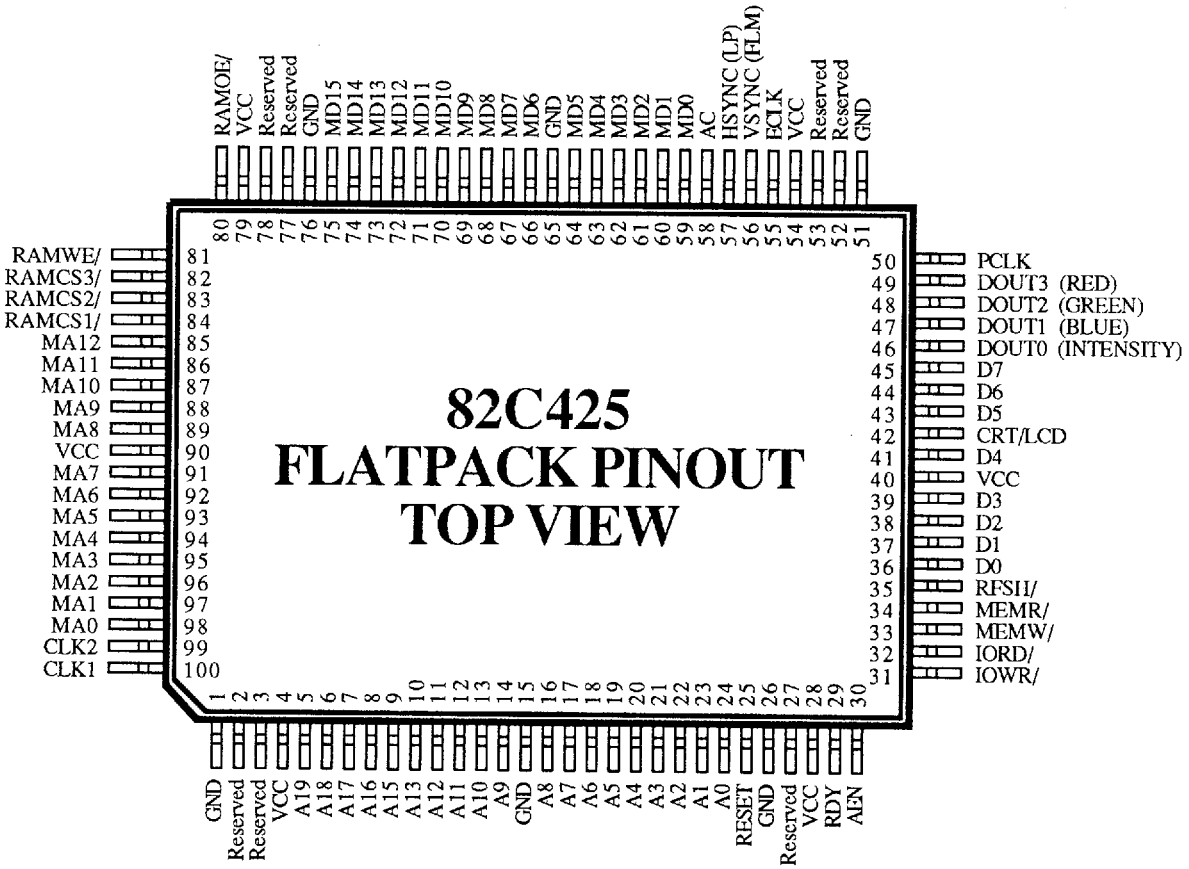
In this mode, one bit of display memory is used for each screen pixel as follows:

7	6	5	4	3	2	1	0
Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8

As with 320 x 200 mode, pixels for a single scan line are stored in bytes located at sequentially increasing addresses in display memory. The highest order bit in a byte is displayed on the screen first. Odd and even scan lines are stored in separate 8 Kbyte blocks of display memory. Figures 2 and 3 are also applicable for 640 x 200 mode.

A single display page is supported. Since this is a monochrome mode, the screen display with a CRT is identical to that achieved with an LCD.

82C425 Pin Diagrams



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82C425 Pin List

Pin Name	Pin #
A0	24
A1	23
A2	22
A3	21
A4	20
A5	19
A6	18
A7	17
A8	16
A9	14
A10	13
A11	12
A12	11
A13	10
A15	9
A16	8
A17	7
A18	6
A19	5
AC	58
AEN	30
CLK1	###
CLK2	99
CRT/LCD	42
D0	36
D1	37
D2	38
D3	39
D4	41
D5	43
D6	44
D7	45
DOUT0 or INTENSITY	46

Pin Name	Pin #
DOUT1 or BLUE	47
DOUT2 or GREEN	48
DOUT3 or RED	49
GND	1
GND	15
GND	26
GND	51
GND	65
GND	76
HSYNC or LP	57
IOR/	32
IOW/	31
MA0	98
MA1	97
MA2	96
MA3	95
MA4	94
MA5	93
MA6	92
MA7	91
MA8	89
MA9	88
MA10	87
MA11	86
MA12	85
MD0	59
MD1	60
MD2	61
MD3	62
MD4	63
MD5	64
MD6	66
MD7	67

Pin Name	Pin #
MD9	69
MD10	70
MD11	71
MD12	72
MD13	73
MD14	74
MD15	75
MEMR/	34
MEMW/	33
NC	2
NC	3
NC	27
NC	52
NC	53
NC	77
NC	78
PCLK	50
RAMCS1/	84
RAMCS2/	83
RAMCS3/	82
RAMOE/	80
RAMWE/	81
READY	29
REFRESH/	35
RESET	25
VCC	4
VCC	28
VCC	40
VCC	54
VCC	79
VCC	90
VSYNC or FLM	56

82C425 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
24	A0	In	Both	Host computer system Address Bus.
23	A1	In	Both	
22	A2	In	Both	
21	A3	In	Both	
20	A4	In	Both	
19	A5	In	Both	
18	A6	In	Both	
17	A7	In	Both	
16	A8	In	Both	
14	A9	In	Both	
13	A10	In	Both	
12	A11	In	Both	
11	A12	In	Both	
10	A13	In	Both	
9	A15	In	Both	
8	A16	In	Both	
7	A17	In	Both	
6	A18	In	Both	
5	A19	In	Both	
36	D0	I/O	Both	Host computer system Data Bus.
37	D1	I/O	Both	
38	D2	I/O	Both	
39	D3	I/O	Both	
41	D4	I/O	Both	
43	D5	I/O	Both	
44	D6	I/O	Both	
45	D7	I/O	Both	
30	AEN	In	High	Address Enable. A high level indicates that a DMA operation is in progress. When low, the host CPU has control of address and command lines.
33	MEMW/	In	Low	Memory Write. This input must be low when the PC writes display/font memory.
34	MEMR/	In	Low	Memory Read. This input must be low when the CPU reads display/font memory.
31	IOWR/	In	Low	I/O Write. This input must be low when the CPU writes 82C425 internal registers.
32	IORD/	In	Low	I/O Read. This input must be low when the CPU reads 82C425 internal registers.
29	RDY/	Out	High	This normally-high pin (READY) is pulled low (not READY) when the 82C425 needs to extend the current CPU bus cycle. Upon completion of this bus cycle, the 82C425 drives this output high for one dot clock. When not active, this pin is 3-stated.

82C425 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
35	RFSH/	In	Low	Host computer system memory refresh. This pin is high for non-refresh cycles
25	RESET	In	High	Reset signal
100	CLK1	In	Both	Master Clock Input
99	CLK2	In	Both	Auxiliary Master Clock Input
59	MD0	I/O	Both	Display and font RAM Data Bus
60	MD1	I/O		
61	MD2	I/O		
62	MD3	I/O		
63	MD4	I/O		
64	MD5	I/O		
66	MD6	I/O		
67	MD7	I/O		
68	MD8	I/O		
69	MD9	I/O		
70	MD10	I/O		
71	MD11	I/O		
72	MD12	I/O		
73	MD13	I/O		
74	MD14	I/O		
75	MD15	I/O		
98	MA0	Out	Both	Display and font RAM Address Bus
97	MA1	Out		
96	MA2	Out		
95	MA3	Out		
94	MA4	Out		
93	MA5	Out		
92	MA6	Out		
91	MA7	Out		
89	MA8	Out		
88	MA9	Out		
87	MA10	Out		
86	MA11	Out		
85	MA12	Out		
84	RAMCS1/	Out	Low	Chip select for Display RAM 1
83	RAMCS2/	Out	Low	Chip select for Display RAM 2
82	RAMCS3/	Out	Low	Chip select for Character Generator (font) RAM
81	RAMWE/	Out	Low	Display and font RAM Write Enable
80	RAMOE/	Out	Low	Display and font RAM Output Enable

82C425 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
57	HSYNC or LP	Out	High	Hsync for CRT display. Latch Pulse input to LCD.
56	VSYNC or FLM	Out	High	Vsync for CRT display. First Line Marker input to LCD.
58	AC	Out	Both	AC input to LCD
55	ECLK	Out	High	Enable Clock input to LCD. Not used by all LCDs.
50	PCLK	Out	Both	Panel Shift Clock output
46	DOUT0 or INTENSITY	Out	Both	Intensity signal for CRT display. Bit 0 of LCD data.
47	DOUT1 or BLUE	Out	Both	Blue signal for CRT display. Bit 1 of LCD data.
48	DOUT2 or GREEN	Out	Both	Green signal for CRT display. Bit 2 of LCD data.
49	DOUT3 or RED	Out	Both	Red signal for CRT display. Bit 3 of LCD data.
42	CRT/LCD	Out	Both	The CRT/LCD output is used to select the current display type. This pin reflects the state of bit 3 of register RDF. It is high for a CRT, low for an LCD.
4	VCC	+5V		Power Pins
28	VCC			
40	VCC			
54	VCC			
79	VCC			
90	VCC			
1	GND	Gnd		Ground
15	GND			
26	GND			
51	GND			
65	GND			
76	GND			
2	NC			No connects
3	NC			
27	NC			
52	NC			
53	NC			
77	NC			
78	NC			

82C425 Registers

The 82C425 contains registers which define and control a raster-scan CRT display or single-panel LCD. Most of these registers are accessed with a two step process that uses two byte addresses in the CPU I/O space. First, a pointer to the desired register is written into the address register (I/O address 3D4h). Then the data register is read or written (I/O address 3D5h). Unless otherwise specified, the default contents of all registers are undefined on power-up.

CRT CONTROLLER REGISTERS

The Address Register is a 8-bit index to the CRT Controller Registers. Nineteen registers perform all display functions for modes: horizontal and verticle blank and sync, cursor size & location, and light pen.

EXTENSION REGISTERS

The 82C425 defines a set of extension registers, most of which are addressed with the 8-bit Address Register. The extension registers handle display and interfacing functions.

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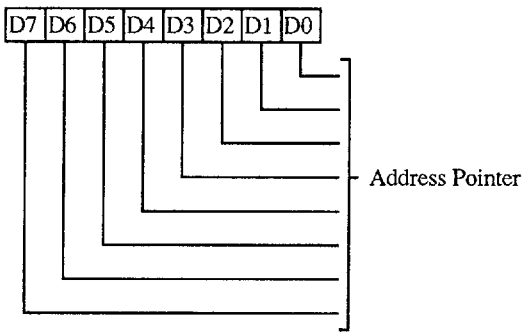
82C425 CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
–	Address Register	–	RW	3D4h	–	17
R0	Horizontal Total	00h	RW	3D5h	–	17
R1	Horizontal Displayed	01h	RW	3D5h	–	18
R2	Horizontal Sync Position	02h	RW	3D5h	–	18
R3	Ignored	03h	–	3D5h	–	–
R4	Vertical Total	04h	RW	3D5h	–	18
R5	Vertical Total Adjust	05h	RW	3D5h	–	18
R6	Vertical Displayed	06h	RW	3D5h	–	19
R7	Vertical Sync Position	07h	RW	3D5h	–	19
R8	Ignored	08h	–	3D5h	–	–
R9	Maximum Scans/Row	09h	RW	3D5h	–	19
RA	Cursor Start Scan	0Ah	RW	3D5h	–	20
RB	Cursor End Scan	0Bh	RW	3D5h	–	20
RC	Start Address High	0Ch	RW	3D5h	–	21
RD	Start Address Low	0Dh	RW	3D5h	–	21
RE	Cursor Address High	0Eh	RW	3D5h	–	21
RF	Cursor Address Low	0Fh	RW	3D5h	–	21
R10	Light Pen High	10h	R	3D5h	–	22
R11	Light Pen Low	11h	R	3D5h	–	22

ADDRESS REGISTER

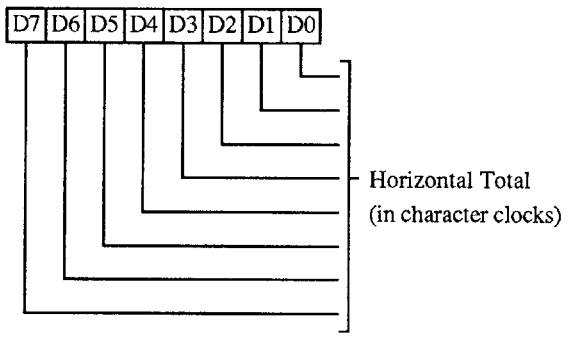
Read/Write at I/O Address 3D4h



7 - 0 The Address Register is an 8 bit register. When loaded with a binary value (pointer), it points to the data register to be accessed.

HORIZONTAL TOTAL REGISTER (R0)

Read/Write at I/O Address 3D5h
Index 00h

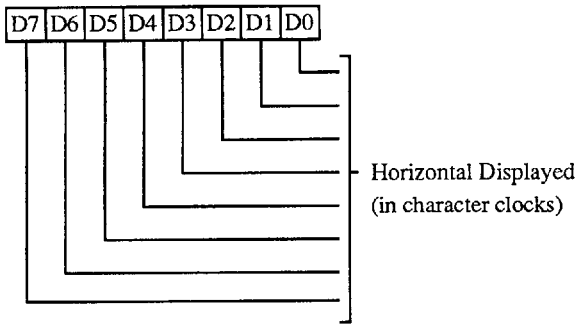


7 - 0 The Horizontal Total Register defines the number of characters in a horizontal scan line, including the retrace time. As such, it defines the horizontal sweep rate. The value programmed in this register is one less than the total character clocks in a horizontal scan line.

This register is ignored when an LCD display is used.

HORIZONTAL DISPLAYED REGISTER (R1)

Read/Write at I/O Address 3D5h
Index 01h

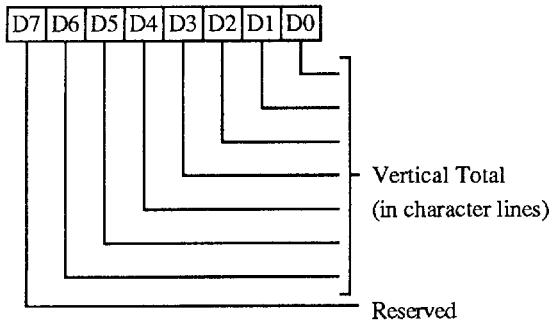


7 - 0 This 8-bit register determines the number characters displayed per line, not including retrace time.

This register is used with both CRT and LCD displays.

VERTICAL TOTAL REGISTER (R4)

Read/Write at I/O Address 3D5h
Index 04h



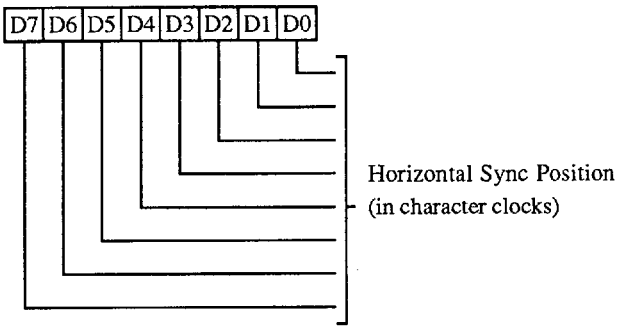
6 - 0 The Vertical Total Register and Vertical Total Adjust Register together determine the number of scan lines per frame. The value in the Vertical Total Register represents character row times while that in the Vertical Total Adjust register represents scan lines. The value programmed in this register is one less than the number of character rows per frame.

7 - 0 Reserved (0)

This register is ignored when an LCD display is used.

HORIZONTAL SYNC POSITION REGISTER (R2)

Read/Write at I/O Address 3D5h
Index 02h

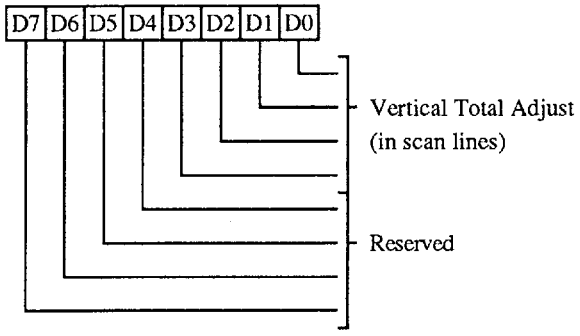


7 - 0 The Horizontal Sync Position Register controls the position of the horizontal sync pulse. The value programmed corresponds to the character location of the start of the horizontal sync pulse; characters are numbered from zero. When the programmed value is increased, the display on the CRT is shifted to the left. When the value is decreased, the display is shifted to the right.

This register is ignored when an LCD display is used.

VERTICAL TOTAL ADJUST (R5)

Read/Write at I/O Address 3D5h
Index 05h



3 - 0 Vertical Total Adjust

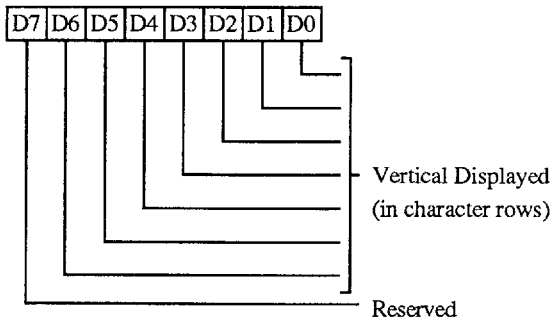
This 4-bit register defines the number of scan lines to be added to the Vertical Total Register content to determine the frame rate.

7 - 4 Reserved (0)

This register is ignored when an LCD display is used.

VERTICAL DISPLAYED REGISTER (R6)

Read/Write at I/O Address 3D5h
Index 06h



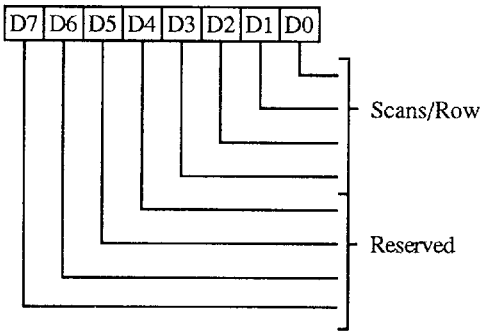
6 - 0 This 7-bit register specifies the number of displayed character rows per frame. This register is programmed in character row times.

7 Reserved (0)

This register is used with both CRT and LCD displays.

MAXIMUM SCAN LINE (R9)

Read/Write at I/O Address 3D5h
Index 09h



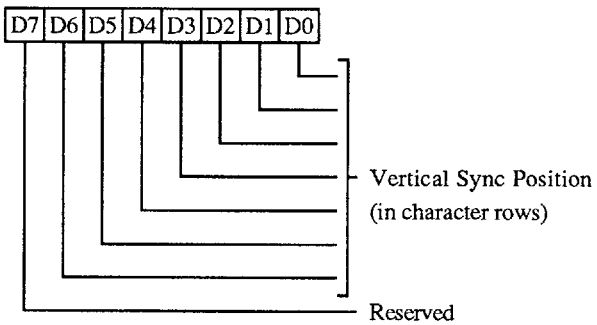
3 - 0 This 4-bit register determines the number of scan lines per character row. The row address counter is controlled by this register. The programmed value is one less than the number of scan lines/row.

7 - 4 Reserved (0)

This register is used with both CRT and LCD displays.

VERTICAL SYNC POSITION (R7)

Read/Write at I/O Address 3D5h
Index 07h



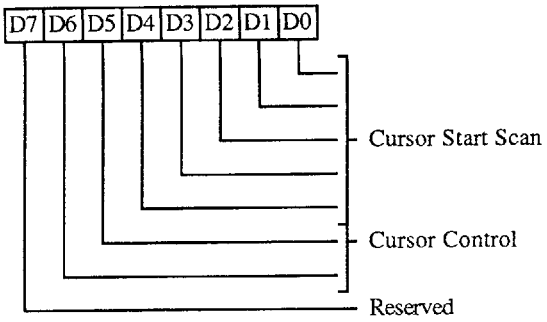
6 - 0 This 7-bit register defines the position of VSYNC and is programmed in terms of character row times. The programmed value corresponds to the character row at which the vertical sync pulse occurs; row are numbered from 0. When the programmed value is increased the display on the CRT is shifted up; when decreased it is shifted down.

7 Reserved (0)

This register is ignored when an LCD display is used.

CURSOR START REGISTER (RA)

Read/Write at I/O Address 3D5h
Index 0Ah



4 - 0 Bits 0 - 4 specify the scan line (starting from 0) within a character row where the rectangular cursor block begins. The programmed value is the scan line at which the cursor starts.

6 - 5 Bits 6 and 5 control display of the text cursor as follows:

6	5	Cursor Attributes
0	0	Cursor is blinked at the blink rate
0	1	Cursor is turned off
1	0	Cursor is blinked at the blink rate
1	1	Cursor is blinked at half the blink rate

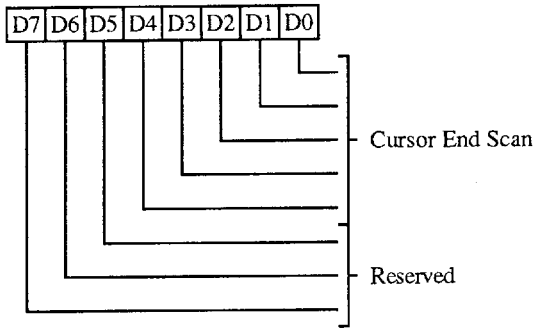
The blink rate is defined by the Verticle Sync Width/Blink Control Register (RDD). The default blink rate is 1/16 of the frame rate (blink on the eight frames, off for the eight frames).

7 - 5 Reserved (0)

This register is used with both CRT and LCD displays.

CURSOR END REGISTER (RB)

Read/Write at I/O Address 3D5h
Index 0Bh



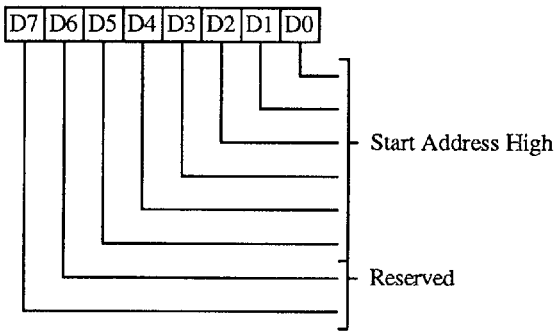
4 - 0 Bits 0 - 4 specify the scan line (starting from 0) within a character row where the rectangular cursor block ends. The pro-grammed value is one less than the scan line at which the cursor ends. If cursor start > cursor end, no cursor is displayed.

7 - 5 Reserved (0)

This register is used with both CRT and LCD displays.

START ADDRESS HIGH REGISTER (RC)

Read/Write at I/O Address 3D5h
Index 0Ch



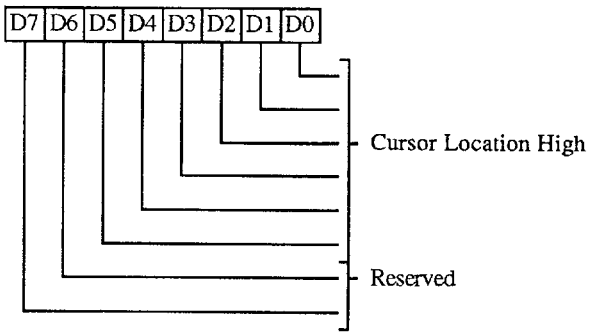
5 - 0 The Start Address is a 14-bit value which specifies the word address in the display buffer at which screen refresh starts. This display buffer address is mapped to the upper left corner of the screen. The Start Address High Register contains the 6 high-order bits of this address, while the Start Address Low Register specifies the 8 low Start Address High register is read/write and does not affect the screen refresh start address.

7 - 6 Reserved (0)

This register is used with both CRT and LCD displays.

CURSOR LOCATION HIGH REGISTER (RE)

Read/Write at I/O Address 3D5h
Index 0Eh



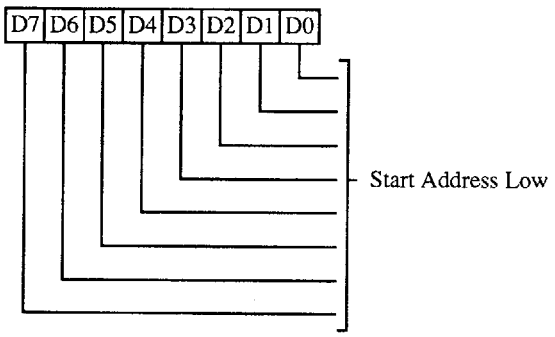
5 - 0 The Cursor Location address is a 14-bit value. The 6 high-order bits are programmed in the Cursor Location High Register. The 8 low-order bits are programmed in the Cursor Location Low Register. This 14-bit word address defines the display memory word address for the character which has the cursor superimposed on it. The most significant bit of the Start Address High register is read/write and does not affect the cursor address.

7 - 6 Reserved (0)

This register is used with both CRT and LCD displays.

START ADDRESS LOW REGISTER (RD)

Read/Write at I/O Address 3D5h
Index 0Dh

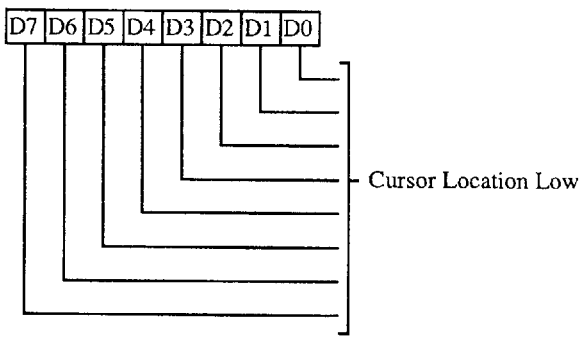


7 - 0 These 8 bits are the low-order bits of the 14-bit word address in display memory at which screen refresh starts. This display buffer address is mapped to the upper left corner of the screen. The Start Address High Register contains the 6 high-order bits of this address.

This register is used with both CRT and LCD displays.

CURSOR LOCATION LOW REGISTER (RF)

Read/Write at I/O Address 3D5h
Index 0Fh

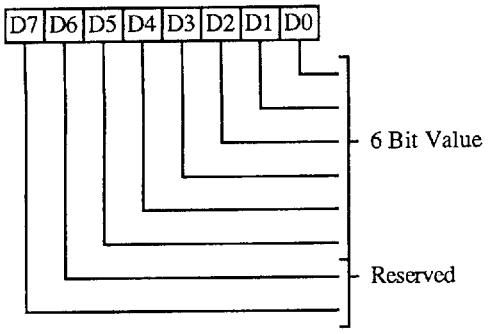


7 - 0 These 8 bits are the low-order bits of the 14-bits Cursor Location address. The upper 6 bits are programmed in the cursor location high register. Together these 14 bits for the display memory word address at which the cursor is located.

This register is used with both CRT and LCD displays.

LIGHT PEN HIGH REGISTER (R10)

Read/Write at I/O Address 3D5h
Index 10h



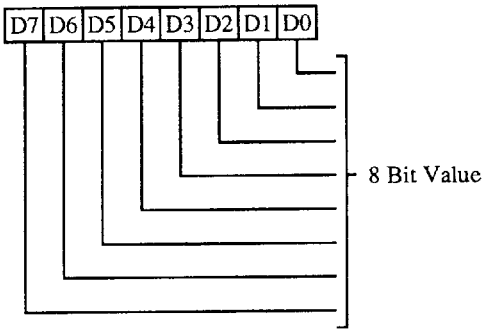
5 - 0 This register returns the upper six bits of the address latched by the light pen strobe. The active edge of the light pen strobe is generated by reading or writing the Set Light Pen Register (address 3DCh); the other edge is generated by reading or writing the Clear Light Pen Register (address 3DBh).

7 - 6 Reserved (0)

This register is used with both CRT and LCD displays.

LIGHT PEN LOW REGISTER (R11)

Read only at I/O Address 3D5h
Index 11h



7 - 0 This register returns the lower eight bits of the address latched by the light pen strobe. It is included for CGA software compatibility. The active edge of the light pen strobe is generated by reading or writing the Set Light Pen Register (address 3DCh); the other edge is generated by reading or writing the Clear Light Pen Register (address 3DBh).

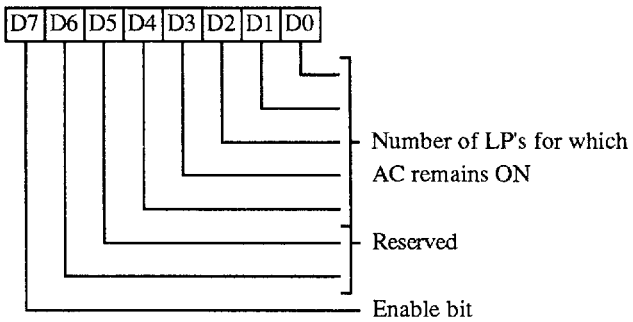
This register is used with both CRT and LCD displays.

82C425 Extension Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
RD9	AC Control	D9h	RW	3D5h	–	23
RDA	Threshold	DAh	RW	3D5h	–	24
RDB	Shift Parameter	DBh	RW	3D5h	–	24
RDC	Horizontal Sync Width	DCh	RW	3D5h	–	25
RDD	Vertical Sync Width/Blink Control	DDh	RW	3D5h	–	25
RDE	Timing Control	DEh	RW	3D5h	–	26
RDF	Function Control	DFh	RW	3D5h	–	26
–	Mode Control	–	RW	3D8h	–	27
–	Color Select	–	RW	3D9h	–	28
–	Input Status	–	R	3DAh	–	29
–	Clear Light Pen	–	RW	3DBh	–	29
–	Set Light Pen	–	RW	3DCh	–	30

AC CONTROL REGISTER (RD9)

Read/Write at I/O Address 3D5h
Index D9h



7 Enable programmable AC. This bit, when set, enables the programmable AC signal generation. When reset (to 0) the AC signal remains ON for one frame and OFF for the next.

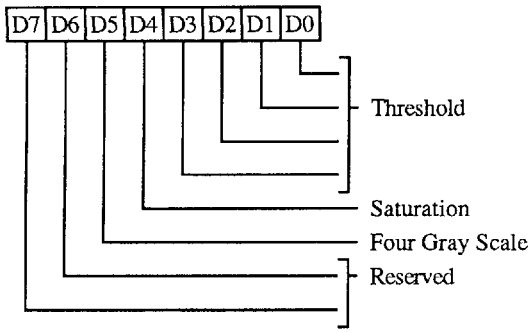
On reset, this bit is '0'.

6-5 Reserved (0)

4-0 The value programmed into this register is one less than the number of Latch Pulses for LCD displays which the AC signal is on and off (50% duty cycle).

THRESHOLD REGISTER (RDA)

Read/Write at I/O Address 3D5h
Index DAh



3-0 Threshold Value. These bits define a threshold used to determine when to apply foreground and background shift values. SMARTMAP applies the shift when the difference between foreground and background colors does not exceed this threshold value.

4 Saturation

- 0 The mapping of colors will be done with modulo-16 arithmetic.
- 1 The shift in foreground and background colors done by SMARTMAP will be limited to the saturation points, i.e. overflow will cause the full scale output and underflow will generate a zero output.

5 Four Gray Scale Bit.

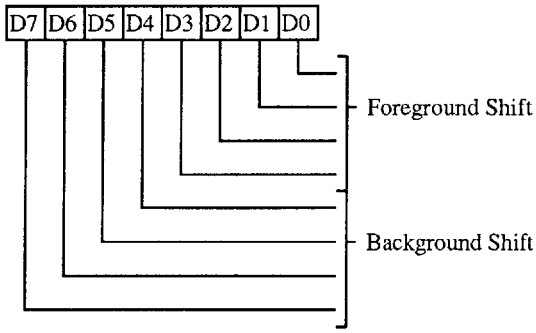
- 0 Eight gray scales are selected for text modes.
- 1 Four gray scale mode is selected.

7 - 6 Reserved (0)

On reset, this register contains 00h.

SHIFT PARAMETER REGISTER (RDB)

Read/Write at I/O Address 3D5h
Index DBh



As explained earlier, these shift values are used as part of SMARTMAP to increase contrast between foreground and background colors in gray scale text modes.

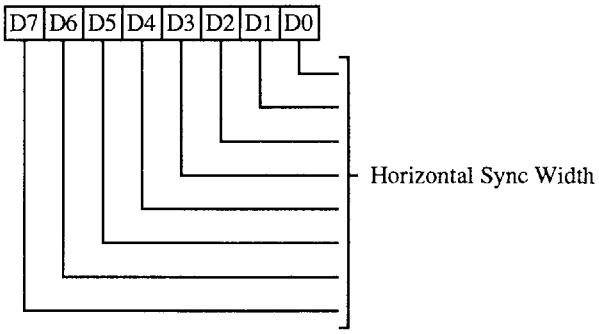
3-0 Foreground Shift. These four bits define the amount of shift for foreground colors in the text gray scale scheme.

7-4 Background Shift. These bits define the background color shift.

On reset, this register contains 00h.

HORIZONTAL SYNC WIDTH REGISTER

Read/Write at I/O Address 3D5h
Index DCh

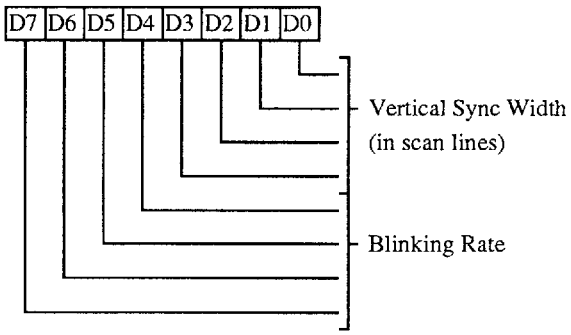


7 - 0 This register defines the width of the HSYNC pulse in terms of dot clocks. On power-up this register defaults to a value of 40h, which is compatible to IBM's CGA when the dot clock has a frequency of 14.318 MHz.

This register is ignored when a LCD display is used.

VERTICLE SYNC WIDTH REGISTER

Read/Write at I/O Address 3D5h
Index DDh



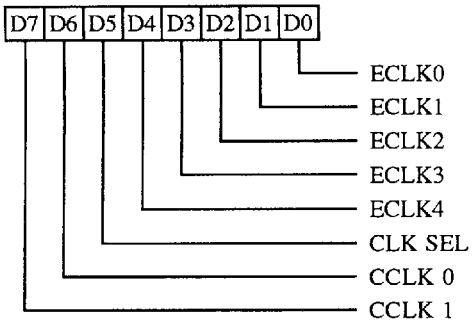
The lower 4 bits of this register define the width of VSYNC in terms of scan lines. On power-up these bits default to a value of 2, which is compatible to IBM's CGA. The actual number of scan lines is one more than the value programmed in this register.

The upper 4 bits define the blinking rate of characters. The cursor blink rate is double the character blink rate. If the programmed value is N, the character will be on for N+1 frames and off for N+1 frames; the cursor will be on for (N+1)/2 frames and off for (N+1)/2 frames.

The default value for blinking rate is 7.

TIMING CONTROL REGISTER (RDE)

Read/Write at I/O Address 3D5h
Index DEh



0-4 ECLK 4-0. These bits determine the period of the ENABLE CLOCK, if such a clock is required for the LCD panel type used. The number of output shift clocks required per enable clock is reduced by one and programmed into this register field.

5 CLK SEL. This bit selects which clock input will be used by the controller as the master clock source. A '0' in this bit selects CLK1 while a '1' selects the CLK2.

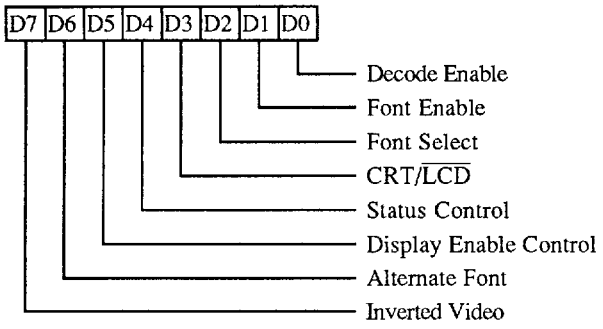
6-7 CCLK DIV 0-1. These bits determine the length of the panel shift clock in units of master clock cycles. These bits control the frequency of the pixel clock and panel shift clock as follows:

CCLK1	CCLK0	Pixel Frequency (CRT)	PCLK (LCD)
0	0	CLKIN/1	CLKIN/4
0	1	CLKIN/2	CLKIN/8
1	0	CLKIN/3	CLKIN/12
1	CLKIN/4	CLKIN/16	

In CRT mode, the panel shift clock is not used. On reset, this register contains 00h.

FUNCTION CONTROL REGISTER (RDF)

Read/Write at I/O Address 3D5h
Index DFh



0 Decode Enable. This bit controls the display buffer and I/O address decoding logic, and determines whether the device will respond to CPU memory and I/O accesses. When D0 = 0, the 82C425 will not respond to any accesses by the host CPU to the display buffer or I/O addresses 3Dx. This bit should be set to '1' to enable CPU I/O and memory accesses. It is initialized to '0' at reset, at which time it is write-only. After it is set to '1', it can be read.

1 Font Enable. This bit controls access to the font RAM. When set to '1', the font RAM can be accessed by the CPU as the first 8K bytes of the display buffer address space (B8000h - B9FFFh). When this bit is '0', access to the font RAM is disabled. This bit is initialized to '0' at reset.

2 Font Select. This bit controls the selection of one of the two fonts resident in the font RAM. When '0', the font resident in low memory (B8000h) is selected. When '1', the upper memory (B9000h) font is selected.

3 CRT/$\overline{\text{LCD}}$.

0 LCD is selected
1 CRT is selected

4 Status Control. For CRT: This bit is ignored for CRT displays.
For LCD: This bit affects the behavior of the Display Enable (3DA,D0) and Vertical Sync (3DA,D3) bits. When cleared (0), the Display Enable bit toggles every sixteen character clocks and the Vertical Sync bit is active during the first scan line.
When set (1), the Display Enable and Vertical Sync bits behave differently. The Display Enable bit is active during the first

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16 characters of each line and during all scanlines of rows 22 through the end of the panel in text modes (or row 85 through the end of the panel in graphics modes). The Vertical Sync bit is active during all scanlines of row 24 in text modes or rows 93 through 96 (inclusive) in graphics modes.

5 Enable Control
For CRT: This bit is ignored for CRT displays.
For LCD: This bit affects the behavior of the Enable Video bit (3D8, bit-3). When cleared (0), the Enable Video bit behaves as in CRT mode. When set (1), disabling of the video data stream by clearing Enable Video is delayed until Display Enable is inactive. This prevents changes to the Enable Video bit from disturbing the LCD panel during active video display.

6 Alternate Font

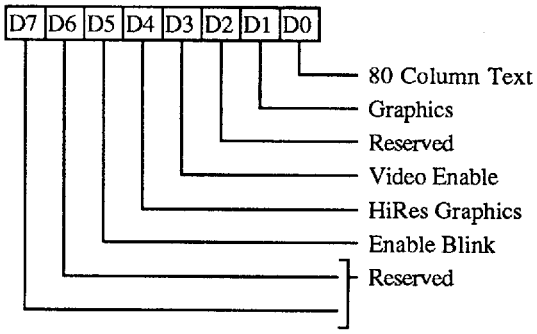
0 The Alternate Font is selected by attribute bit AT3.
1 Attribute bit AT3 is the foreground intensity bit.

7 - 0 Inverted Video

0 The video outputs are normal (positive true) TTL levels.
1 The video outputs are inverted.

On reset, this register contains 00h.

MODE CONTROL REGISTER
Read/Write at I/O Address 3D8h



4, 1, 0 CGA Submode Select
Submodes are defined by the following table (bit combinations not listed are illegal):

Bit 4	Bit 1	Bit 0	Submode
1	1	0	640 x 200 Graphics
0	1	0	320 x 200 Graphics
0	0	1	80 x 25 Text
0	0	0	40 x 25 Text

2 Reserved
3 Enable Video.

For CRT:
0 Video is enabled
1 Video is disabled

For LCD: Behavior of this bit depends on the Enable Control bit (RDF, 5). When the Enable Control bit is cleared this bit behaves the same as for a CRT. When the Enable Control bit is set, the effect of clearing this bit (disabling video) is delayed until the Display Enable bit is inactive. This prevents changes to the Enable Video bit from disturbing the LCD panel during active video display.

5 Enable Blink. When bit 5 = 1, blinking is controlled by attribute bit AT7. When 0, AT7 selects background intensity.

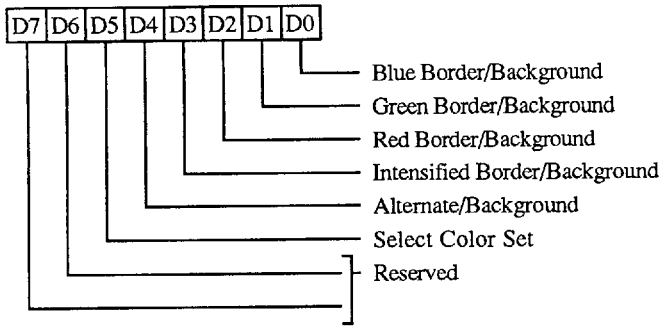
0 AT7 selects
1 Blinking

On reset, this register contains 00h.

7 - 6 Reserved

CGA COLOR SELECT REGISTER

Read/Write at I/O Address 3D9h



0 Blue Border/Background. Selects blue border in 40x25 CGA text mode. Selects blue background in CGA 320x200 graphics mode. Selects blue foreground in CGA 640x200 graphics mode.

1 Green Border/Background. Selects green border in 40x25 CGA text mode. Selects green background in CGA 320x200 graphics mode. Selects green foreground in CGA 640x200 graphics mode.

2 Red Border/Background. Selects red border in 40x25 CGA text mode. Selects red background in CGA 320x200 graphics mode. Selects red foreground in CGA 640x200 graphics mode.

3 Intensified Border/Background. Selects intensified border in 40x25 CGA text mode. Selects intensified background in CGA 320x200 graphics mode. Selects intensified foreground in CGA 640x200 graphics mode.

4 Alternate/Background. Selects alternate intensified colors in CGA graphics mode. Selects background colors in CGA text modes.

5 Select Color Set. Selects foreground colors in CGA 320x200 graphics mode. The colors are generated as shown in the table to the right.

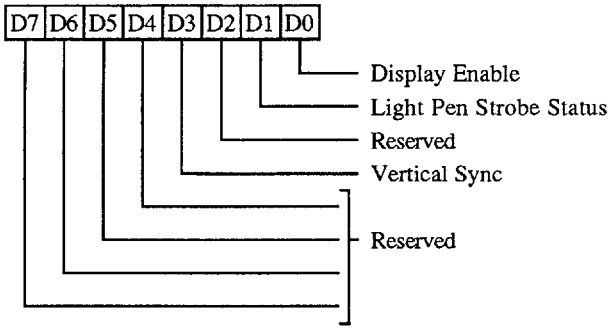
7 - 6 Reserved (0)

3D9 Bit 5	Pixel Bit 1	Pixel Bit 0	Foreground Color
0	0	0	Background (Bit 0 - 3)
0	0	1	Green
0	1	0	Red
0	1	1	Brown
1	0	0	Background (Bit 0 - 3)
1	0	1	Cyan
1	1	0	Magenta
1	1	1	White

On reset, this register contains 00h.

INPUT STATUS REGISTER

Read/Write at I/O Address 3DAh



Bits 0 and 3 have different meaning depending on the type of display selected.

0 Display Enable.
For CRT: A '1' indicates that the raster is in the retrace period.
For LCD: The behavior of this bit depends on the Status Control bit (RDF, 4). When the Status Control bit is cleared (0), the Display Enable bit toggles every sixteen character clocks. When the Status Control bit is set (1), Display Enable bit is active during the first 16 characters of each line and during all scanlines of rows 22 through the end of the panel in text modes (or row 85 through the end of the panel in graphics modes).

1 Light Pen Strobe. A '1' indicates that the Light Pen strobe has been set.

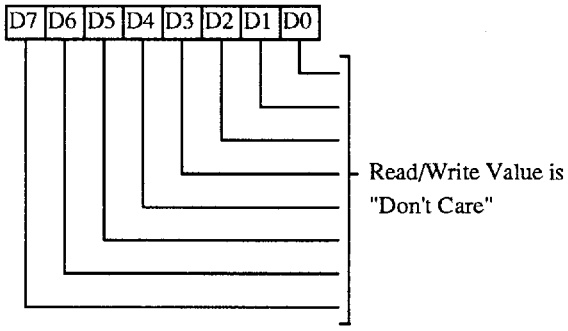
2 Reserved (0)

3 Vertical Sync.
For CRT: A '1' indicates that Vsync is active.
For LCD: The behavior of this bit depends on the Status Control bit (RDF, D4). When the Status Control bit is cleared (0), the Vertical Sync bit is active during the first scanline. When the Status Control bit is set (1), the Vertical Sync bit is active during all scanlines of row 24 in text modes or rows 93 through 96 (inclusive) in graphics modes.

7 - 4 Reserved (0)

CLEAR LIGHT PEN REGISTER

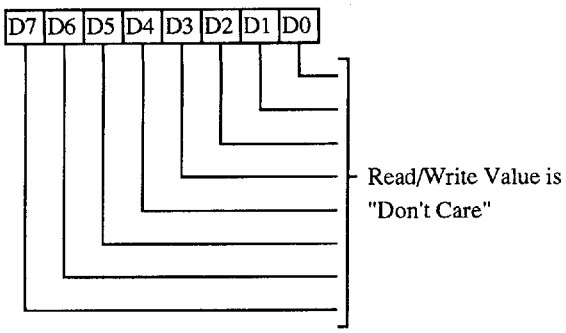
Read/Write at I/O Address 3DBh



7 - 0 Reading or writing this register clears the strobe to the light pen latch. It may be cleared before or after the value is read from the Light Pen registers (R10h, R11h).

SET LIGHT PEN REGISTER

Read/Write at I/O Address 3DCh



7 - 0 Reading or writing this register sets the light pen strobe, latching the current display memory address. This display memory address may be subsequently read through the Light Pen registers R10h and R11h. The Light Pen strobe must be explicitly reset by reading or writing the Clear Light Pen register (3DBh).

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82C425 Functional Description

CPU INTERFACE

In all CGA modes, I/O addresses are mapped to the 3Dx block of CPU I/O space. Display and font buffer memory is located at B8000-BBFFFh, for a total of 16 KBytes of memory space. CPU reads and writes of font memory are accomplished after overlaying it over the lower half of display memory (starting at B8000h); this is controlled by bit 1 of the Function Control register (RDF).

The 82C425 handles CPU read/write operations to display memory. The 82C425 interleaves CPU accesses with screen refresh accesses, ensuring rapid CPU transfers to/from display memory without screen "snow." The arbitration technique utilized does not limit CPU accesses to horizontal or vertical retrace periods. It relies on the PC bus RDY line to force the CPU to wait as necessary if a screen refresh is occurring since a refresh is higher priority than a CPU access. The CPU will typically wait for a period equal to one to four character clocks (dependent on the speed of the CPU). Figure 5 depicts connection of the 82C425 to the PC bus.

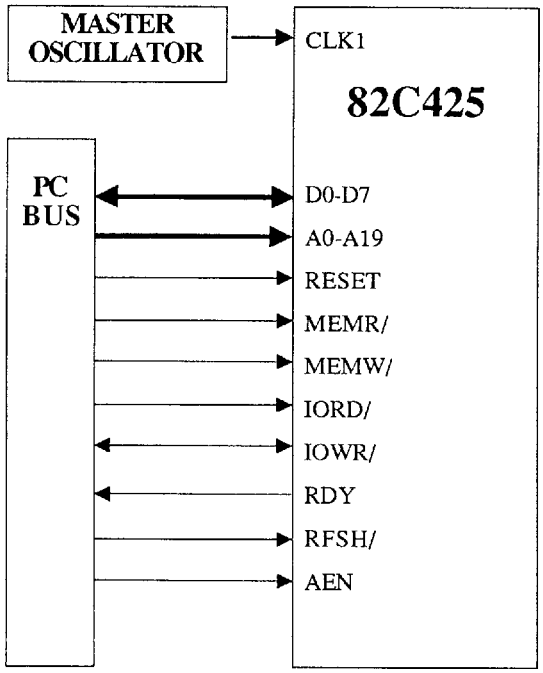
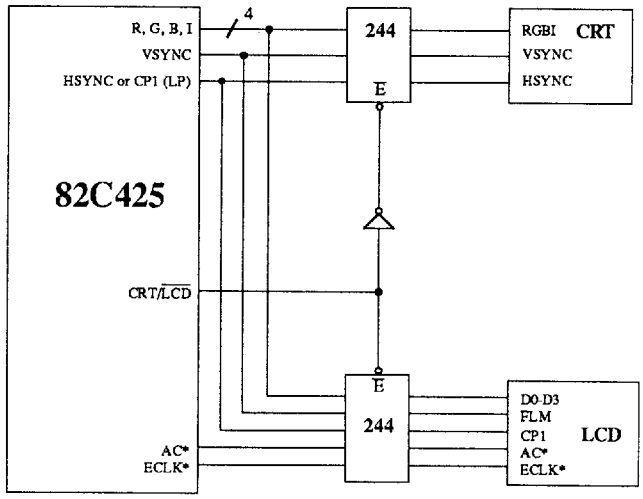


Figure 5: CPU Interface

DISPLAYS SUPPORTED

The 82C425 supports both CGA-compatible CRTs and Liquid Crystal Displays. Details of each are covered below. Only one display may be active at any one time. The display in use is reflected on the CRT/$\overline{\text{LCD}}$ output pin. Since different clocks may be required for each display, two clock inputs are provided (CLK1 and CLK2) along with a programmable divider used for generating the character clock from the selected clock input. Bit 5 in the Timing Control register (RDE) determines which clock input is used while bits 6 and 7 of this register determine the period of the character clock in master clock cycles.



*Note: The ECLK and AC Signals may not be required for some Liquid Crystal Display Panels.

Figure 6: 82C425 Connections to CRT and LCD Displays

Liquid Crystal Displays

When using an LCD, a single-panel, single-drive type is required. Panels with resolutions to 640 horizontal by 200 vertical are supported. Four bits of video data are supplied by the 82C425 as well as FLM and CP1 (or LP) control lines. For those panels requiring it, ECLK and AC signals are supplied. Figure 6 depicts the connection of the 82C425 to an LCD. The period of the ECLK signal is determined by the value in the Timing Control register (RDE). The gray scale techniques used when displaying colors on a monochrome panel are explained above.

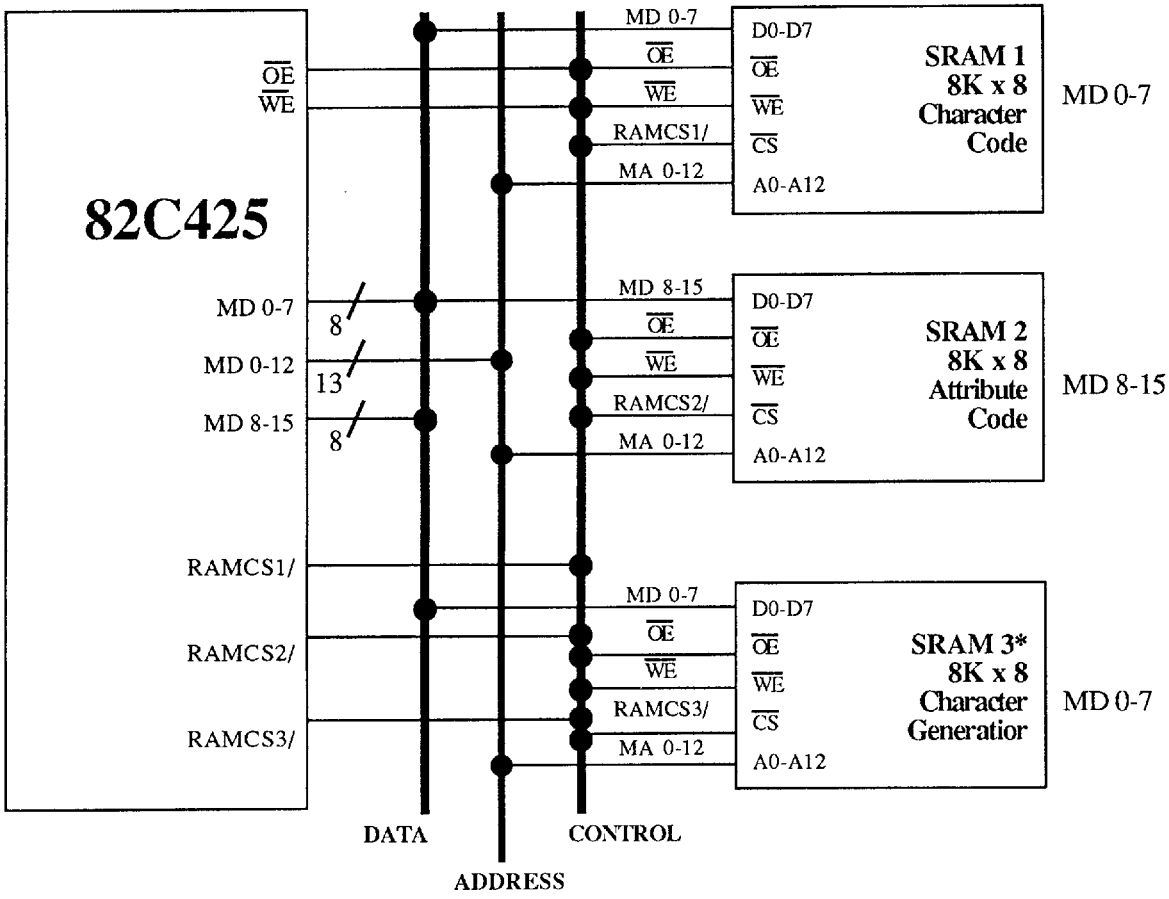
When driving an LCD panel, no pixel should be subjected to a non-zero average DC bias. If such a bias exists, vertical lines (ghosting) appear and the panel may be damaged over time. To avoid this problem and to compensate for variations in panels, an AC Control register (RD9) has been provided in the 82C425. The value programmed in bits 0-4 of this register should be odd and as large as possible since there are always an even number of lines in a panel. Determine the correct value for a particular panel through trial and error by looking for ghosting while programming specific values.

CRT Displays

IBM CGA-compatible CRTs are used with the 82C425. Variable-frequency displays as well as higher resolution fixed-frequency displays offering a CGA mode can be used. Four bits of video data are supplied by the 82C425 to the CRT display; these use TTL levels. Vertical and horizontal sync signals are also generated. Figure 6 depicts connection of the 82C425 to a CRT.

DISPLAY/FONT SRAM STORAGE

The 82C425 uses three 8Kx8 static CMOS RAM chips for display and font memory. Figure 7 depicts connection of these RAMs to the 82C425. The CGA display memory of 16 Kbytes uses two of these SRAMs while the font storage area uses the third. CPU access of font RAM is achieved by mapping it in or out of the display buffer address space with a bit in the Function Control register (RDF). This font RAM can be replaced with a ROM if downloadable fonts are not required. For applications requiring a single 8x8 font, one 2K ROM may be used.



*Note: This SRAM may be replaced by a ROM if programmable character sets are not required.

Figure 7: Interface of the 82C425 to SRAMs

Two separate fonts can be stored in the font RAM at one time. Each font defines a set of 256 characters which are drawn in a cell 8 dots wide by up to 16 dots high, character height being determined by the value programmed in the Maximum Scan register (R9). Thus each font requires a maximum of 4 Kbytes (16x256) of storage in the font RAM. The two fonts are stored sequentially, each in a 4 Kbyte segment of the RAM; the first block starts at the beginning display buffer address for CGA mode (B8000h) while the second font begins at B9000h.

Figure 8 shows the organization of data within the font RAM. Note that the first 8 scans (numbered 0 through 7) of each character are stored contiguously within the RAM. Scans 8 through 15 (if needed) are stored at addresses 2 Kbytes above scans 0 through 7. Characters are stored in ascending order beginning with character code 0.

The formulae below define the location of any scan line within the font RAM. In the formulae, A is equal to the address offset relative to the starting address of the display buffer:

FONT 0:

Scan Lines 0-7:

A = (Charcode x 8) + Scan Line

Scan Lines 8-15:

2048 + (Charcode x 8) + (Scan Line - 8)

FONT 1:

Scan Lines 0-7:

A = 4096 + (Charcode x 8) + Scan Line

Scan Lines 8-15:

6144 + (Charcode x 8) + (Scan Line - 8)

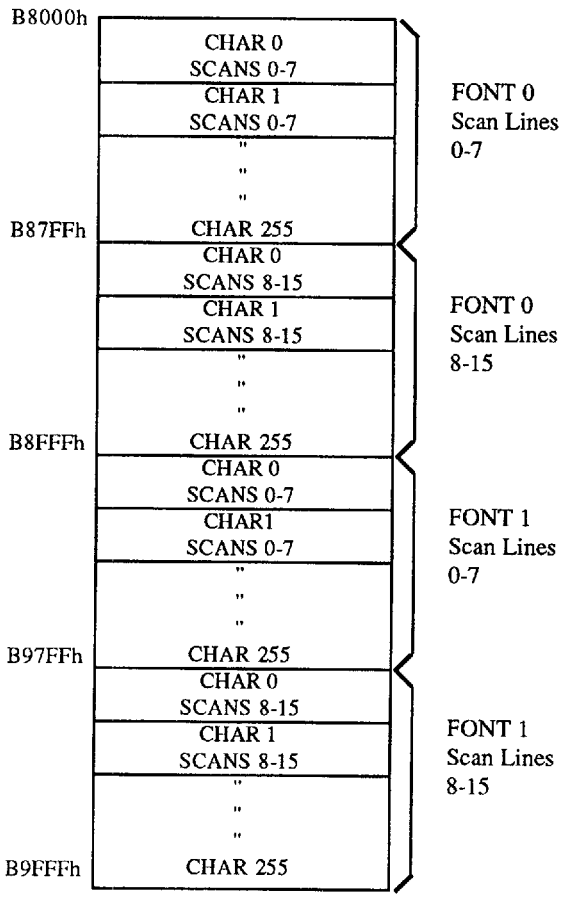


Figure 8: Font RAM Organization

USAGE NOTES

Users of the 82C425 should be aware of the concepts explained below.

Using the Cursor

The cursor blink rate is twice that of the character blink rate. Both the cursor blink rate and the character blink rate are controlled by bits 7-4 of the Vertical Sync Width/Blink Control register (RDD). This capability is provided so that LCD panels with different refresh rates can be accommodated.

To turn the cursor off, program the Cursor Start Scan register (RA) to a value greater than the Cursor End Scan (RB) register.

Using SMARTMAP

The SMARTMAP technique, when invoked, ensures legibility of CGA text on LCD panels. SMARTMAP is enabled by programming a non-zero value in the Threshold register (RDAh). Once enabled, SMARTMAP will automatically adjust foreground and background values in text modes but will have no effect in graphics modes.

When enabled, SMARTMAP, on a character by character basis, continuously monitors the foreground and background values to ensure a minimum contrast level on LCD panels. This minimum contrast is determined by the Threshold register (RDAh). If this minimum criteria is not met, the foreground and background values are appropriately adjusted using the values stored in the Shift Parameter register (RDBh). If the adjusted values exceed the maximum allowed values, the Saturation bit (bit 4 in RDAh) determines if the output is limited to the saturation point or allowed to wrap around. The resulting value is then adjusted to a four or eight gray scale output, depending on the programmed value of RDAh, bit 5. Threshold and Shift Parameter values should be determined experimentally for each manufacturer's LCD panel model.

SMARTMAP Usage Notes:

1. If the Blink attribute is enabled, the background intensity bit (AT7) is forced to zero before the SMARTMAP algorithm is applied.
2. If the Alternate Font Select Function is enabled, the foreground color intensity bit (AT3) is forced to zero before applying the SMARTMAP algorithm.

82C425 Electrical Specifications

82C425 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	–	7	V
V_I	Input Voltage	-0.5	V_{DD}+0.5	V
V_O	Output Voltage	-0.5	V_{DD}+0.5	V
T_{OP}	Operating Temperature (Ambient)	-25	85	°C
T_{STG}	Storage Temperature	-40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C425 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	4.5	5.5	V
T_A	Ambient Temperature	-40	70	°C

82C425 DC CHARACTERISTICS

(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
V_{IL}	Input Low Voltage		–	0.8	V
V_{IH}	Input High Voltage	(All pins except CLK1, CLK2, MD15:0)	2.0	–	V
V_{IH}	Input High Voltage	(CLK1 and CLK2)	2.8	–	V
V_{IH}	Input High Voltage	(MD15:0)	3.5	–	V
V_{OL}	Output Low Voltage		–	0.45	V
V_{OH}	Output High Voltage		2.4	–	V
I_{OL}	Output Low Current	(All pins except D0-D7, RDY, PCLK, ECLK,	–	+4	mA
		HSYNC, VSYNC, AC, CRT/$\overline{\text{LCD}}$)			
I_{OL}	Output Low Current	(D0-D7, RDY, PCLK, ECLK, HSYNC, VSYNC,	–	+8	mA
		AC, CRT/$\overline{\text{LCD}}$)			
I_{OH}	Output High Current	(All pins except D0-D7, RDY, PCLK, ECLK,	–	-4	mA
		HSYNC, VSYNC, AC, CRT/$\overline{\text{LCD}}$)			
I_{OH}	Output High Current	(D0-D7, RDY, PCLK, ECLK, HSYNC, VSYNC,	–	-8	mA
		AC, CRT/$\overline{\text{LCD}}$)			
I_{IL}	Input Leakage Current		-100	+100	µA

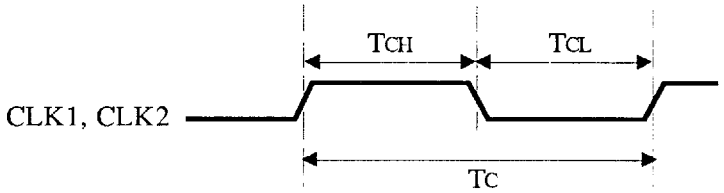
82C425 DC CHARACTERISTICS, *Continued*

(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC}	Active Power Supply Current	@ 14.3 MHz CLK, 0°C	–	15	mA
I_{CC}	Active Power Supply Current	Clocks Stopped	–	100	µA
I_{OZ}	Output High Impedance Leakage	0.45 <VPIN <VDD	-100	+100	µA

82C425 AC TIMING CHARACTERISTICS - CLOCK TIMING

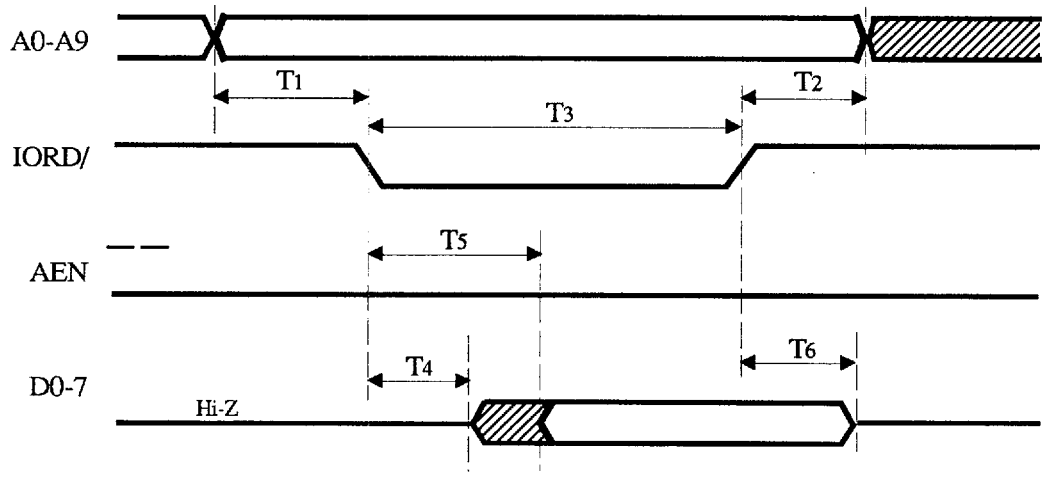
Symbol	Parameter	Min	Max	Units
T_C	CLK1, 2 Period	50	–	ns
T_{CH}	CLK1, 2 High Time	25	–	ns
T_{CL}	CLK1, 2 Low Time	25	–	ns



82C425 CLKIN Timing

82C425 I/O BUS TIMING - I/O READ CYCLE TIMING

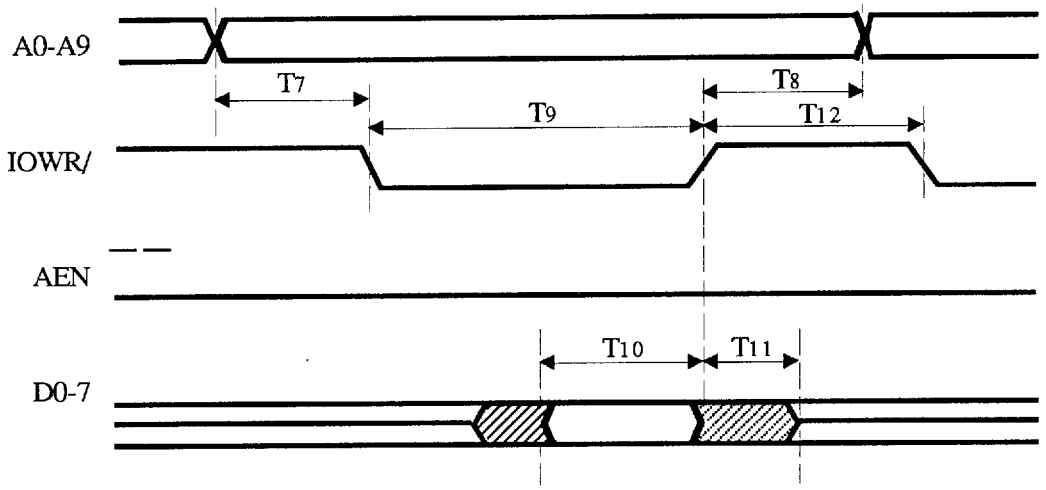
Symbol	Parameter		Min	Max	Units
T_1	Address setup to IORD/ (I/O Read)		25	–	ns
T_2	Address hold from IORD/ (I/O Read)		0	–	ns
T_3	IORD/ Pulse Width		100	–	ns
T_4	Valid data delay from IORD/		–	40	ns
T_5	Data Three-State from IORD/		–	25	ns



82C425 I/O Read Cycle

82C425 I/O BUS TIMING - I/O WRITE CYCLE TIMING

Symbol	Parameter		Min	Max	Units
T_7	Address setup to IOWR/ (I/O Write)		25	–	ns
T_8	Address hold from IOWR/ (I/O Write)		0	–	ns
T_9	IOW R/ Pulse Width		100	–	ns
T_{10}	Data Setup to IOWR/		40	–	ns
T_{11}	Data Hold from IOWR/		0	–	ns
T_{12}	Write Recovery Time		60	–	ns

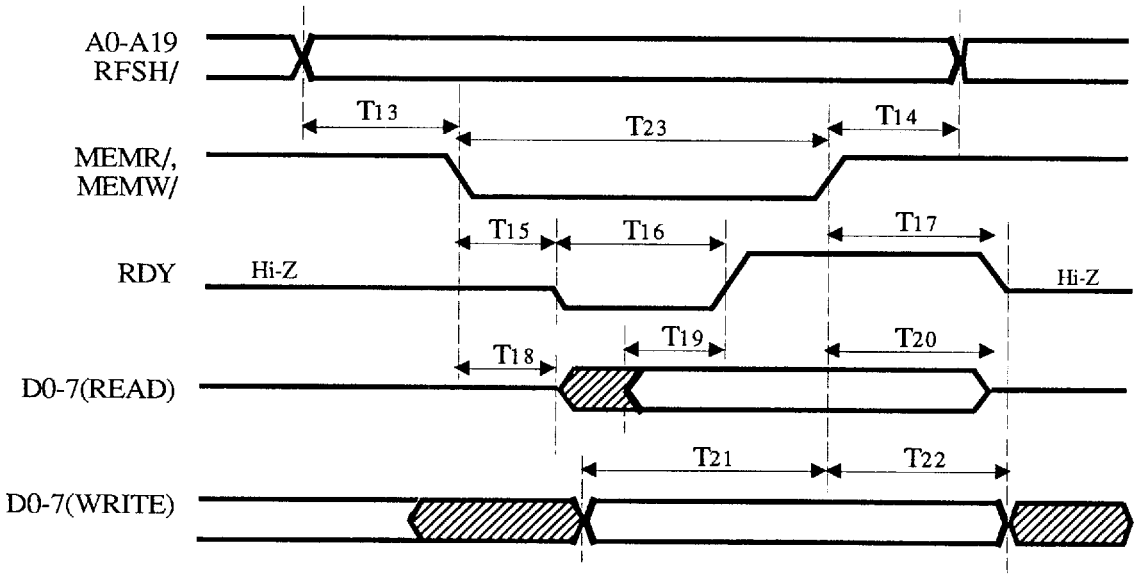


82C425 I/O Write Cycle

T-52-33-45

82C425 I/O BUS TIMING - MEMORY READ/WRITE CYCLE TIMINGS

Symbol	Parameter		Min	Max	Units
T_{13}	Memory Address setup to MEMR/, MEMW/		25	–	ns
T_{14}	Memory Address hold form MEMR/, MEMW/		0	–	ns
T_{15}	MEMR/, MEMW/ to RDY Low delay		–	25	ns
T_{16}	RDY Width		$4T_C$	$12T_C$	ns
T_{17}	RDY Inactive Delay		–	25	ns
T_{18}	READ Data Active delay		–	20	ns
T_{19}	Memory Read Data setup to RDY		0		ns
T_{20}	Memory Read Data hold from MEMR/		5	30	ns
T_{21}	Memory Write Data setup to MEMW/		$2T_C$	–	ns
T_{22}	Memory Write Data hold from MEMW/		0	–	ns
T_{23}	MEMR/, MEMW/ Pulse Width		100	–	ns



82C425 CPU Read/Write Cycle

82C425 AC TIMING CHARACTERISTICS - VIDEO TIMING

Symbol	Parameter	Min	Typ	Max	Units
T_{24}	DOUT Delay	–	-20	20	ns
T_{25}	LP Delay (1)	–	-20	20	ns
T_{26}	ECLK Delay	–	T_C-20	T_C+20	ns
T_{27}	LP to AC Delay	–	-20	20	ns
T_{PCLK}	PCLK Period (2)	–	–	–	ns
T_{28}	FLM Setup Time (3)	Tchar	–	–	ns
T_{29}	FLM Hold Time	Tchar	–	–	ns

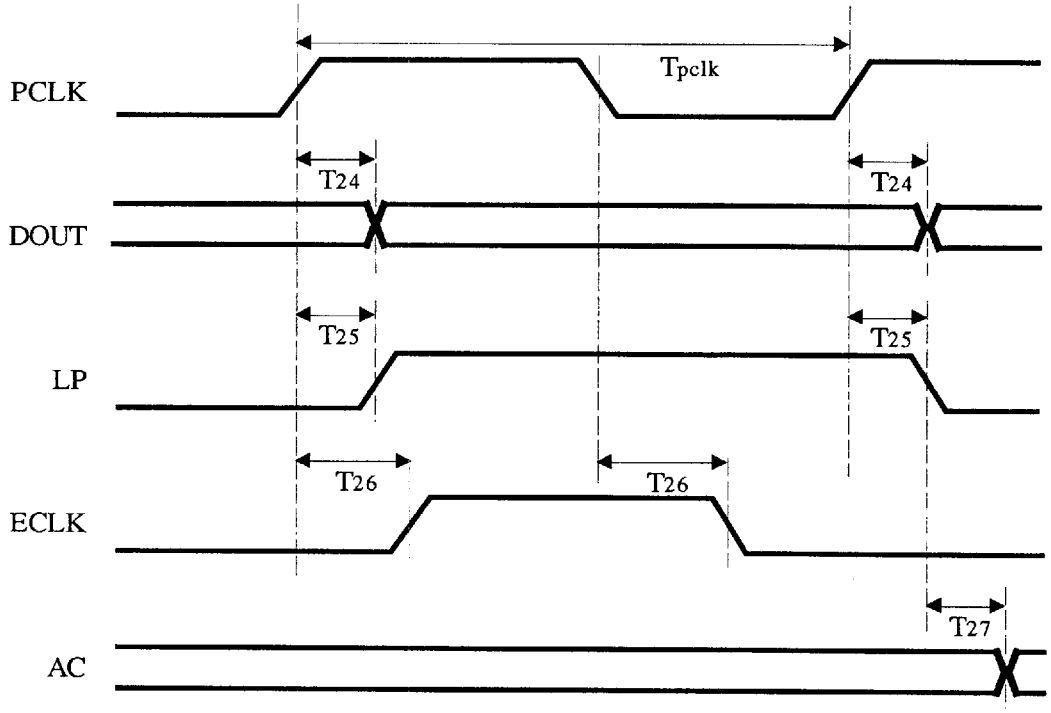
Notes: **1.** LP is active only during output of the last video data for each scan line.

2. Tpclk = (4, 8, 12, or 16)x Tc, as programmed by the character clock divider field in the Timing Control Register (RDE).

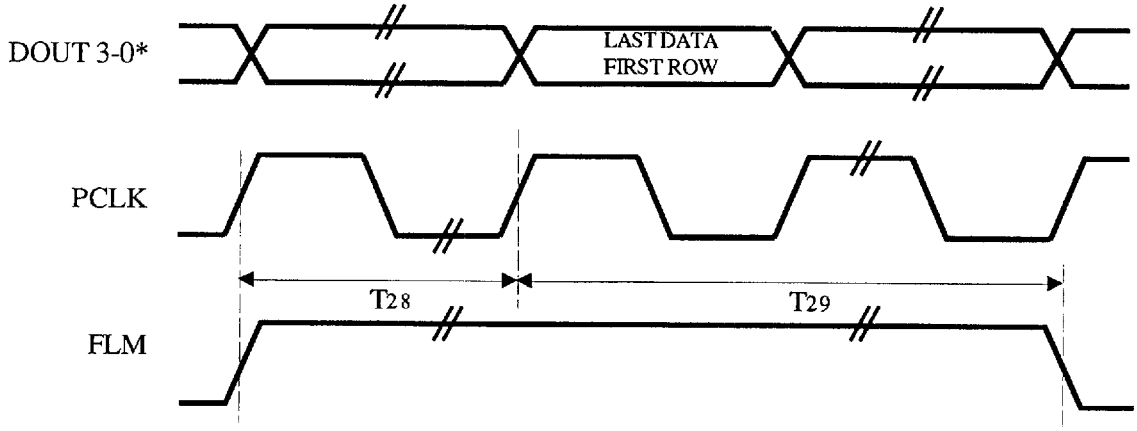
3. The period of Tchar varies with the type of mode selected as follows:

Period of the Character Clock in Each Mode

Mode	80 x 25 Text	40 x 25 Text	640 x 200 Graphics	320 x 200 Graphics
Tchar	2 Tpclk	4 Tpclk	2 Tpclk	2 Tpclk



82C425 LCD Video Timing



*NOTE: DOUT3 is the left-most pixel for monochrome panels.

82C425 FLM Detail

T-52-33-45

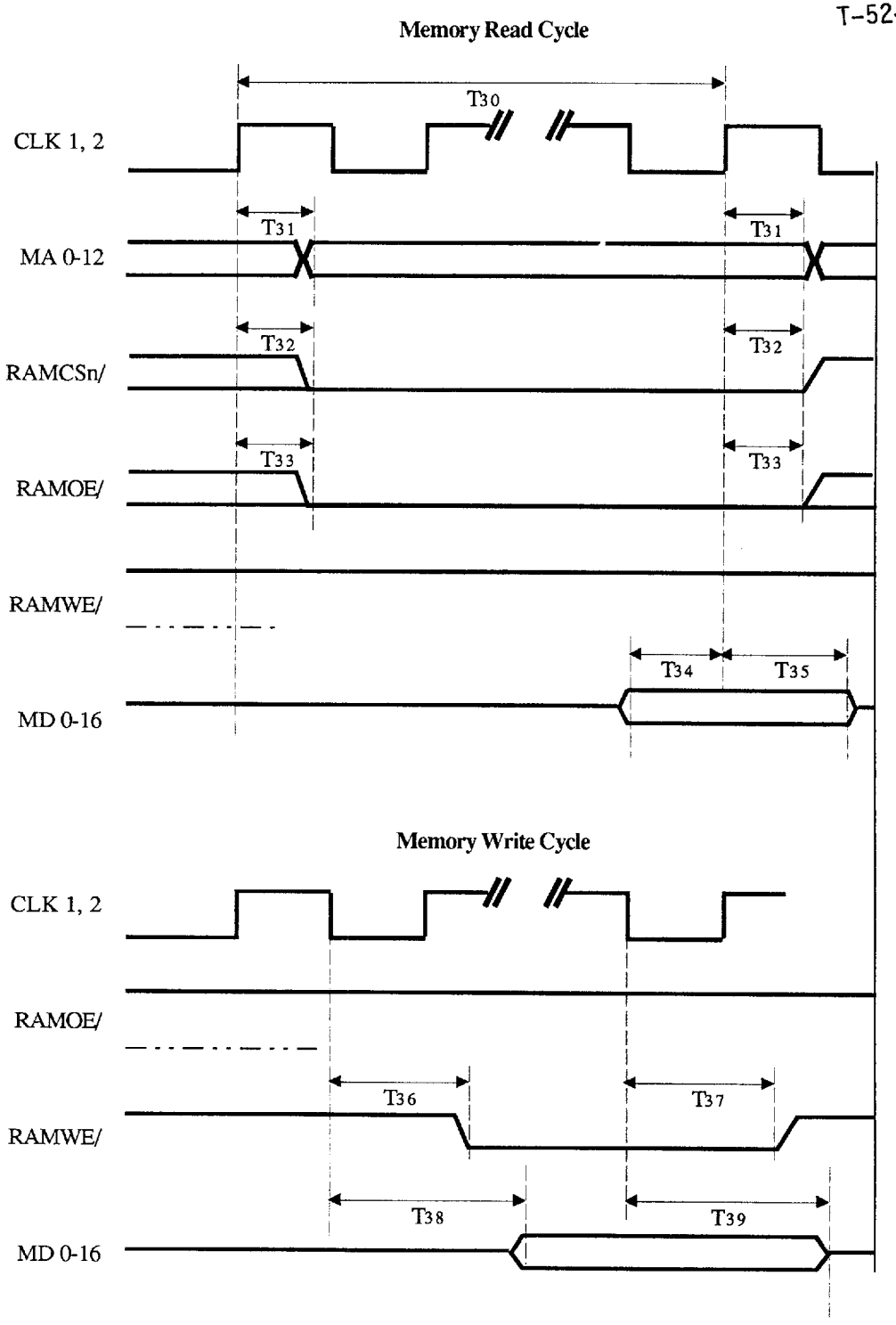
82C425 AC TIMING CHARACTERISTICS - SRAM INTERFACE TIMING

Symbol	Parameter	Min	Max	Units
T_{30}	Read/Write Cycle Time	$2T_C$ or $3T_C$ (2)	$2T_C$ or $3T_C$ (2)	ns
T_{31}	Address Delay Time	10	25	ns
T_{32}	Chip Select Delay Time	10	25	ns
T_{33}	Output Enable Delay Time	10	25	ns
T_{34}	Read Data Setup Time	–	-10(1)	ns
T_{35}	Read Data Hold Time	–	25(1)	ns
T_{36}	Write Enable Active Delay Time	–	25	ns
T_{37}	Write Enable Inactive Delay Time	–	25	ns
T_{38}	Write Data Valid Delay	–	30	ns
T_{39}	Write Data Valid Hold Time	20	–	ns

Notes: **1.** These parameters indicate that the data must be valid from 10ns following until 25ns following the rising edge of the input clock.

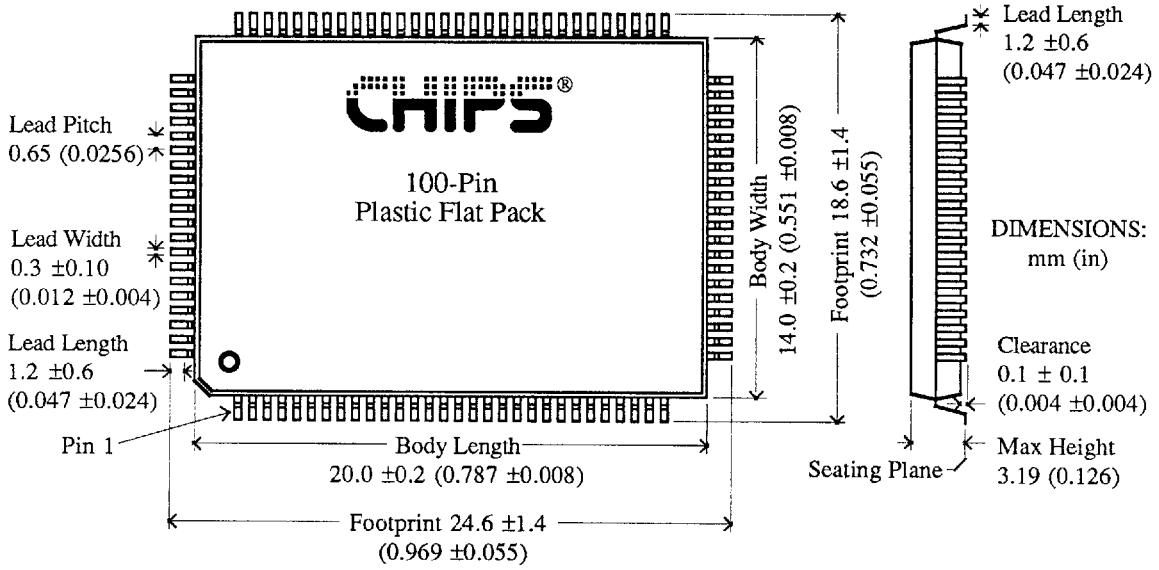
2. Accesses to character and attribute memory are 3Tc long, requiring memory with an access time of (3Tc - 15ns) or less. Font memory accesses are also 3Tc long except for the following case in which the memory cycle is 2Tc long: font read cycles in 80 column text mode when there are 8 master clocks per character clock (both bits 6 and 7 of register RDE = 0). In this case, the font memory must be capable of a 2Tc - 15ns access time.

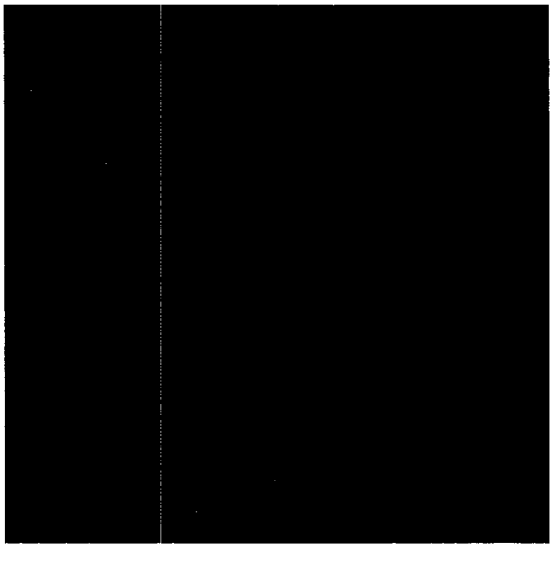
T-52-33-45



82C425 SRAM Interface Timing

82C425 Mechanical Specifications





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