

STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT NAME	Synchronous DC/DC converter controller
TYPE	<b>BD9040FV</b>
FEATURES	<ul style="list-style-type: none"> <li>•Wide Input Range</li> <li>•High Precision Reference Voltage</li> <li>•Built-in over current , output short and over voltage protect with Timer latch.</li> <li>•Adjustable Frequency</li> <li>•Available use ceramic capacitor.</li> </ul>

### ●ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
VCC Voltage*	V <sub>CC</sub>	20	V
EN Input Voltage	V <sub>EN</sub>	20	V
SW Voltage	V <sub>SW</sub>	V <sub>CC</sub>	V
BOOT-SW Voltage	V <sub>BOOT</sub>	6	V
Power Dissipation**	P <sub>d</sub>	0.81*	W
Operating Temperature Range	T <sub>opr</sub>	-40~+85	°C
Storage Temperature Range	T <sub>stg</sub>	-55~+150	°C
Maximum Junction Temperature	T <sub>jmax</sub>	150	°C

\*1 Do not however exceed P<sub>d</sub>.

\*\* \*2 P<sub>d</sub> derated at 6.45mW/°C for temperature above Ta=25°C, Mounted on PCB 70mm×70mm×1.6mm.

### ●OPERATING CONDITIONS (Ta=-40°C~+85°C)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Supply Voltage ***	V <sub>CC</sub>	4.5	12	18	V
RT resistor	RT	39	—	130	kΩ
Oscillator Frequency	f <sub>osc</sub>	200	—	750	kHz

\*\*\* In case of using less than 6V, short to VCC and VREG5.

\* This product is not designed for normal operation within a radio active environment.

Status of this document

The Japanese version of this document is the formal specification.

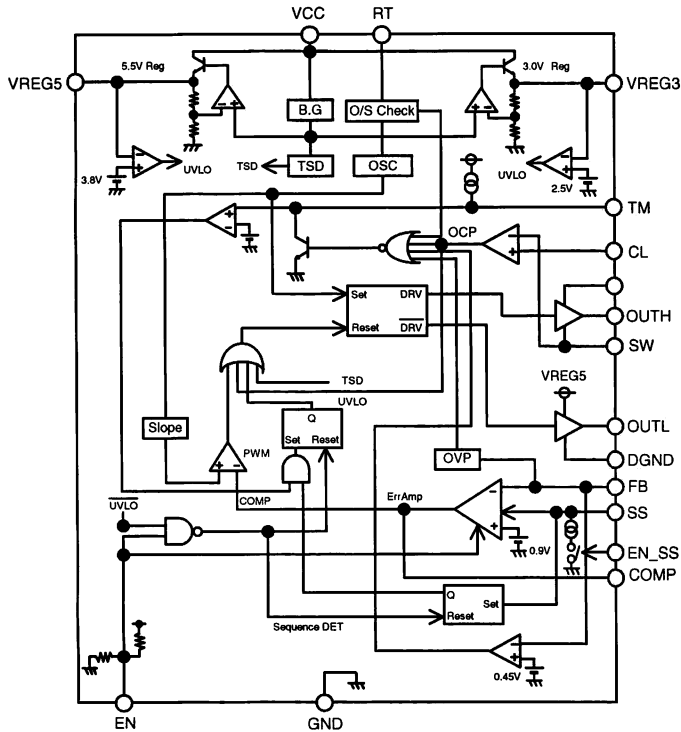
A customer may use this translation version only for a reference to help reading the formal version.

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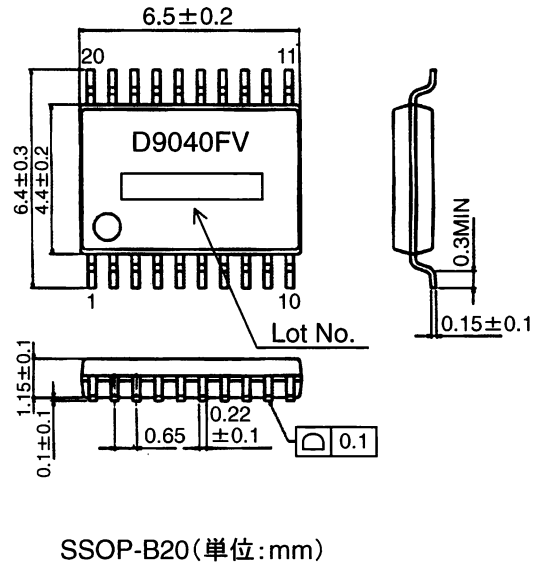
○ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C VCC=12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VCC Bias Current	ICC	-	3	6	mA	
Stand-by Current	ISTB	-	430	860	μA	V <sub>EN</sub> =0V
[VREG5]						
Output Voltage	VREG5	5	5.5	6	V	
Load Regulation	VREG5_L	-	20	50	mV	I <sub>VREG5</sub> =0 to 6mA
[VREG3]						
Output Voltage	VREG3	2.85	3.0	3.15	V	
Load Regulation	VREG3_L	-	10	20	mV	I <sub>VREG3</sub> =0 to 1mA
[Under Voltage Lock Out]						
VREG5 Threshold Voltage	VREG5_UVLO	3.4	3.8	4.2	V	V <sub>REG5</sub> :Sweep down
VREG3 Threshold Voltage	VREG3_UVLO	2.4	2.5	2.6	V	V <sub>REG3</sub> :Sweep down
[Oscillator Section]						
Oscillator Frequency	FOSC	240	300	360	kHz	RT=91 kΩ
[Error Amp]						
VO Bias Current	I <sub>vo+</sub>	-	-	1	μA	
Comp Source Current	I <sub>source</sub>	-12	-6.5	-2	mA	V <sub>FB</sub> =1.1V
Comp Sink Current	I <sub>sink</sub>	-0.75	-1.5	5	mA	V <sub>FB</sub> =0.7V
Reference Voltage	VOB	0.891	0.900	0.909	V	FB-COMP Short
Output Short Threshold	V <sub>osh</sub>	0.37	0.45	0.53	V	V <sub>FB</sub> :Sweep down
Hysteresis Voltage	ΔV <sub>osh</sub>	22	45	90	mV	V <sub>FB</sub> :Sweep up
[Soft Start]						
Charging Current	I <sub>SS</sub>	-14	-10	-6	μA	V <sub>SS</sub> =1V
Discharging Current	I <sub>DIS</sub>	0.6	1.7	5	mA	V <sub>SS</sub> =1V
Discharging Current2	I <sub>DIS2</sub>	2.35	3.3	4.62		V <sub>SS</sub> =1V, V <sub>EN_SS</sub> =0V
Maximum Voltage	V <sub>SS_MAX</sub>	1.75	1.95	2.15	V	
Stand-by Voltage	V <sub>SS_STB</sub>	-	-	0.3	V	
[Over Current Protect]						
CL Input Current	I <sub>swin</sub>	9	10	11	μA	V <sub>CL</sub> =V <sub>CC</sub> -0.2V
[Over Voltage Protect]						
Threshold Voltage	V <sub>ovp</sub>	1.06	1.1	1.14	V	
[Timer latch]						
Charging Current	I <sub>TM</sub>	-14	-10	-6	μA	V <sub>TM</sub> =1V
Threshold Voltage	V <sub>th_TM</sub>	0.9	1	1.1	V	
TM Sink Current	I <sub>OFFS</sub>	0.6	1.7	5	mA	V <sub>TM</sub> =0.5V
[CTL]						
EN Pull-up Resistor	R <sub>EN</sub>	150	300	450	kΩ	
EN_SS Pull-up Resistor	R <sub>EN_SS</sub>	150	300	450	kΩ	

○BLOCK DIAGRAM



○PHYSICAL DIMENSIONS・MARKING



○Pin No. ・ Pin Name

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	EN_SS	SS Discharge Delay ON/OFF Control	11	VCC	Power Input
2	RT	Connect to External Resistor Setting Operating Frequency	12	N.C	Non Connect
3	TM	Timer Latch Setting Terminal By External Capacitor	13	N.C	Non Connect
4	SS	Soft Start	14	VREG5	5V Regulator Output
5	COMP	Error Amp Output	15	OUTL	Low Side FET Gate Drive
6	FB	Error Amp Inverting Input	16	DGND	Low Side FET Source
7	EN	Control Voltage Input	17	SW	High Side FET Source
8	N.C	Non Connect	18	OUTH	High Side FET Gate Driver
9	VREG3	Regulator Output	19	BOOT	OUTH1 Driver Supply Input
10	GND	Ground	20	CL	OCP Setting terminal By External Resistance

## NOTES FOR USE

1. Absolute maximum range  
Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed we cannot be defined the failure mode, such as short mode or open mode.  
Therefore physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.
2. GND pin voltage  
GND terminal should be connected the lowest voltage, under all conditions. And all terminals except SW should be under GND terminal voltage under all conditions including transient situations. If a terminal exists under GND, it should be inserting a bypass route.
3. Power dissipation  
If IC is used on condition that the power loss is over the power dissipation, the reliability will become worse by heat up, such as reduced output current capability.  
Also, be sure to use this IC within a power dissipation range allowing enough of margin.
4. Input supply voltage  
Input supply pattern layout should be as short as possible.
5. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.
6. Thermal Shut Down Circuit  
A temperature control is built in the IC to prevent the damage due to overheat. Therefore, the output is turned off when the thermal circuit works and are turned on when the temperature goes down to the specified level.
7. Mounting Failures  
Mounting failure, such as misdirection or mount's error, may cause a malfunction in the device.
8. Internal circuits or elements may be damaged when Vcc and pin voltage are reversed. For example, Vcc short circuit to GND while a external capacitor is charged. Pin capacitors of Vreg5 and VREG3 output are recommended 1  $\mu$ F and 0.1  $\mu$ F . In addition, inserting a Vcc series countercurrent prevention diode, or a bypass diode between the various pins and the Vcc, is recommended.
9. Malfunction may be happened when the device is used in the strong electromagnetic field.
10. We recommend to put Diode for protection purpose in case of output pin connected with large load of impedance or reserve current occurred at initial and output off.
11. Precautions for board inspection  
Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the test operation.  
To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.
12. GND pattern  
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point ) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid voltage fluctuations in any connected external component GND.
13. SW Terminal  
A counter-electromotive force may generate a negative potential at the SW terminal during connection to the particular application. Therefore, it should be inserting a bypass route between SW to GND.
14. Output Load  
When EN is Low, UVLO active and timer latch active, SW terminal output a few current .  
In case of output load is less than 1mA in Application, output should be connected under 1k $\Omega$  resistor to GND.

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