ANALOG DEVICES

500 MHz, 32 x 32 Buffered Video Crosspoint Switch

Preliminary Technical Data

AD8117/AD8118

FEATURES

Large, 32 x 32 High Speed, Nonblocking Switch Array
G = 1 (AD8117) or G = 2 (AD8118) Operation
Differential or Single-Ended Operation
Single +5 V supply, or dual ± 2.5 V supply
Serial or Parallel Programming of Switch Array
High impedance output disable allows connection of multiple devices with minimal output bus load
Excellent Video Performance
- **100 MHz 0.1 dB Gain Flatness**
- **0.1% Differential Gain Error (R_L = 150 Ω)**
- **0.1° Differential Phase Error (R_L = 150 Ω)**

Excellent AC Performance
- **Bandwidth: >500 MHz**
- **Slew rate: 1,800 V/µs**

Low power of 2.5 W
Low all hostile crosstalk:
- **-75 dB @ 5 MHz**
- **-40 dB @ 500 MHz**

Reset pin allows disabling of all outputs
- **(Connected through a capacitor to ground provides power-on reset capability)**

304 ball SBGA package (31 mm × 31 mm)

APPLICATIONS

Routing of high speed signals including:
- **RGB and component video routing**
- **Compressed video (MPEG, Wavelet)**
- **Data communications**

FUNCTIONAL BLOCK DIAGRAM

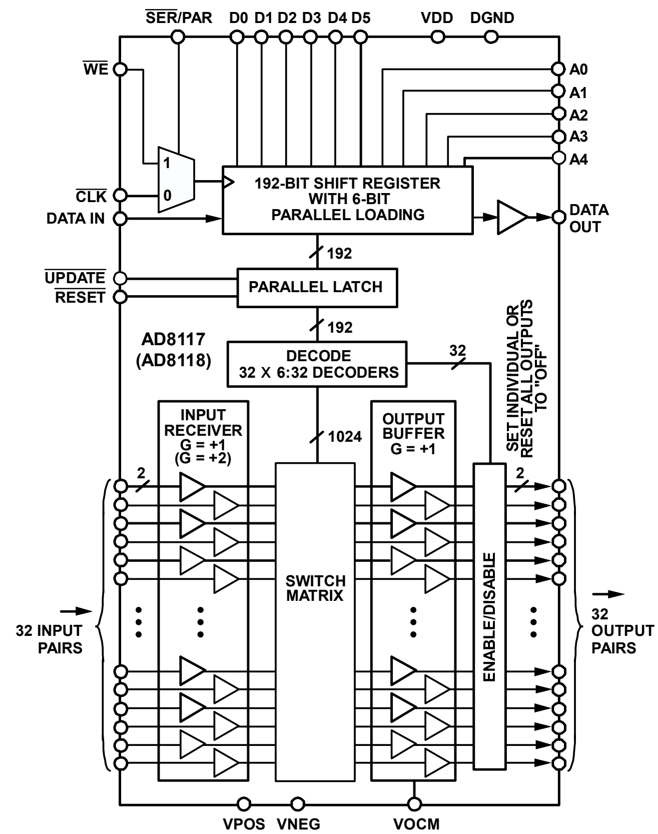

Figure 1. AD8117 G = +1

PRODUCT DESCRIPTION

The AD8117/AD8118 is a high speed 32 × 32 video crosspoint switch matrix. It offers a 500 MHz bandwidth and slew rate of 1800 V/µs for high resolution computer graphics (RGB) signal switching. With −75 dB of crosstalk and −100 dB isolation (@ 5 MHz), the AD8117 is useful in many high-speed applications. The 0.1 dB flatness out to 100 MHz makes the AD8117 ideal for composite video switching.

The AD8117's 32 independent output buffers can be placed into a high impedance state for paralleling crosspoint outputs so that off-channels present minimal loading to an output bus. The AD8117 is available in gain of 1 or 2 (AD8118) for ease of use in back-terminated load applications. It operates as a fully differential device or can be configured for single-ended operation. Either a single +5 V supply, or dual ± 2.5 V supplies can be used while consuming only 500 mA of idle current with all outputs enabled. The channel switching is performed via a double-buffered, serial digital control (which can accommodate daisy chaining of several devices) or via a parallel control allowing updating of an individual output without reprogramming the entire array.

The AD8117/AD8118 is packaged in a 304 Ball BGA package and is available over the extended industrial temperature range of −40°C to +85°C.

Rev. PrA

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REVISION HISTORY

Revision PrA: Preliminary Datasheet

AD8117 SPECIFICATIONS

V_S = ± 2.5 V at T_A = 25°C, G = +1, R_L = 100 Ω, Differential I/O mode, unless otherwise noted.

Table 1. AD8117ABPZ

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB bandwidth	200 mV p-p, R_L = 100 Ω		>500		MHz
	2 V p-p, R_L = 100 Ω		>420		MHz
Gain flatness	0.1 dB, 200 mV p-p, R_L = 100 Ω		100		MHz
	0.1 dB, 2 V p-p, R_L = 100 Ω		70		MHz
Propagation delay	2 V p-p, R_L =100 Ω		1.3		ns
Settling time	1% , 2 V step, R_L = 100 Ω		2.5		ns
Slew rate	2 V Step, R_L = 100 Ω, peak		1,800		V/μs
	2 V Step, R_L = 100 Ω, 10-90%		1,500		V/μs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL, R_L = 150 Ω or R_L = 1kΩ		0.1		%
Differential Phase Error	NTSC or PAL, R_L = 150 Ω or R_L = 1kΩ		0.1		Degrees
Crosstalk, all hostile	f = 5 MHz		−75		dB
	f = 10 MHz		−70		dB
	f = 100 MHz		−50		dB
	f = 500 MHz		−40		dB
Off isolation, input-output	f = 10 MHz, R_L = 100 Ω, one channel		−100		dB
Input Voltage Noise	0.01 MHz to 50 MHz		45		nV/√Hz
DC PERFORMANCE					
Gain Error	R_L = 100 Ω or 150 Ω		1	2	%
Gain Matching	No Load, Channel-Channel		0.5	1	%
	R_L = 100 Ω, Channel-Channel		0.5	1	%
OUTPUT CHARACTERISTICS					
Output impedance	DC, Enabled		0.1		Ω
	Disabled, differential		30		kΩ
Output disable capacitance	Disabled		2		pF
Output leakage current	Disabled		1		μA
Output voltage range	No Load			2	V p-p
INPUT CHARACTERISTICS					
Input offset voltage	Differential		10		mV
Input Voltage Range - Common Mode			4		V p-p
Input Voltage Range - Differential Mode			2		V p-p
Common-mode rejection ratio	f = 10 MHz		−48		dB
Input capacitance	Any switch configuration		2		pF
Input resistance	Differential		5		kΩ
Input bias current			3		μA
SWITCHING CHARACTERISTICS					
Enable on time	50% update to 1% settling		200		ns
Switching time, 2 V step	50% settling		20		ns
Switching transient (glitch)	Differential		40		mV p-p

POWER SUPPLIES					
Supply current	V_{POS}, outputs enabled, no load		500		mA
	Outputs disabled		210		mA
	V_{NEG}, outputs enabled, no load		500		mA
	Outputs disabled		220		mA
	D_{VDD}, outputs enabled, no load			1	mA
Supply voltage range			4.5 to 5.5		V
PSRR	V_{NEG}, V_{POS}, f = 1 MHz		−85		dB
	V_{OCM}, f = 1 MHz		−75		dB
OPERATING TEMPERATURE RANGE					
Temperature range	Operating (still air)		−40 to +85		°C
θ_{JA}	Operating (still air)		15		°C/W

TIMING CHARACTERISTICS (SERIAL MODE)

Parameter	Symbol	Limit Min	Typ	Max	Unit
Serial Data Setup Time	t_1				ns
CLK Pulsewidth	t_2				ns
Serial Data Hold Time	t_3				ns
CLK Pulse Separation	t_4				ns
CLK to UPDATE Delay	t_5				ns
UPDATE Pulsewidth	t_6				ns
CLK to DATA OUT Valid	t_7				ns
Propagation Delay, UPDATE to Switch On or Off					ns
Data Load Time, CLK = 5 MHz, Serial Mode					µs
CLK, UPDATE Rise and Fall Times					ns
RESET Time					ns

Specifications subject to change without notice.

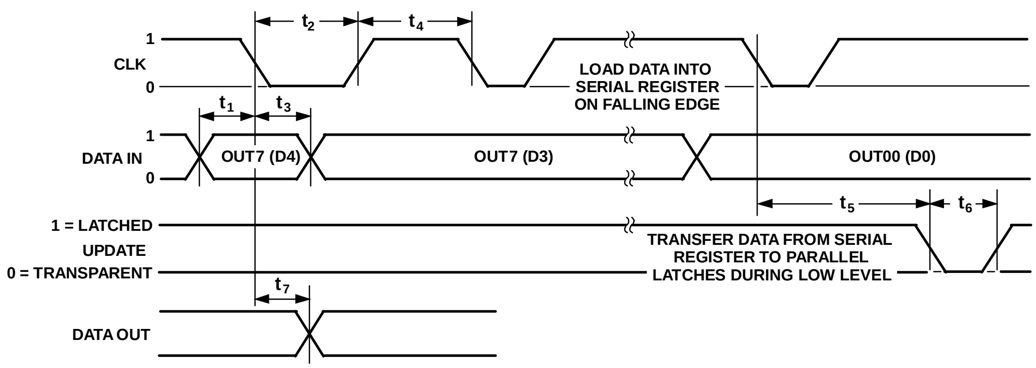


Figure 2. Timing Diagram, Serial Mode

Table 2. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
RESET, SERPAR, CLK, DATA IN, UPDATE	RESET, SERPAR, CLK, DATA IN, UPDATE	DATA OUT	DATA OUT	RESET, SERPAR, CLK, DATA IN, UPDATE	RESET, SERPAR, CLK, DATA IN, UPDATE	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	–400 µA max	–400 µA max	1 mA min

TIMING CHARACTERISTICS (PARALLEL MODE)

Parameter	Symbol	Limit Min	Typ	Max	Unit
Parallel Data Setup Time	t_1				ns
WE Pulsewidth	t_2				ns
Parallel Data Hold Time	t_3				ns
WE Pulse Separation	t_4				ns
WE to UPDATE Delay	t_5				ns
UPDATE Pulsewidth	t_6				ns
Propagation Delay, UPDATE to Switch On or Off					ns
WE, UPDATE Rise and Fall Times					ns
RESET Time					ns

Specifications subject to change without notice.

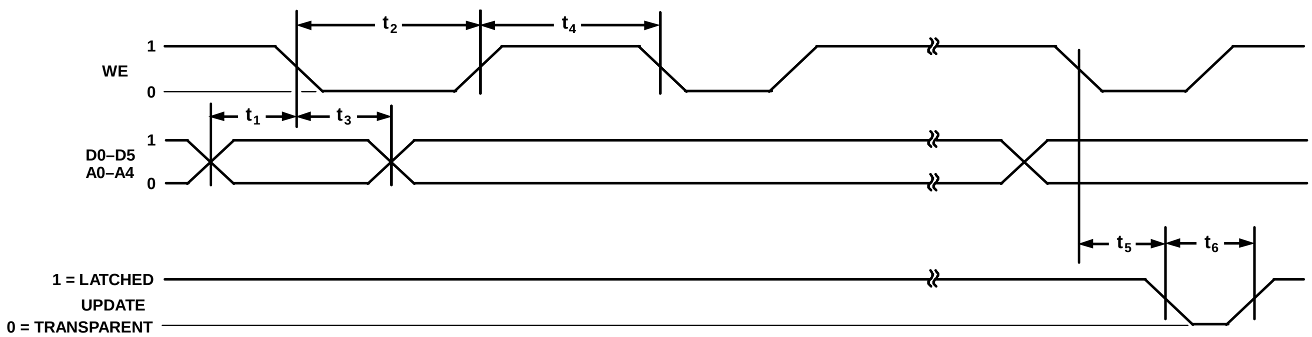


Figure 3. Timing Diagram, Parallel Mode

Table 3. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
RESET, SERPAR, WE, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, A4, UPDATE	RESET, SERPAR, WE, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, A4, UPDATE	DATA OUT	DATA OUT	RESET, SERPAR, WE, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, A4, UPDATE	RESET, SERPAR, WE, D0, D1, D2, D3, D4, D5, A0, A1, A2, A3, A4, UPDATE	DATA OUT	DATA OUT
2.0 V min	0.8 V max	*disabled*	*disabled*	20 µA max	–400 µA max	*disabled*	*disabled*

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Supply Voltage (V_{POS} – V_{NEG})	+6 V
Digital Supply Voltage (V_{DD} – D_{GND})	+6 V
Ground potential difference (V_{NEG} – D_{GND})	+0.5 V to −2.5 V
Maximum potential difference (V_{DD} – V_{NEG})	+6 V
Common-Mode Analog Input Voltage	(V_{NEG} – 0.5 V) to (V_{POS} + 0.5 V)
Differential Analog Input Voltage	± 2 V
Digital Input Voltage	VDD
Output Voltage (Disabled Analog Output)	(V_{POS} – 1 V) to (V_{NEG} + 1 V)
Output Short-Circuit Duration	Momentary
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

NOTE
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
BGA	15		°C/W

POWER DISSIPATION

The AD8117/AD8118 are operated with ±2.5 V or +5 V supplies and can drive loads down to 100 Ω, resulting in a large range of possible power dissipations. For this reason, extra care must be taken derating the operating conditions based on ambient temperature.

Packaged in a 308-lead BGA, the AD8117/AD8118 junction-to-ambient thermal impedance (θ_{JA}) is 15°C/W. For long-term reliability, the maximum allowed junction temperature of the die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. The following curve shows the range of allowed internal die power dissipations that meet these conditions over the −40°C to +85°C ambient temperature range. When using the table, do not include external load power in the Maximum Power calculation, but do include load current dropped on the die output transistors.

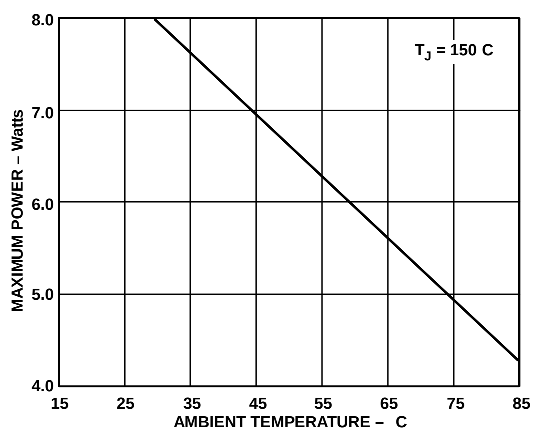


Figure 4. Maximum Die Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	vpos	vpos	vpos	vpos	op17	on17	op19	on19	op21	on21	op23	on23	op25	on25	op27	on27	op29	on29	op31	on31	vpos	vpos	vpos	A
B	vpos	vpos	vpos	op16	on16	op18	on18	op20	on20	op22	on22	op24	on24	op26	on26	op28	on28	op30	on30	vpos	vpos	vpos	vpos	B
C	vpos	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vpos	C
D	in16	vpos	vpos	vneg	vocm	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vocm	vneg	vpos	ip0	vpos	D
E	ip16	in17	vneg	vocm																vocm	vneg	in0	ip1	E
F	in18	ip17	vneg	vdd																vdd	vneg	ip2	in1	F
G	ip18	in19	vneg	dgnd																dgnd	vneg	in2	ip3	G
H	in20	ip19	vneg	resetb																data_out	vneg	ip4	in3	H
J	ip20	in21	vneg	updateb																clk	vneg	in4	ip5	J
K	in22	ip21	vneg	web																data_in	vneg	ip6	in5	K
L	ip22	in23	vpos	d5																serbpar	vpos	in6	ip7	L
M	in24	ip23	vpos	d4																a4	vpos	ip8	in7	M
N	ip24	in25	vpos	d3																a3	vpos	in8	ip9	N
P	in26	ip25	vneg	d2																a2	vneg	ip10	in9	P
R	ip26	in27	vneg	d1																a1	vneg	in10	ip11	R
T	in28	ip27	vneg	d0																a0	vneg	ip12	in11	T
U	ip28	in29	vneg	vdd																vdd	vneg	in12	ip13	U
V	in30	ip29	vneg	dgnd																dgnd	vneg	ip14	in13	V
W	ip30	in31	vneg	vocm																vocm	vneg	in14	ip15	W
Y	vpos	ip31	vpos	vneg	vocm	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vocm	vneg	vpos	vpos	in15	Y
AA	vpos	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vpos	AA
AB	vpos	vpos	vpos	vpos	on14	op14	on12	op12	on10	op10	on8	op8	on6	op6	on4	op4	on2	op2	on0	op0	vpos	vpos	vpos	AB
AC	vpos	vpos	vpos	on15	op15	on13	op13	on11	op11	on9	op9	on7	op7	on5	op5	on3	op3	on1	op1	vpos	vpos	vpos	vpos	AC
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PRELIMINARY

Bottom View

PRELIMINARY

Figure 5. BGA Bottom View Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	vpos	vpos	vpos	on31	op31	on29	op29	on27	op27	on25	op25	on23	op23	on21	op21	on19	op19	on17	op17	vpos	vpos	vpos	vpos
B	vpos	vpos	vpos	vpos	on30	op30	on28	op28	on26	op26	on24	op24	on22	op22	on20	op20	on18	op18	on16	op16	vpos	vpos	vpos
C	vpos	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vpos
D	vpos	ip0	vpos	vneg	vocm	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vocm	vneg	vpos	vpos	in16
E	ip1	in0	vneg	vocm																vocm	vneg	in17	ip16
F	in1	ip2	vneg	vdd																vdd	vneg	ip17	in18
G	ip3	in2	vneg	dgnd																dgnd	vneg	in19	ip18
H	in3	ip4	vneg	data_out																resetb	vneg	ip19	in20
J	ip5	in4	vneg	clk																updateb	vneg	in21	ip20
K	in5	ip6	vneg	data_in																web	vneg	ip21	in22
L	ip7	in6	vpos	serbpar								PRELIMINARY								d5	vpos	in23	ip22
M	in7	ip8	vpos	a4								Top View								d4	vpos	ip23	in24
N	ip9	in8	vpos	a3								PRELIMINARY								d3	vpos	in25	ip24
P	in9	ip10	vneg	a2																d2	vneg	ip25	in26
R	ip11	in10	vneg	a1																d1	vneg	in27	ip26
T	in11	ip12	vneg	a0																d0	vneg	ip27	in28
U	ip13	in12	vneg	vdd																vdd	vneg	in29	ip28
V	in13	ip14	vneg	dgnd																dgnd	vneg	ip29	in30
W	ip15	in14	vneg	vocm																vocm	vneg	in31	ip30
Y	in15	vpos	vpos	vneg	vocm	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vocm	vneg	vpos	ip31	vpos
AA	vpos	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vneg	vneg	vneg	vneg	vneg	vneg	vpos	vpos	vpos	vpos
AB	vpos	vpos	vpos	op0	on0	op2	on2	op4	on4	op6	on6	op8	on8	op10	on10	op12	on12	op14	on14	vpos	vpos	vpos	vpos
AC	vpos	vpos	vpos	vpos	op1	on1	op3	on3	op5	on5	op7	on7	op9	on9	op11	on11	op13	on13	op15	on15	vpos	vpos	vpos

Figure 6. BGA Top View Pinout

Table 6. Ball Grid Description

Ball	Mnemonic	Description
A1	VPOS	Analog positive power supply.
A2	VPOS	Analog positive power supply.
A3	VPOS	Analog positive power supply.
A4	ON31	Output number 31, negative phase.
A5	OP31	Output number 31, positive phase.
A6	ON29	Output number 29, negative phase.
A7	OP29	Output number 29, positive phase.
A8	ON27	Output number 27, negative phase.
A9	OP27	Output number 27, positive phase.
A10	ON25	Output number 25, negative phase.
A11	OP25	Output number 25, positive phase.
A12	ON23	Output number 23, negative phase.
A13	OP23	Output number 23, positive phase.
A14	ON21	Output number 21, negative phase.
A15	OP21	Output number 21, positive phase.
A16	ON19	Output number 19, negative phase.
A17	OP19	Output number 19, positive phase.
A18	ON17	Output number 17, negative phase.
A19	OP17	Output number 17, positive phase.
A20	VPOS	Analog positive power supply.
A21	VPOS	Analog positive power supply.
A22	VPOS	Analog positive power supply.
A23	VPOS	Analog positive power supply.
B1	VPOS	Analog positive power supply.

Ball	Mnemonic	Description
B2	VPOS	Analog positive power supply.
B3	VPOS	Analog positive power supply.
B4	VPOS	Analog positive power supply.
B5	ON30	Output number 30, negative phase.
B6	OP30	Output number 30, positive phase.
B7	ON28	Output number 28, negative phase.
B8	OP28	Output number 28, positive phase.
B9	ON26	Output number 26, negative phase.
B10	OP26	Output number 26, positive phase.
B11	ON24	Output number 24, negative phase.
B12	OP24	Output number 24, positive phase.
B13	ON22	Output number 22, negative phase.
B14	OP22	Output number 22, positive phase.
B15	ON20	Output number 20, negative phase.
B16	OP20	Output number 20, positive phase.
B17	ON18	Output number 18, negative phase.
B18	OP18	Output number 18, positive phase.
B19	ON16	Output number 16, negative phase.
B20	OP16	Output number 16, positive phase.
B21	VPOS	Analog positive power supply.
B22	VPOS	Analog positive power supply.
B23	VPOS	Analog positive power supply.
C1	VPOS	Analog positive power supply.
C2	VPOS	Analog positive power supply.
C3	VPOS	Analog positive power supply.
C4	VPOS	Analog positive power supply.
C5	VNEG	Analog negative power supply.
C6	VNEG	Analog negative power supply.
C7	VNEG	Analog negative power supply.
C8	VNEG	Analog negative power supply.
C9	VNEG	Analog negative power supply.
C10	VNEG	Analog negative power supply.
C11	VPOS	Analog positive power supply.
C12	VPOS	Analog positive power supply.
C13	VPOS	Analog positive power supply.
C14	VNEG	Analog negative power supply.
C15	VNEG	Analog negative power supply.
C16	VNEG	Analog negative power supply.
C17	VNEG	Analog negative power supply.
C18	VNEG	Analog negative power supply.
C19	VNEG	Analog negative power supply.
C20	VPOS	Analog positive power supply.
C21	VPOS	Analog positive power supply.
C22	VPOS	Analog positive power supply.
C23	VPOS	Analog positive power supply.
D1	VPOS	Analog positive power supply.
D2	IP0	Input number 0, positive phase.
D3	VPOS	Analog positive power supply.
D4	VNEG	Analog negative power supply.
D5	VOCM	Output common-mode reference supply.
D6	VNEG	Analog negative power supply.
D7	VNEG	Analog negative power supply.
D8	VNEG	Analog negative power supply.
D9	VNEG	Analog negative power supply.
D10	VNEG	Analog negative power supply.
D11	VPOS	Analog positive power supply.
D12	VPOS	Analog positive power supply.
D13	VPOS	Analog positive power supply.
D14	VNEG	Analog negative power supply.
D15	VNEG	Analog negative power supply.
D16	VNEG	Analog negative power supply.
D17	VNEG	Analog negative power supply.
D18	VNEG	Analog negative power supply.
D19	VOCM	Output common-mode reference supply.
D20	VNEG	Analog negative power supply.
D21	VPOS	Analog positive power supply.
D22	VPOS	Analog positive power supply.
D23	IN16	Input number 16, negative phase.
E1	IP1	Input number 1, positive phase.
E2	IN0	Input number 0, negative phase.
E3	VNEG	Analog negative power supply.
E4	VOCM	Output common-mode reference supply.
E20	VOCM	Output common-mode reference supply.
E21	VNEG	Analog negative power supply.
E22	IN17	Input number 17, negative phase.
E23	IP16	Input number 16, positive phase.
F1	IN1	Input number 1, negative phase.
F2	IP2	Input number 2, positive phase.
F3	VNEG	Analog negative power supply.
F4	VDD	Logic positive power supply.
F20	VDD	Logic positive power supply.
F21	VNEG	Analog negative power supply.
F22	IP17	Input number 17, positive phase.
F23	IN18	Input number 18, negative phase.
G1	IP3	Input number 3, positive phase.
G2	IN2	Input number 2, negative phase.
G3	VNEG	Analog negative power supply.
G4	DGND	Logic negative power supply.
G20	DGND	Logic negative power supply.
G21	VNEG	Analog negative power supply.
G22	IN19	Input number 19, negative phase.
G23	IP18	Input number 18, positive phase.
H1	IN3	Input number 3, negative phase.
H2	IP4	Input number 4, positive phase.
H3	VNEG	Analog negative power supply.
H4	DATA_OUT	Control pin: serial data out.
H20	RESETB	Control pin: second rank data reset.
H21	VNEG	Analog negative power supply.
H22	IP19	Input number 19, positive phase.
H23	IN20	Input number 20, negative phase.

Ball	Mnemonic	Description
J1	IP5	Input number 5, positive phase.
J2	IN4	Input number 4, negative phase.
J3	VNEG	Analog negative power supply.
J4	CLK	Control pin: serial data clock.
J20	UPDATEB	Control pin: second rank write strobe.
J21	VNEG	Analog negative power supply.
J22	IN21	Input number 21, negative phase.
J23	IP20	Input number 20, positive phase.
K1	IN5	Input number 5, negative phase.
K2	IP6	Input number 6, positive phase.
K3	VNEG	Analog negative power supply.
K4	DATA_IN	Control pin: serial data in.
K20	WEB	Control pin: first rank write strobe.
K21	VNEG	Analog negative power supply.
K22	IP21	Input number 21, positive phase.
K23	IN22	Input number 22, negative phase.
L1	IP7	Input number 7, positive phase.
L2	IN6	Input number 6, negative phase.
L3	VPOS	Analog positive power supply.
L4	SERBPAR	Control pin: serial/parallel mode select.
L20	D5	Control pin: input address bit 5.
L21	VPOS	Analog positive power supply.
L22	IN23	Input number 23, negative phase.
L23	IP22	Input number 22, positive phase.
M1	IN7	Input number 7, negative phase.
M2	IP8	Input number 8, positive phase.
M3	VPOS	Analog positive power supply.
M4	A4	Control pin: output address bit 4.
M20	D4	Control pin: input address bit 4.
M21	VPOS	Analog positive power supply.
M22	IP23	Input number 23, positive phase.
M23	IN24	Input number 24, negative phase.
N1	IP9	Input number 9, positive phase.
N2	IN8	Input number 8, negative phase.
N3	VPOS	Analog positive power supply.
N4	A3	Control pin: output address bit 3.
N20	D3	Control pin: input address bit 3.
N21	VPOS	Analog positive power supply.
N22	IN25	Input number 25, negative phase.
N23	IP24	Input number 24, positive phase.
P1	IN9	Input number 9, negative phase.
P2	IP10	Input number 10, positive phase.
P3	VNEG	Analog negative power supply.
P4	A2	Control pin: output address bit 2.
P20	D2	Control pin: input address bit 2.
P21	VNEG	Analog negative power supply.
P22	IP25	Input number 25, positive phase.
P23	IN26	Input number 26, negative phase.
R1	IP11	Input number 11, positive phase.
R2	IN10	Input number 10, negative phase.
R3	VNEG	Analog negative power supply.
R4	A1	Control pin: output address bit 1.
R20	D1	Control pin: input address bit 1.
R21	VNEG	Analog negative power supply.
R22	IN27	Input number 27, negative phase.
R23	IP26	Input number 26, positive phase.
T1	IN11	Input number 11, negative phase.
T2	IP12	Input number 12, positive phase.
T3	VNEG	Analog negative power supply.
T4	A0	Control pin: output address bit 0.
T20	D0	Control pin: input address bit 0.
T21	VNEG	Analog negative power supply.
T22	IP27	Input number 27, positive phase.
T23	IN28	Input number 28, negative phase.
U1	IP13	Input number 13, positive phase.
U2	IN12	Input number 12, negative phase.
U3	VNEG	Analog negative power supply.
U4	VDD	Logic positive power supply.
U20	VDD	Logic positive power supply.
U21	VNEG	Analog negative power supply.
U22	IN29	Input number 29, negative phase.
U23	IP28	Input number 28, positive phase.
V1	IN13	Input number 13, negative phase.
V2	IP14	Input number 14, positive phase.
V3	VNEG	Analog negative power supply.
V4	DGND	Logic negative power supply.
V20	DGND	Logic negative power supply.
V21	VNEG	Analog negative power supply.
V22	IP29	Input number 29, positive phase.
V23	IN30	Input number 30, negative phase.
W1	IP15	Input number 15, positive phase.
W2	IN14	Input number 14, negative phase.
W3	VNEG	Analog negative power supply.
W4	VOCM	Output common-mode reference supply.
W20	VOCM	Output common-mode reference supply.
W21	VNEG	Analog negative power supply.
W22	IN31	Input number 31, negative phase.
W23	IP30	Input number 30, positive phase.
Y1	IN15	Input number 15, negative phase.
Y2	VPOS	Analog positive power supply.
Y3	VPOS	Analog positive power supply.
Y4	VNEG	Analog negative power supply.
Y5	VOCM	Output common-mode reference supply.
Y6	VNEG	Analog negative power supply.
Y7	VNEG	Analog negative power supply.
Y8	VNEG	Analog negative power supply.
Y9	VNEG	Analog negative power supply.
Y10	VNEG	Analog negative power supply.
Y11	VPOS	Analog positive power supply.
Y12	VPOS	Analog positive power supply.

Ball	Mnemonic	Description
Y13	VPOS	Analog positive power supply.
Y14	VNEG	Analog negative power supply.
Y15	VNEG	Analog negative power supply.
Y16	VNEG	Analog negative power supply.
Y17	VNEG	Analog negative power supply.
Y18	VNEG	Analog negative power supply.
Y19	VOCM	Output common-mode reference supply.
Y20	VNEG	Analog negative power supply.
Y21	VPOS	Analog positive power supply.
Y22	IP31	Input number 31, positive phase.
Y23	VPOS	Analog positive power supply.
AA1	VPOS	Analog positive power supply.
AA2	VPOS	Analog positive power supply.
AA3	VPOS	Analog positive power supply.
AA4	VPOS	Analog positive power supply.
AA5	VNEG	Analog negative power supply.
AA6	VNEG	Analog negative power supply.
AA7	VNEG	Analog negative power supply.
AA8	VNEG	Analog negative power supply.
AA9	VNEG	Analog negative power supply.
AA10	VNEG	Analog negative power supply.
AA11	VPOS	Analog positive power supply.
AA12	VPOS	Analog positive power supply.
AA13	VPOS	Analog positive power supply.
AA14	VNEG	Analog negative power supply.
AA15	VNEG	Analog negative power supply.
AA16	VNEG	Analog negative power supply.
AA17	VNEG	Analog negative power supply.
AA18	VNEG	Analog negative power supply.
AA19	VNEG	Analog negative power supply.
AA20	VPOS	Analog positive power supply.
AA21	VPOS	Analog positive power supply.
AA22	VPOS	Analog positive power supply.
AA23	VPOS	Analog positive power supply.
AB1	VPOS	Analog positive power supply.
AB2	VPOS	Analog positive power supply.
AB3	VPOS	Analog positive power supply.
AB4	OP0	Output number 0, positive phase.
AB5	ON0	Output number 0, negative phase.
AB6	OP2	Output number 2, positive phase.
AB7	ON2	Output number 2, negative phase.
AB8	OP4	Output number 4, positive phase.
AB9	ON4	Output number 4, negative phase.
AB10	OP6	Output number 6, positive phase.
AB11	ON6	Output number 6, negative phase.
AB12	OP8	Output number 8, positive phase.
AB13	ON8	Output number 8, negative phase.
AB14	OP10	Output number 10, positive phase.
AB15	ON10	Output number 10, negative phase.
AB16	OP12	Output number 12, positive phase.
AB17	ON12	Output number 12, negative phase.
AB18	OP14	Output number 14, positive phase.
AB19	ON14	Output number 14, negative phase.
AB20	VPOS	Analog positive power supply.
AB21	VPOS	Analog positive power supply.
AB22	VPOS	Analog positive power supply.
AB23	VPOS	Analog positive power supply.
AC1	VPOS	Analog positive power supply.
AC2	VPOS	Analog positive power supply.
AC3	VPOS	Analog positive power supply.
AC4	VPOS	Analog positive power supply.
AC5	OP1	Output number 1, positive phase.
AC6	ON1	Output number 1, negative phase.
AC7	OP3	Output number 3, positive phase.
AC8	ON3	Output number 3, negative phase.
AC9	OP5	Output number 5, positive phase.
AC10	ON5	Output number 5, negative phase.
AC11	OP7	Output number 7, positive phase.
AC12	ON7	Output number 7, negative phase.
AC13	OP9	Output number 9, positive phase.
AC14	ON9	Output number 9, negative phase.
AC15	OP11	Output number 11, positive phase.
AC16	ON11	Output number 11, negative phase.
AC17	OP13	Output number 13, positive phase.
AC18	ON13	Output number 13, negative phase.
AC19	OP15	Output number 15, positive phase.
AC20	ON15	Output number 15, negative phase.
AC21	VPOS	Analog positive power supply.
AC22	VPOS	Analog positive power supply.
AC23	VPOS	Analog positive power supply.

Table 7. Operation Truth Table

UPDATE	CLK	DATA IN	DATA OUT	WE	RESET	SER/PAR	Operation/Comment
X	X	X	X	X	0	X	Asynchronous reset. All outputs are disabled.
X	X	X	X	X	1	X	tbd
X	X	X	X	X	1	X	tbd
X	X	X	X	X	1	X	tbd
X	X	X	X	X	1	X	tbd
X	X	X	X	X	1	X	tbd

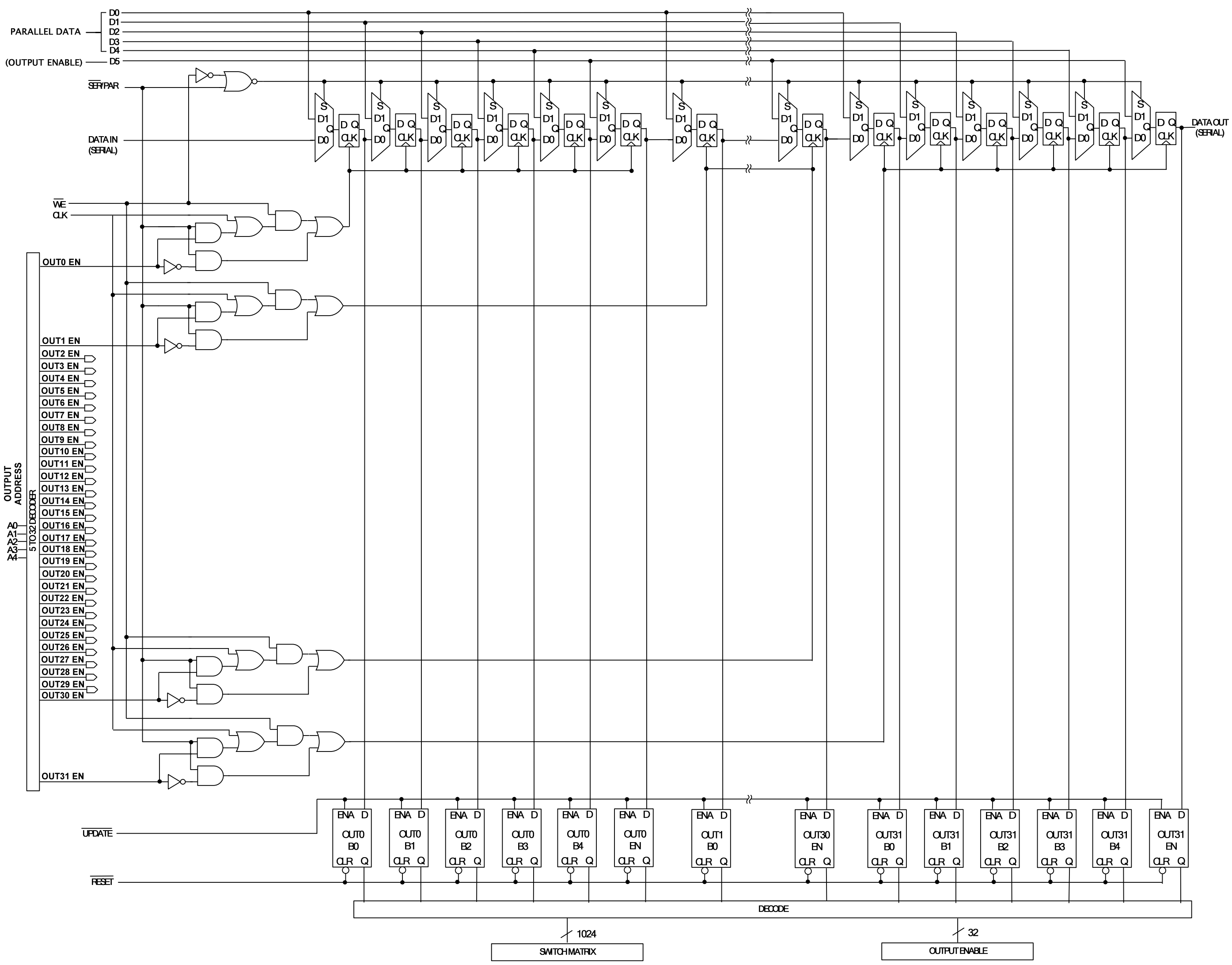
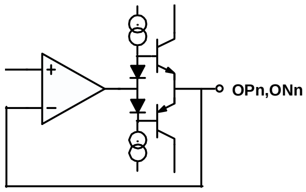
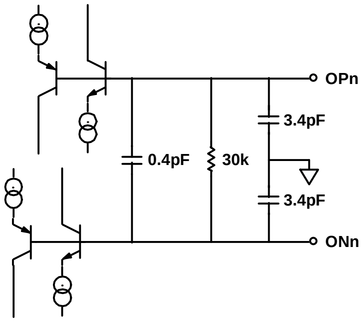


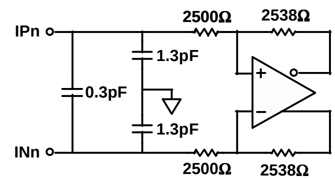
Figure 7. Logic Diagram



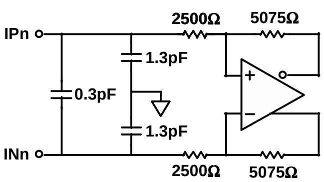
a. AD8117/AD8118 Enabled Output (see also ESD Protection Map)



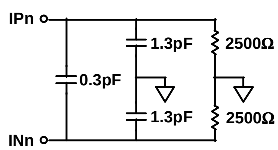
b. AD8117/AD8118 Disabled Output (see also ESD Protection Map)



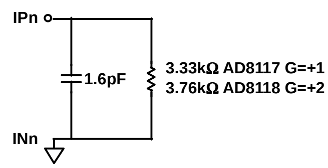
c. AD8117 Receiver (see also ESD Protection Map)



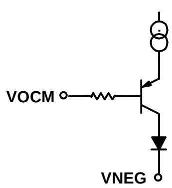
d. AD8118 Receiver (see also ESD Protection Map)



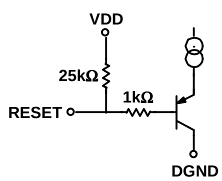
e. AD8117/AD8118 Receiver Simplified Equivalent Circuit When Driving Differentially



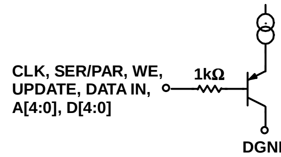
f. AD8117/AD8118 Receiver Simplified Equivalent Circuit When Driving Single-Ended



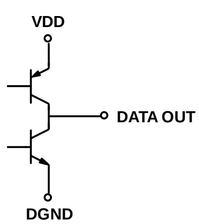
g. VOCM input (see also ESD Protection Map)



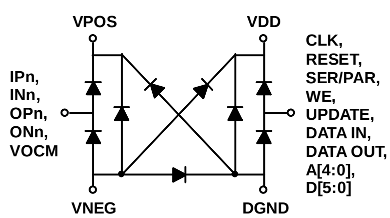
h. Reset Input (see also ESD Protection Map)



i. Logic Input (see also ESD Protection Map)



j. Logic Output (see also ESD Protection Map)



k. ESD Protection Map

Figure 8. I/O Schematics

TYPICAL PERFORMANCE CHARACTERISTICS

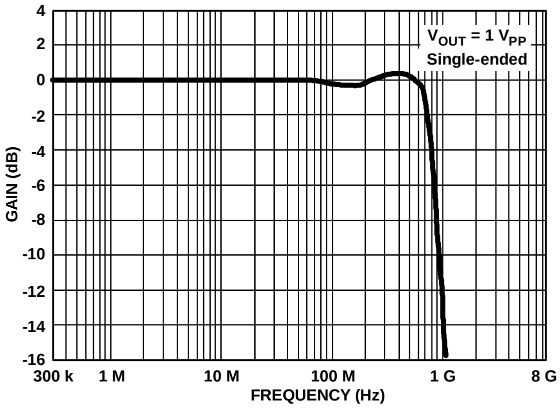


Figure 9. AD8117 Large Signal Frequency Response

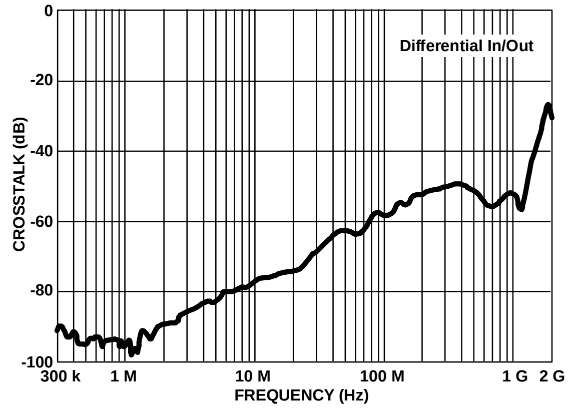


Figure 12. AD8117 Crosstalk, One Adjacent Channel, Differential Mode

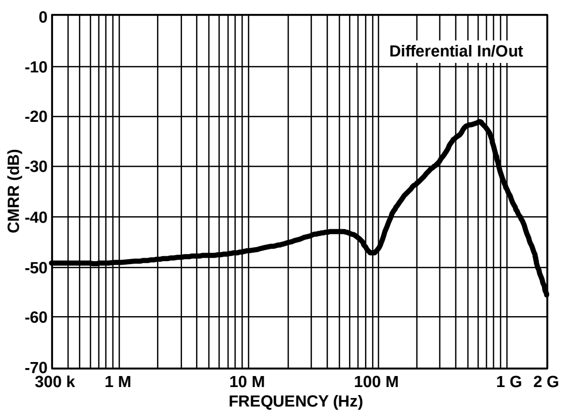


Figure 10. AD8117 Common-Mode Rejection

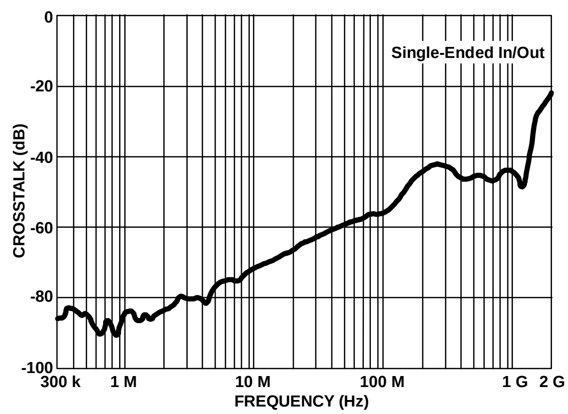


Figure 13. AD8117 Crosstalk, One Adjacent Channel, Single-Ended Mode

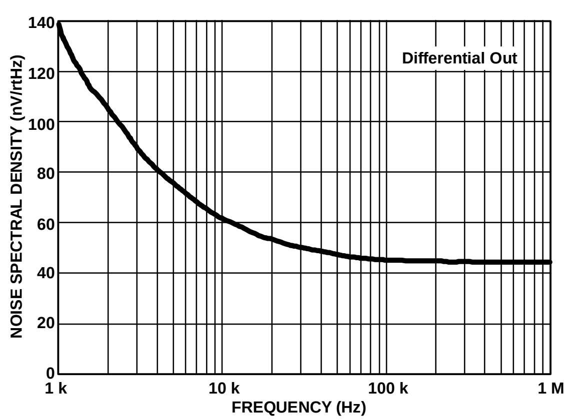


Figure 11. AD8117 Noise Spectral Density, Differential Mode

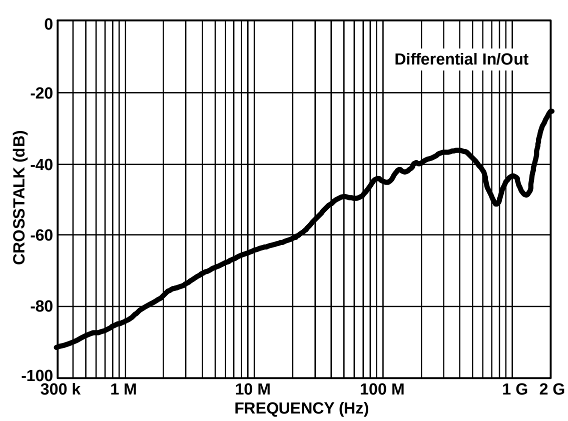


Figure 14. AD8117 Crosstalk, All-Hostile, Differential Mode

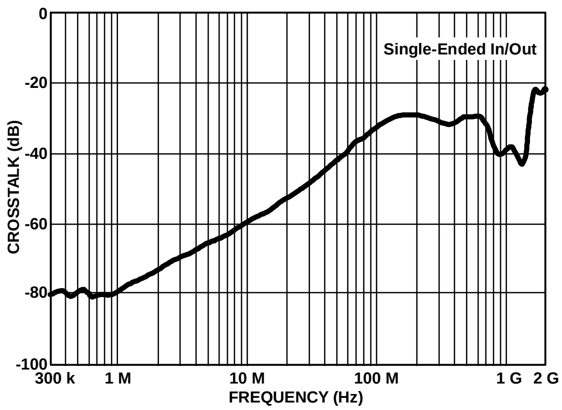


Figure 15. AD8117 Crosstalk, All-Hostile, Single-Ended Mode

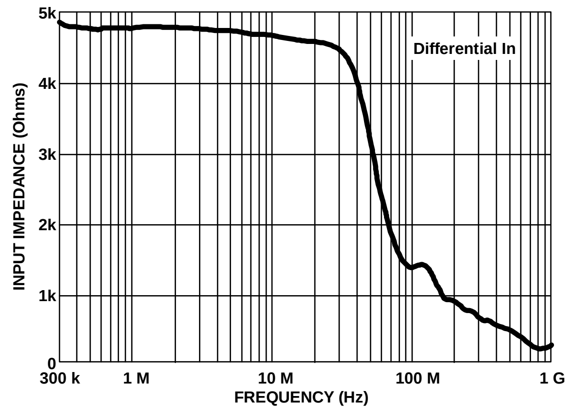


Figure 18. AD8117 Input Impedance, Differential Mode

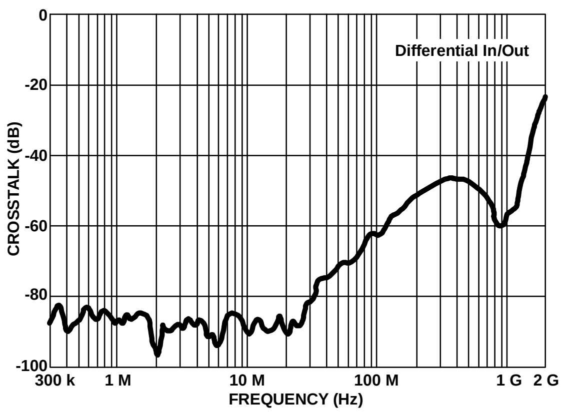


Figure 16. AD8117 Crosstalk, Off-Isolation, Differential Mode

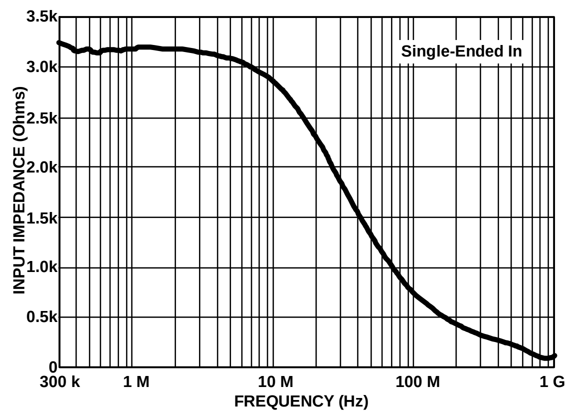


Figure 19. AD8117 Input Impedance, Single-Ended Mode

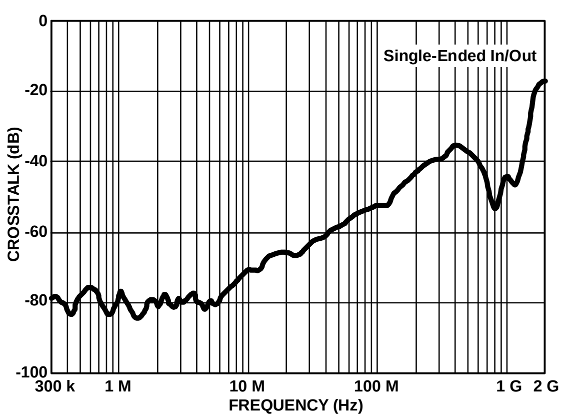


Figure 17. AD8117 Crosstalk, Off-Isolation, Single-Ended Mode

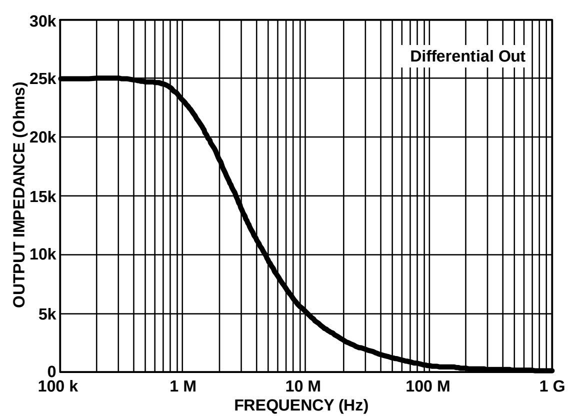


Figure 20. AD8117 Output Impedance, Disabled, Differential Mode

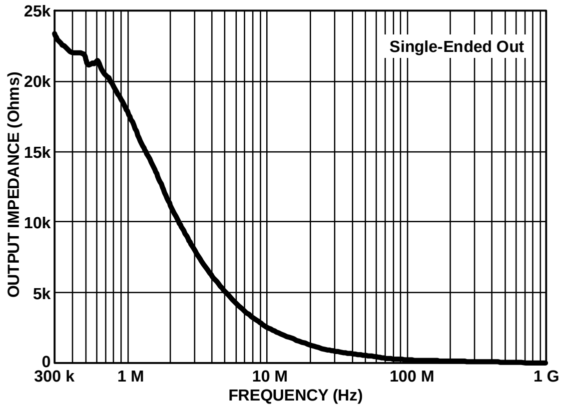


Figure 21. AD8117 Output Impedance, Disabled, Single-Ended Mode

THEORY OF OPERATION

The AD8117 is a fully-differential crosspoint array with 32 outputs, each of which can be connected to any one of 32 inputs. Organized by output row, 32 switchable input transconductance stages are connected to each output buffer to form 32-to-1 multiplexers. There are 32 of these multiplexers, each with its inputs wired in parallel, for a total array of 1,024 transconductance stages forming a multicast-capable crosspoint switch.

Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The enabled transconductance stage drives the output stage, and feedback forms a closed-loop amplifier with a differential gain of one (the difference between the output voltages is equal to the difference between the input voltages). A second feedback loop controls the common-mode output level, forcing the average of the differential output voltages to match the voltage on the VOCM reference pin. Although each output has an independent common-mode control loop, the VOCM reference is common for the entire chip, and as such needs to be driven with a low impedance to avoid crosstalk.

Each differential input to the AD8117 is buffered by a receiver. The purpose of this receiver is to provide an extended input common-mode range, and to remove this common-mode from the signal chain. Like the output multiplexers, the input receiver has both a differential loop and a common-mode control loop. A mask-programmable feedback network sets the closed-loop differential gain. For the AD8117, this differential gain is one, and for the AD8118, this is a differential gain of two. The receiver has an input stage that does not respond to the common-mode of the signal. This architecture, along with the attenuating feedback network, allows the user to apply input voltages that extend from rail-to-rail. Excess differential loop gain-bandwidth product reduces the effect of the closed-loop gain on the bandwidth of the device.

The output stage of the AD8117 is designed for low differential gain and phase error when driving composite video signals. It also provides slew current for fast pulse response when driving component video signals. Unlike many multiplexer designs, these requirements are balanced such that large signal bandwidth is very similar to small signal bandwidth. The design load is 150 Ω, but provisions are made to drive loads as low as 75 Ω so long as on-chip power dissipation limits are not exceeded.

The outputs of the AD8117 can be disabled to minimize on-chip power dissipation. When disabled, there is only a common-mode feedback network of 30kΩ between the differential outputs. This high impedance allows multiple ICs to be bussed together without additional buffering. Care must be taken to reduce output capacitance, which will result in more overshoot and frequency-domain peaking. A series of internal amplifiers drive internal nodes such that a wide-band high-impedance is presented at the disabled output, even while the output bus is under large signal swings. When the outputs are disabled and driven externally, the voltage applied to them should not exceed the valid output swing range for the AD8117 in order to keep these internal amplifiers in their linear range of operation. Applying excess differential voltages to the disabled outputs can cause damage to the AD8117 and should be avoided (see the Absolute Maximum Ratings section of this datasheet for guidelines).

The connection of the AD8117 is controlled by a flexible TTL compatible logic interface. Either parallel or serial loading into a first rank of latches preprograms each output. A global update signal moves the programming data into the second rank of latches, simultaneously updating all outputs. In serial mode, a serial-out pin allows devices to be daisy chained together for single-pin programming of multiple ICs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs. This power-on reset clears the second rank of latches, but does not clear the first rank of latches. In parallel mode, to quickly clear the first rank, a broadcast parallel programming feature is available. In serial-mode, pre-programming individual inputs is not possible and the entire shift register needs to be flushed.

The AD8117 can operate on a single +5 V supply, powering both the signal path (with the VPOS/VNEG supply pins), and the control logic interface (with the VDD/DGND supply pins). But in order to easily interface to ground-referenced video signals, split supply operation is possible with ± 2.5 V supplies. In this case, a flexible logic interface allows the control logic supplies (VDD/DGND) to be run off +2 V/0 V to +3.3 V/0 V while the core remains on split supplies. Additional flexibility in the analog output common-mode level facilitates unequal split supplies. If +3 V/−2 V supplies to +2 V/−3 V supplies are desired, the VOCM pin can still be set to 0 V for ground-referenced video signals.

APPLICATIONS

PROGRAMMING

The AD8117/AD8118 have two options for changing the programming of the crosspoint matrix. In the first option a serial word of 192 bits can be provided that will update the entire matrix each time. The second option allows for changing a single output's programming via a parallel interface. The serial option requires fewer signals, but more time (clock cycles) for changing the programming, while the parallel programming technique requires more signals, but can change a single output at a time and requires fewer clock cycles to complete programming.

Serial Programming Description

The serial programming mode uses the device pins CLK, DATA IN, UPDATE and SER/PAR. The first step is to assert a LOW on SER/PAR in order to enable the serial programming mode. The parallel clock, WE should be held HIGH during the entire serial programming operation.

The UPDATE signal should be high during the time that data is shifted into the device's serial port. Although the data will still shift in when UPDATE is LOW, the transparent, asynchronous latches will allow the shifting data to reach the matrix. This will cause the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATA IN is clocked in at every falling edge of CLK. A total of 192 bits must be shifted in to complete the programming. For each of the 32 outputs, there are five bits (D0–D4) that determine the source of its input followed by one bit (D5) that determines the enabled state of the output. If D5 is LOW (output disabled), the four associated bits (D0–D4) do not matter, because no input will be switched to that output.

The most-significant-output-address data is shifted in first, then following in sequence until the least-significant-output-address data is shifted in. At this point UPDATE can be taken low, which will cause the programming of the device according to the data that was just shifted in. The UPDATE latches are asynchronous and when UPDATE is low they are transparent.

If more than one AD8117 device is to be serially programmed in a system, the DATA OUT signal from one device can be connected to the DATA IN of the next device to form a serial chain. All of the CLK, UPDATE, and SER/PAR pins should be connected in parallel and operated as described above. The serial data is input to the DATA IN pin of the first device of the chain, and it will ripple through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence will be 192 bits times the number of devices in the chain.

Parallel Programming Description

When using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. In fact, parallel programming allows the modification of a single output at a time. Since this takes only one WE/UPDATE cycle, significant time savings can be realized by using parallel programming.

One important consideration in using parallel programming is that the RESET signal does not reset all registers in the AD8117. When taken LOW, the RESET signal will only set each output to the disabled state. This is helpful during power-up to ensure that two parallel outputs will not be active at the same time.

After initial power-up, the internal registers in the device will generally have random data, even though the RESET signal has been asserted. If parallel programming is used to program one output, then that output will be properly programmed, but the rest of the device will have a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that all outputs be programmed to a desired state after power-up. This will ensure that the programming matrix is always in a known state. From then on, parallel programming can be used to modify a single output or more at a time.

In similar fashion, if UPDATE is taken LOW after initial power-up, the random power-up data in the shift register will be programmed into the matrix. Therefore, in order to prevent the crosspoint from being programmed into an unknown state, do not apply a low logic level to UPDATE after power is initially applied. Programming the full shift register one time to a desired state, by either serial or parallel programming after initial power-up, will eliminate the possibility of programming the matrix to an unknown state.

To change an output's programming via parallel programming, SER/PAR and UPDATE should be taken HIGH. The serial programming clock, CLK, should be left HIGH during parallel programming. The parallel clock, WE, should start in the HIGH state. The 5-bit address of the output to be programmed should be put on A0–A4. The first five data bits (D0–D4) should contain the information that identifies the input that gets programmed to the output that is addressed. The sixth data bit (D5) will determine the enabled state of the output. If D5 is LOW (output disabled), then the data on D0–D4 does not matter.

After the desired address and data signals have been established, they can be latched into the shift register by a high to low transition of the WE signal. The matrix will not be programmed, however, until the UPDATE signal is taken low. It is thus possible to latch in new data for several or all of the outputs first via successive negative transitions of WE while UPDATE is held HIGH, and then have all the new data take effect when UPDATE goes LOW. This is the technique that should be used when programming the device for the first time after power-up when using parallel programming.

Reset

When powering up the AD8117, it is usually desirable to have the outputs come up in the disabled state. The RESET pin, when taken LOW, will cause all outputs to be in the disabled state. However, the RESET signal does not reset all registers in the AD8117. This is important when operating in the parallel programming mode. Please refer to that section for information about programming internal registers after power-up. Serial programming will program the entire matrix each time, so no special considerations apply.

Since the data in the shift register is random after power-up, it should not be used to program the matrix, or the matrix can enter unknown states. To prevent this, do not apply a logic low signal to UPDATE initially after power-up. The shift register should first be loaded with the desired data, and then UPDATE can be taken LOW to program the device.

The RESET pin has a 20 kΩ pull-up resistor to VDD that can be used to create a simple power-up reset circuit. A capacitor from RESET to ground will hold RESET low for some time while the rest of the device stabilizes. The low condition will cause all the outputs to be disabled. The capacitor will then charge through the pull-up resistor to the high state, thus allowing full programming capability of the device.

Broadcast

The AD8117 logic interface has a broadcast mode, in which all first rank latches can be simultaneously parallel-programmed to the same data in one write-cycle. This is especially useful in clearing random first rank data after power-up. To access the broadcast mode, the part is parallel-programmed using the device pins WE, A0–A4, D0–A5 and UPDATE. The only difference is that the SER/PAR pin is held LOW, as if serial programming. By holding CLK high, no serial clocking will occur, and instead the WE can be used to clock all first rank latches in the chip at once.

OPERATING MODES

The AD8117/AD8118 has fully-differential inputs and outputs. The inputs and outputs can also be operated in a single-ended fashion. This presents several options for circuit configurations that will require different gains and treatment of terminations, if they are used.

Differential Input

The AD8117/AD8118 has differential input receivers. These receivers allow the user to drive the inputs with a differential signal with an uncertain common-mode voltage, such as from a remote source over twisted pair. The receivers will respond only to the difference in input voltages, and will restore a common-mode voltage suitable for the internal signal path. Noise or crosstalk that is present in both inputs will be rejected by the input stage, as specified by its common-mode rejection ratio (CMRR). Differential operation offers a great noise benefit for signals that are propagated over distance in a noisy environment.

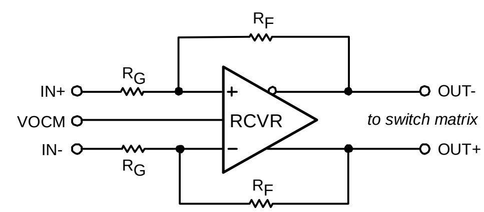


Figure 22. Input Receiver Equivalent Circuit

The circuit configuration used by the differential input receivers is similar to that of several Analog Devices general-purpose differential amplifiers, such as the AD8131. It is a voltage-feedback amplifier with internal gain setting resistors. The arrangement of feedback makes the differential input impedance appear to be 5 kΩ across the inputs.

$$R_{IN,\,dm} = 2 \times R_G = 5\ \text{k}\Omega$$

This impedance will create a small differential termination error if the user does not account for the 5 kΩ parallel element, although this error will be less than 1% in most cases. Additionally, the source impedance driving the AD8117 appears in parallel with the internal gain-setting resistors, such that there may be a gain error for some values of source resistance. The AD8117/AD8118 are adjusted such that their gains will be correct when driven by a back-terminated 75 Ω source impedance at each input phase (37.5 Ω effective impedance to ground at each input pin, or 75 Ω differential source impedance across pairs of input pins). If a different source impedance is presented, the differential gain of the AD8117/AD8118 can be calculated by

$$G_{dm} = \frac{V_{OUT,\,dm}}{V_{IN,\,dm}} = \frac{R_F}{R_G + R_S}$$

where R_G is 2.5 kΩ, R_S is the user single-ended source resistance (such as 37.5 Ω for a back-terminated 75 Ω source), and R_F is 2.538 kΩ for the AD8117 and 5.075 kΩ for the AD8118.

In the case of the AD8117, this is

$$G_{dm} = \frac{2.538\ \text{k}\Omega}{2.5\ \text{k}\Omega + R_S}$$

In the case of the AD8118, this is

$$G_{dm} = \frac{5.075\ \text{k}\Omega}{2.5\ \text{k}\Omega + R_S}$$

When operating with a differential input, care must be taken to keep the common-mode, or average, of the input voltages within the linear operating range of the AD8117/AD8118 receiver. This common-mode range can extend rail-to-rail, provided the differential signal swing is small enough to avoid forward biasing the ESD diodes (it is safest to keep the common-mode plus differential signal excursions within the supply voltages of the part).

The differential output of the AD8117/AD8118 receiver is linear for a peak of 1.4V of output voltage difference (1.4 V peak input difference for the AD8117, and 0.7 V peak input difference for the AD8118). Taking the output differentially, using the two output phases, this allows 2.8 V_{PP} of linear output signal swing. Beyond this level, the signal path will saturate and limit the signal swing. This is not a desired operation, as the supply current will increase and the signal path will be slow to recover from clipping. The absolute maximum allowed differential input signal is limited by long-term reliability of the input stage. The limits in the Absolute Maximum Ratings section of the datasheet should be observed in order to avoid degrading device performance permanently.

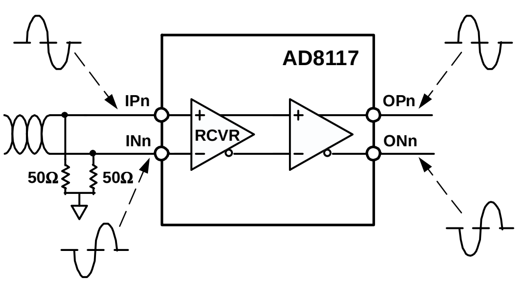


Figure 23. Example of Input Driven Differentially

AC-Coupling

It is possible to AC-couple the inputs of the AD8117/AD8118 receiver. This is simplified in that bias current does not need to be supplied externally. A capacitor in series with the inputs to the AD8117/AD8118 will create a high-pass filter with the input impedance of the device. This capacitor will need to be sized such that the corner frequency is low enough for frequencies of interest.

Single-ended Input

The AD8117/AD8118 input receiver can also be driven single-ended (unbalanced). From the standpoint of the receiver, there is very little difference between signals applied positive and negative in two phases to the input pair, versus a signal applied to one input only with the other input held at a constant potential. One small difference is that the common-mode between the input pins will be changing if only one input is moving, and there is a very small common-mode to differential conversion gain in the receiver that will add an additional gain error to the output (see the common-mode rejection ratio specifications for the input stage). For low frequencies, this gain error is negligible. The common-mode rejection ratio degrades with increasing frequency.

When operating the AD8117/AD8118 receiver single-endedly, the observed input resistance at each input pin is higher than in the differential input case, due to a fraction of the receiver internal output voltage appearing as a common-mode signal on its input terminals, bootstrapping the voltage on the input resistance. This single-ended input resistance can be calculated by the formula

$$R_{IN} = \frac{R_G + R_S}{1 - \dfrac{R_F}{2 \times (R_G + R_S + R_F)}}$$

where R_G is 2.5 kΩ, R_S is the user single-ended source resistance (such as 37.5 Ω for a back-terminated 75 Ω source), and R_F is 2.538 kΩ for the AD8117 and 5.075 kΩ for the AD8118.

In most cases, a single-ended input signal will be referred to mid-supply, typically ground. In this case, the undriven differential input could be connected to ground. For best dynamic performance and lowest offset voltage, this unused input should be terminated with an impedance matching the driven input, instead of being directly shorted to ground. Due to the differential feedback of the receiver, there is high-frequency signal current in the undriven input and it should be treated as a signal line in the board design.

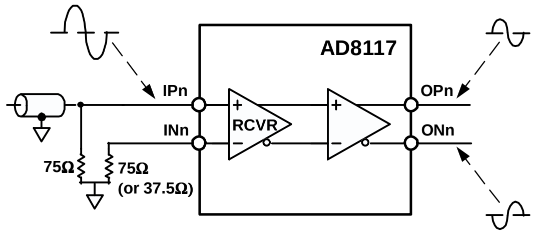


Figure 24. Example of Input Driven Single-Ended

Differential Output

Benefits of Differential Operation

The AD8117/AD8118 has a fully-differential switch core, with differential outputs. The two output voltages move in opposite directions, with a differential feedback loop maintaining a fixed output stage differential gain of +1 (the different overall signal path gains between the AD8117 and AD8118 are set in the input stage for best signal-to-noise ratio). This differential output stage provides a benefit of crosstalk-canceling due to parasitic coupling from one output to another being equal and out of phase. Additionally, if the output of the device is utilized in a differential design, noise, crosstalk and offset voltages generated on-chip that are coupled equally into both outputs will be cancelled by the common-mode rejection ratio of the next device in the signal chain. By utilizing the AD8117/AD8118 outputs in a differential application, the best possible noise and offset specifications can be realized.

Differential Gain

The specified signal path gain of the AD8117/AD8118 refers to its differential gain. For the AD8117, the gain of +1 means that the difference in voltage between the two output terminals is equal to the difference applied between the two input terminals. For the AD8118, the ratio of output difference voltage to applied input difference voltage is +2.

The common-mode, or average voltage of the pair of output signals is set by the voltage on the VOCM pin. This voltage is typically set to mid-supply (often ground), but may be moved approximately ± 0.5 V in order to accommodate cases where the desired output common-mode voltage may not be mid-supply (as in the case of unequal split supplies). Adjusting VOCM beyond ± 0.5 V can limit differential swing internally below the specifications on the datasheet.

Regardless of the differential gain of the device, the common-mode gain for the AD8117 and AD8118 is +1 to the output. This means that the common-mode of the output voltages will directly follow the reference voltage applied to the VOCM input.

The VOCM reference is a high-speed signal input, common to all output stages on the device. It requires only small amounts of bias current, but noise appearing on this pin will be buffered to the outputs of all the output stages. As such, the VOCM node should be connected to a low-noise, low-impedance voltage to avoid being a source of noise, offset and crosstalk in the signal path.

Termination

The AD8117/AD8118 is designed to drive 150 Ω on each output (or an effective 300 Ω differential) while meeting datasheet specifications, but the output stage is capable of supplying the current to drive 100 Ω loads (200 Ω differential) over the specified operating temperature range. If care is taken to observe the maximum power derating curves, the output stage can drive 75 Ω loads with slightly reduced slew rate and bandwidth (an effective 150 Ω differential load).

Termination at the load end is recommended for best signal integrity. This load termination is often a resistor to a ground reference on each individual output. By terminating to the same voltage level that drives the VOCM reference, the power dissipation due to DC termination current will be reduced. In differential signal paths, it is often desirable to terminate differentially, with a single resistor across the differential outputs at the load end. This is acceptable for the AD8117/AD8118, but when the device outputs are placed in a disabled state, a small amount of DC bias current is required if the output is to present as a high-impedance over an excursion of output bus voltages. If the AD8117/AD8118 disabled outputs are floated (or simply tied together by a resistor), internal nodes will saturate and an increase in disabled output current may be observed.

For best pulse response, it is often desirable to place a series resistor in each output to match the characteristic impedance and termination of the output trace or cable. This is known as back-termination, and helps shorten settling time by terminating reflected signals when driving a load that is not accurately terminated at the load end. A side-effect of back-termination is an attenuation of the output signal by a factor of two. In this case, a gain of two is usually necessary somewhere in the signal path to restore the signal.

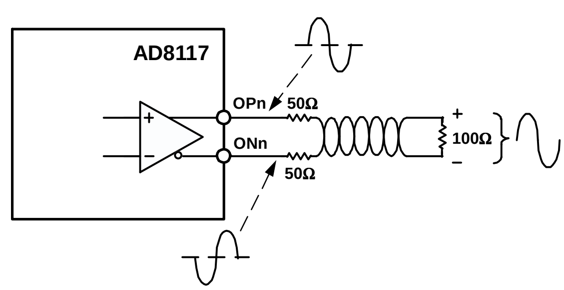


Figure 25. Example of Back-Terminated Differential Load

Single-ended Output

Usage

The AD8117/AD8118 output pairs can be used single-endedly, taking only one output and not using the second. This is often desired to reduce the routing complexity in the design, or because a single-ended load is being driven directly. This mode of operation will produce good results, but has some shortcomings when compared to taking the output differentially. When observing the single-ended output, noise that is common to both outputs appears in the output signal. This includes thermal noise in the chip biasing, as well as crosstalk that coupled into the signal path. This component noise and crosstalk is equal in both outputs, and as such can be ignored by a differential receiver with high common-mode rejection ratio. But when taking the output single-ended, this noise is present with respect to the ground (or VOCM) reference and is not rejected.

When observing the output single-ended, the distribution of offset voltages will appear greater. In the differential case, the difference between the outputs when the difference between the inputs is zero will be a small differential offset. This offset of created from mismatches in components of the signal path which must be corrected by the finite differential loop gain of the device. In the single-ended case, this differential offset is still observed, but an additional offset component is also relevant. This additional component is the common-mode offset, which is a difference between the average of the outputs and the VOCM reference. This offset is created by mismatches that affect the signal path in a common-mode manner, and is corrected by the finite common-mode loop gain of the device. A differential receiver would reject this common-mode offset voltage, but in the single ended case this offset is observed with respect to the signal ground. The single-ended output sums half the differential offset voltage and all of the common-mode offset voltage for a net gain in observed random offset.

Single-Ended Gain

The AD8117/AD8118 operates as a closed-loop differential amplifier. The primary control loop forces the difference between the output terminals to be a ratio of the difference between the input terminals. One output will increase in voltage, while the other decreases an equal amount to make the total difference correct. The average of these output voltages is forced to the voltage on the VOCM terminal by a second control loop. If only one output terminal is observed with respect to the VOCM terminal, only half of the difference voltage will be observed. This implies that when using only one output of the device, half of the differential gain will be observed. An AD8117 taken with single-ended output will appear to have a gain of +0.5. An AD8118 will be a single-ended gain of +1.

This factor of one-half in the gain increases the noise of the device when referred to the input, contributing to higher noise specifications for single-ended output designs.

Termination

When operating the AD8117/AD8118 with a single-ended output, the preferred output termination scheme is a resistor at the load end to the VOCM voltage. A back-termination may be used, at an additional cost of one half the signal gain.

In single-ended output operation, the second phase of the output is not used, and may or may not be terminated locally. Termination of the unused output is not necessary for proper device operation, so total design power dissipation can be reduced by floating this output. However, there are several reasons for terminating the unused output with a load resistance equal to the signal output.

One component of crosstalk is magnetic, coupling by mutual inductance between output package traces and bond wires that carry load current. In a differential design, there is coupling from one pair of outputs to other adjacent pairs of outputs. The differential nature of the output signal simultaneously drives the coupling field in one direction for one phase of the output, and in an opposite direction for the other phase of the output. These magnetic fields do not couple exactly equal into adjacent output pairs due to different proximities, but they do destructively cancel the crosstalk to some extent. If the load current in each output is equal, this cancellation will be greater and less adjacent crosstalk will be observed (regardless if the second output is actually being used).

A second benefit of balancing the output loads in a differential pair is to reduce fluctuations in current requirements from the power supply. In single-ended loads, the load currents alternate from the positive supply to the negative supply. This creates a parasitic signal voltage in the supply pins due to the finite resistance and inductance of the supplies. This supply fluctuation appears as crosstalk in all outputs, attenuated by the power supply rejection ratio (PSRR) of the device. At low frequencies, this is a negligible component of crosstalk, but PSRR falls off as frequency increases. With differential, balanced loads, as one output draws current from the positive supply, the other output draws current from the negative supply. When the phase alternates, the first output draws current from the negative supply and the second from the positive supply. The effect is that a more constant current is drawn from each supply, such that the crosstalk-inducing supply fluctuation is minimized.

A third benefit of driving balanced loads can be seen if one considers that the output pulse response will change as load changes. The differential signal control loop in the AD8117/AD8118 forces the difference of the outputs to be a fixed ratio to the difference of the inputs. If the two output responses are different due to loading, this creates a difference that the control loop will see as signal response error, and it will attempt to correct this error. This will distort the output signal from the ideal response if the two outputs were balanced.

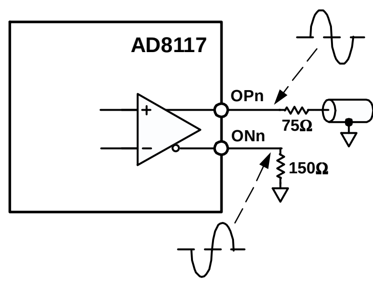


Figure 26. Example of Back-Terminated Single-Ended Load

Decoupling

The signal path of the AD8117/AD8118 is based on high open loop gain amplifiers with negative feedback. Dominant-pole compensation is used on-chip to stabilize these amplifiers over the range of expected applied swing and load conditions. To guarantee this designed stability, proper supply decoupling is necessary with respect to both the differential control loops and the common-mode control loops of the signal path. Signal-generated currents must return to their sources through low-impedance paths at all frequencies in which there is still loop gain (up to 700 MHz at a minimum). Refer to the example Evaluation Board schematic as an example of wideband parallel capacitor arrangements that can properly decouple the AD8117/AD8118.

The signal path compensation capacitors in the AD8117/AD8118 are connected to the VNEG supply. At high frequencies, this limits the power supply rejection ratio (PSRR) from the VNEG supply to a lower value than that from the VPOS supply. If given a choice, an application board should be designed such that the VNEG power is supplied from a low-inductance plane, subject to a least amount of noise.

The VOCM should be considered a reference pin and not a power supply. It is an input to the high-speed, high-gain common-mode control loop of all receivers and output drivers. In the single-ended output sense, there is no rejection from noise on the VOCM net to the output. For this reason, care must be taken to produce a low-noise VOCM source over the entire range of frequencies of interest. This is not only important to single-ended operation, but to differential operation as there is a common-mode to differential gain conversion that becomes greater at higher frequencies.

During operation of the AD8117/AD8118, transient currents will flow into the VOCM net from the amplifier control loops. Although the magnitude of these currents are small (10 – 20 μA per output), they can contribute to crosstalk if they flow through significant impedances. Driving VOCM with a low-impedance, low-noise source is desirable.

Power Dissipation

Calculation of Power Dissipation

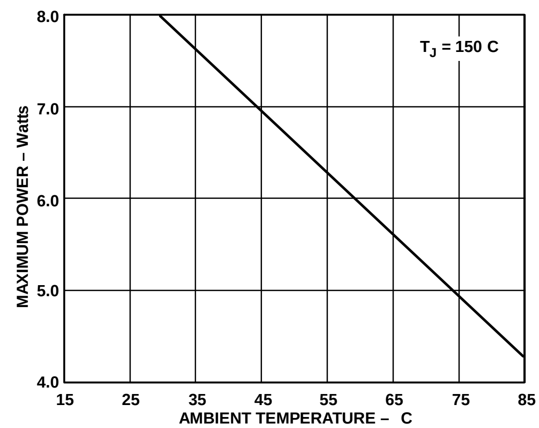


Figure 27. Maximum Die Power Dissipation vs. Ambient Temperature

The above curve was calculated from

$$P_{D,\,MAX} = \frac{(T_{JUNCTION,\,MAX} - T_{AMBIENT})}{\theta_{JA}}$$

As an example, if the AD8117/AD8118 is enclosed in an environment at 45°C (T_A), the total on-chip dissipation under all load and supply conditions must not be allowed to exceed 7.0 W.

When calculating on-chip power dissipation, it is necessary to include the rms current being delivered to the load, multiplied by the rms voltage drop on the AD8117/AD8118 output devices. For a sinusoidal output, the on-chip power dissipation due the load can be approximated by

$$P_{D,\,OUT} = (V_{POS} - V_{OUTPUT,\,RMS}) \times I_{OUTPUT,\,RMS}$$

For nonsinusoidal output, the power dissipation should be calculated by integrating the on-chip voltage drop multiplied by the load current over one period.

The user may subtract the quiescent current for the Class AB output stage when calculating the loaded power dissipation. For each output stage driving a load, subtract a quiescent power according to

$$P_{D,\ OUT,\ Q} = (V_{POS} - V_{NEG}) \times I_{OUTPUT,\ QUIESCENT}$$

For the AD8117/AD8118, $I_{OUTPUT,\ QUIESCENT}$ = 1.65 mA for each single-ended output pin.

For each disabled output, the quiescent power supply current in VPOS and VNEG drops by approximately 9 mA.

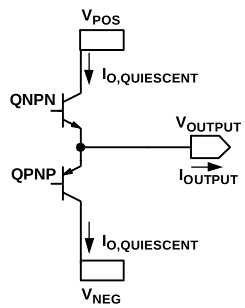


Figure 28. Simplified Output Stage

An example: AD8117, in an ambient temperature of 85°C, with all 32 outputs driving 1 V rms into 100 Ω loads. Power supplies are ± 2.5 V.

Step 1. Calculate power dissipation of AD8117 using data sheet quiescent currents. We are neglecting V_{DD} current as it is insignificant.

$$P_{D,\ QUIESCENT} = (V_{POS} \times I_{VPOS}) + (V_{NEG} \times I_{VNEG})$$

$$P_{D,\ QUIESCENT} = (2.5\ \text{V} \times 500\ \text{mA}) + (2.5\ \text{V} \times 500\ \text{mA}) = 2.5\ \text{W}$$

Step 2. Calculate power dissipation from loads. For a differential output and ground-referenced load, the output power is symmetrical in each output phase.

$$P_{D,\ OUTPUT} = (V_{POS} - V_{OUTPUT,\ RMS}) \times I_{OUTPUT,\ RMS}$$

$$P_{D,\ OUTPUT} = (2.5\ \text{V} - 1\ \text{V}) \times (1\ \text{V}/100\ \Omega) = 15\ \text{mW}$$

There are 32 output pairs, or 64 output currents.

$$nP_{D,\ OUTPUT} = 64 \times 15\ \text{mW} = 0.96\ \text{W}$$

Step 3. Subtract quiescent output stage current for number of loads (64 in this example). The output stage is either standing, or driving a load but the current only needs to be counted once (valid for output voltages > 0.5 V).

$$P_{DQ,\ OUTPUT} = (V_{POS} - V_{NEG}) \times I_{O,\ QUIESCENT}$$

$$P_{DQ,\ OUTPUT} = (2.5\ \text{V} - (-2.5\text{V})) \times (1.65\ \text{mA}) = 8.25\ \text{mW}$$

There are 32 output pairs, or 64 output currents.

$$nP_{D,\ OUTPUT} = 64 \times 8.25\ \text{mW} = 0.53\ \text{W}$$

Step 4. Verify that the power dissipation does not exceed maximum allowed value.

$$P_{D,\ ON\text{-}CHIP} = P_{D,\ QUIESCENT} + nP_{D,\ OUTPUT} + nP_{DQ,\ OUTPUT}$$

$$P_{D,\ ON\text{-}CHIP} = 2.5\ \text{W} + 0.96\ \text{W} - 0.53\ \text{W} = 2.9\ \text{W}$$

From the figure or the equation, this power dissipation is below the maximum allowed dissipation for all ambient temperatures up to and including 85°C.

Short Circuit Output Conditions

Although there is short-circuit current protection on the AD8117 outputs, the output current can reach values of 80 mA into a grounded output. Any sustained operation with too many shorted outputs can exceed the maximum die temperature and can result in device failure (see Absolute Maximum Ratings).

Crosstalk

Many systems, such as broadcast video and KVM switches, that handle numerous analog signal channels, have strict requirements for keeping the various signals from influencing any of the others in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in close proximity in a system, as will undoubtedly be the case in a system that uses the AD8117/AD8118, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required in order to specify a system that uses one or more crosspoint devices.

Types of Crosstalk

Crosstalk can be propagated by means of any of three methods. These fall into the categories of electric field, magnetic field, and sharing of common impedances. This section will explain these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (e.g., free space) and couples with the receiver and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields then generate voltages in any other conductors whose paths they link. The undesired induced voltages in these other channels are crosstalk signals. The channels that crosstalk can be said to have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds, and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows in one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities, so the magnitudes cannot simply be added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can actually reduce the crosstalk. The fact that the AD8117/AD8118 is a fully-differential design means that many sources of crosstalk either destructively cancel, or are common-mode to the signal and can be rejected by a differential receiver.

Areas of Crosstalk

A practical AD8117/AD8118 circuit must be mounted to some sort of circuit board in order to connect it to power supplies and measurement equipment. Great care has been taken to create a characterization board (also available as an evaluation board) that adds minimum crosstalk to the intrinsic device. This, however, raises the issue that a system's crosstalk is a combination of the intrinsic crosstalk of the devices in addition to the circuit board to which they are mounted. It is important to try to separate these two areas when attempting to minimize the effect of crosstalk.

In addition, crosstalk can occur among the inputs to a crosspoint and among the outputs. It can also occur from input to output. Techniques will be discussed for diagnosing which part of a system is contributing to crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by

$$|XT| = 20 \log_{10} (A_{SEL}(s) / A_{TEST}(s))$$

where $s = j\omega$ is the Laplace transform variable, $A_{SEL}(s)$ is the amplitude of the crosstalk induced signal in the selected channel, and $A_{TEST}(s)$ is the amplitude of the test signal. It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to first order). In addition, the crosstalk signal will have a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 32 × 32 matrix of the AD8117, we can look at the number of crosstalk terms that can be considered for a single channel, say the IN00 input. IN00 is programmed to connect to one of the AD8117 outputs where the measurement can be made.

First, the crosstalk terms associated with driving a test signal into each of the other 31 inputs can be measured one at a time, while applying no signal to IN00. Then the crosstalk terms associated with driving a parallel test signal into all 31 other inputs can be measured two at a time in all possible combinations, then three at a time, and so on, until, finally, there is only one way to drive a test signal into all 31 other inputs in parallel.

Each of these cases is legitimately different from the others and might yield a unique value, depending on the resolution of the measurement system, but it is hardly practical to measure all these terms and then specify them. In addition, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other outputs (not used for measurement) are taken into consideration, the numbers rather quickly grow to astronomical proportions. If a larger crosspoint array of multiple AD8117s is constructed, the numbers grow larger still.

Obviously, some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure all hostile crosstalk; this means that the crosstalk to the selected channel is measured while all other system channels are driven in parallel. In general, this will yield the worst crosstalk number, but this is not always the case, due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those created by one nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements will generally be higher than those of more distant channels, so they can serve as a worst-case measure for any other one-channel or two-channel crosstalk measurements.

Input and Output Crosstalk

Capacitive coupling is voltage-driven (dV/dt), but is generally a constant ratio. Capacitive crosstalk is proportional to input or output voltage, but this ratio is not reduced by simply reducing signal swings. Attenuation factors must be changed by changing impedances (lowering mutual capacitance), or destructive canceling must be utilized by summing equal and out of phase components. For high-input impedance devices such as the AD8117/AD8118, capacitances generally dominate input-generated crosstalk.

Inductive coupling is proportional to current (dI/dt), and will often scale as a constant ratio with signal voltage, but will also show a dependence on impedances (load current). Inductive coupling can also be reduced by constructive canceling of equal and out of phase fields. In the case of driving low-impedance video loads, output inductances contribute highly to output crosstalk.

The flexible programming capability of the AD8117/AD8118 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. Some examples are illustrative. A given input pair (IN07 in the middle for this example) can be programmed to drive OUT07 (also in the middle). The inputs to IN07 are just terminated to ground (via 50 Ω or 75 Ω) and no signal is applied.

All the other inputs are driven in parallel with the same test signal (practically provided by a distribution amplifier), with all other outputs except OUT07 disabled. Since grounded IN07 is programmed to drive OUT07, no signal should be present. Any signal that is present can be attributed to the other 15 hostile input signals, because no other outputs are driven (they are all disabled). Thus, this method measures the all-hostile input contribution to crosstalk into IN07. Of course, the method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel is driven (IN00, for example) and all outputs other than a given output (IN07 in the middle) are programmed to connect to IN00. OUT07 is programmed to connect to IN15 (far away from IN00), which is terminated to ground. Thus OUT07 should not have a signal present since it is listening to a quiet input. Any signal measured at the OUT07 can be attributed to the output crosstalk of the other 16 hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Thus, the PC board on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies the magnitude of the crosstalk will be given by

$$|XT| = 20 \log_{10}[(R_S C_M) \times s]$$

where R_S is the source resistance, C_M is the mutual capacitance between the test signal circuit and the selected circuit, and s is the Laplace transform variable.

From the equation it can be observed that this crosstalk mechanism has a high-pass nature; it can also be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8117 is specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk will be higher than the minimum obtainable due to the high output currents. These currents will induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8117.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer with a mutual inductance between the windings that drives a load resistor. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20 \log_{10} (M_{XY} \times s/R_L)$$

where M_{XY} is the mutual inductance of output X to output Y and R_L is the load resistance on the measured output. This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

PCB Layout

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully detailed are grounding, shielding, signal routing, and supply bypassing.

The packaging of the AD8117/AD8118 is designed to help keep the crosstalk to a minimum. On the BGA substrate, each pair is carefully routed to predominately couple to each other, with shielding traces separating adjacent signal pairs. The ball grid array is arranged such that similar board routing can be achieved. Only the outer two rows are used for signals, such that vias can be used to take the input rows to a lower signal plane if desired.

The input and output signals will have minimum crosstalk if they are located between ground planes on layers above and below, and separated by ground in between. Vias should be located as close to the IC as possible to carry the inputs and outputs to the inner layer. The input and output signals surface at the input termination resistors and the output series back-termination resistors. To the extent possible, these signals should also be separated as soon as they emerge from the IC package.

PCB Termination Layout

As frequencies of operation increase, the importance of proper transmission line signal routing becomes more important. The bandwidth of the AD8117/AD8118 is large enough that using high impedance routing will not provide a flat in-band frequency response for practical signal trace lengths. It is necessary for the user to choose a characteristic impedance suitable for the application and properly terminate the input and output signals of the AD8117/AD8118. Traditionally, video applications have used 75 Ω single-ended enviroments. RF applications are generally 50 Ω single-ended (and board manufacturers have the most experience with this application). CAT-5 cabling is usually driven as differential pairs of 100 Ω differential impedance.

For flexibility, the AD8117/AD8118 does not contain on-chip termination resistors. This flexibility in application comes with some board layout challenges. The distance between the termination of the input transmission line and the AD8117/AD8118 die is a high-impedance stub, and will cause reflections of the input signal. With some simplification, it can be shown that these reflections will cause peaking of the input at regular intervals in frequency, dependent on the propagation speed (V_P) of the signal in the choosen board material and the distance (d) between the termination resistor and the AD8117/AD8118. If the distance is great enough, these peaks can occur in-band. In fact, practical experience shows that these peaks are not high-Q, and should be pushed out to three or four times the desired bandwidth in order to not have an effect on the signal. For a board designer using FR4 (V_P = 144 $\times 10^6$ m/s), this means the AD8117/AD8118 should be no more than 1.5 cm after the termination resistors, and preferably should be placed even closer. The BGA substrate routing inside the AD8117/AD8118 is approximately 1 cm in length and adds to the stub length, so 1.5 cm PCB routing equates to $d = 2.5 \times 10^{-2}$ m in the calculations.

$$f_{peak} = \frac{(2n+1)V_P}{4d}, \quad n = \{0, 1, 2, 3, \ldots\}$$

In some cases, it is difficult to place the termination close to the AD8117/AD8118 due to space constraints, differential routing, and large resistor footprints. A preferable solution in this case is to maintain a controlled transmission line past the AD8117/AD8118 inputs and terminate the end of the line. This is known as fly-by termination. The input impedance of the AD8117/AD8118 is large enough and stub length inside the package is small enough that this works well in practice. Implementation of fly-by input termination often includes bringing the signal in on one routing layer, then passing through a filled-via under the AD8117/AD8118 input ball, then back out to termination on another signal layer. In this case, care must be taken to tie the reference ground planes together near the signal via if the signal layers are referenced to different ground planes.

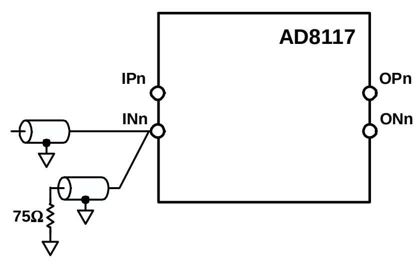


Figure 29. Fly-by Input Termination. Grounds for the two transmission lines shown must be tied together close to the INn pin.

If multiple AD8117/AD8118 are to be driven in parallel, a fly-by input termination scheme is very useful, but the distance from each AD8117/AD8118 input to the driven input transmission line is a stub that should be minimized in length and parasitics using the discussed guidelines.

When driving the AD8117/AD8118 single-endedly, the undriven input is often terminated with a resistance in order to balance the input stage. It can be seen that by terminating the undriven input with a resistor of one-half the characteristic impedance, the input stage will be perfectly balanced (37.5 Ω, for example, to balance the two parallel 75 Ω terminations on the driven input). However, due to the feedback in the input receiver, there is high-speed signal current leaving the undriven input. In order to terminate this high-speed signal, proper transmission-line techniques should be used. One solution is to adjust the trace width to create a transmission line of half the characteristic impedance and terminate the far end with this resistance (37.5 Ω in a 75 Ω system). This is not often practical as trace widths become large. In most cases, the best practical solution is to place the half-characteristic impedance resistor as close as possible (preferably less than 1.5 cm away) and to reduce the parasitics of the stub (by removing the ground plane under the stub, for example). In either case, the designer must decide if the layout complexity created by a balanced, terminated solution is preferable to simply grounding the undriven input at the ball with no trace.

While the examples discussed so far are for input termination, the theory is similar for output back-termination. Taking the AD8117/AD8118 as an ideal voltage source, any distance of routing between the AD8117/AD8118 and a back-termination resistor will be a stub that will create reflections. For this reason, back-termination resistors should also be placed close to the AD8117/AD8118. In practice, because back-termination resistors are series elements, their footprint in the routing is narrower and it is easier to place them close in board layout.

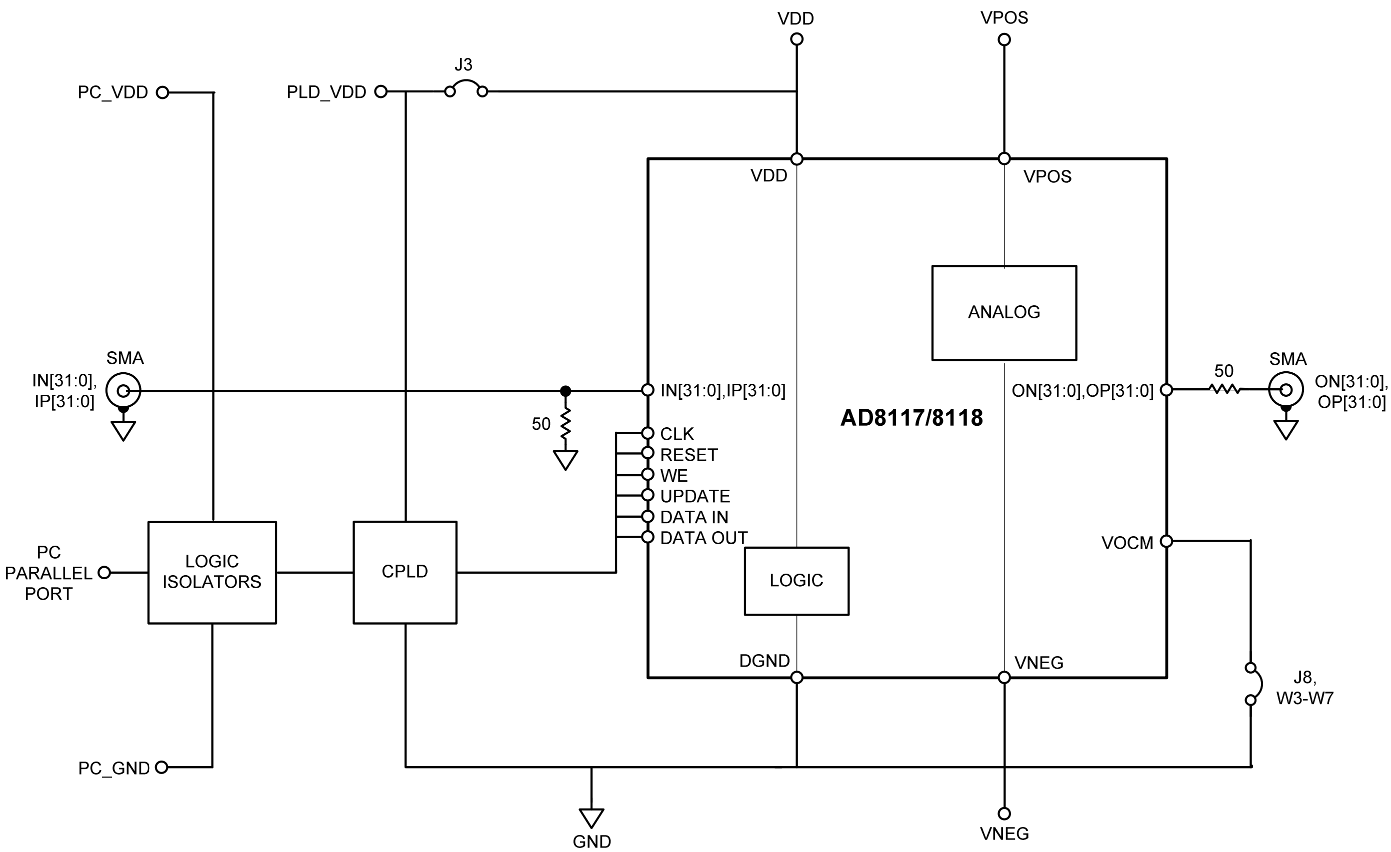


Figure 30. Evaluation Board Simplified Schematic

OUTLINE DIMENSIONS

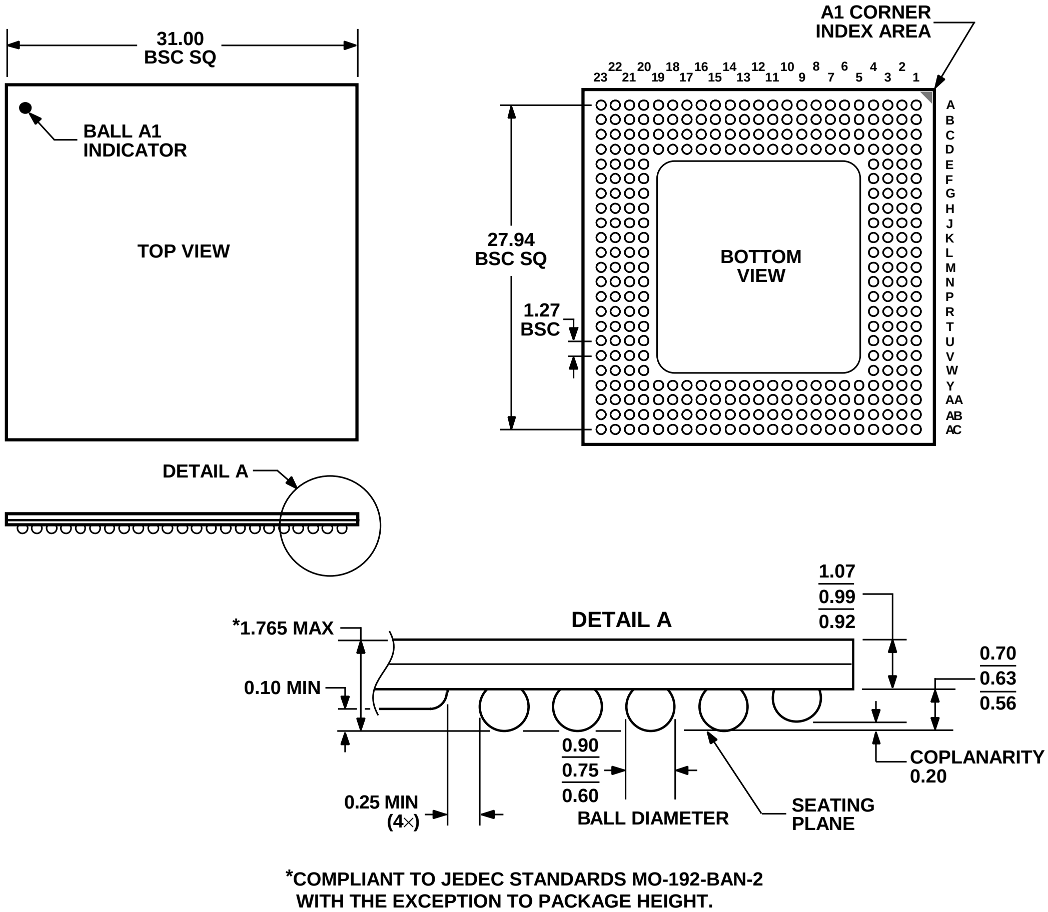


Figure 31. 304-Lead Ball Grid Array, Thermally Enhanced [BGA_ED]
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8117ABPZ	−40°C to +85°C	304-Lead Ball Grid Array Package [BGA_ED] (31 × 31 mm)	SBGA-304
AD8118ABPZ	−40°C to +85°C	304-Lead Ball Grid Array Package [BGA_ED] (31 × 31 mm)	SBGA-304
AD8117-EVAL		AD8117 Evaluation Kit	

NOTE: Z suffix denotes lead-free package.

NOTES

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