

8-bit parallel-access shift register

74F199

FEATURES

- Buffered clock and control inputs
- Shift right and parallel load capability
- Fully synchronous data transfers
- J- \bar{K} (D) inputs to first stage
- Clock enable for hold (do nothing) mode
- Asynchronous Master Reset

DESCRIPTION

The 74F199 is an 8-bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic Diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The 74F199 operates in two primary modes: shift right (Q0→Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\bar{P}E$) input. Serial data enters the first flip-flop (Q0) via the J and \bar{K} inputs when the $\bar{P}E$ input is High, and is shifted one bit in the direction Q0→Q1→Q2 following each Low-to-High clock transition.

The J and \bar{K} inputs provide the flexibility of the J-K type input for special applications, and by tying the two together the simple D-type input is made for general applications.

The device appears as eight common clocked D flip-flops when the $\bar{P}E$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D0–D7) is transferred to the respective Q0–Q7 outputs.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F199 utilizes edge-triggered, therefore there is no restriction on the activity of the J, \bar{K} , Dn, and $\bar{P}E$ inputs for logic operation, other than the setup and hold time requirements.

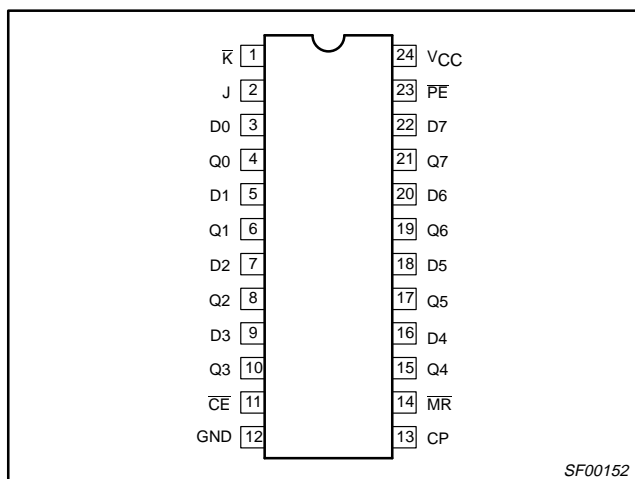
A Low on the Master Reset ($\bar{M}R$) input overrides all other inputs and clears the register asynchronously forcing all bit positions to a Low state.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Parallel data inputs	1.0/1.0	20 μ A/0.6mA
J, \bar{K}	J and K inputs	1.0/1.0	20 μ A/0.6mA
$\bar{P}E$	Parallel Enable input	1.0/1.0	20 μ A/0.6mA
$\bar{C}E$	Clock Enable input	1.0/1.0	20 μ A/0.6mA
DP	Clock Pulse inputs (Active rising edge)	1.0/1.0	20 μ A/0.6mA
$\bar{M}R$	Master Reset input (Active Low)	1.0/1.0	20 μ A/0.6mA
Q0–Q7	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F199	95MHz	70mA

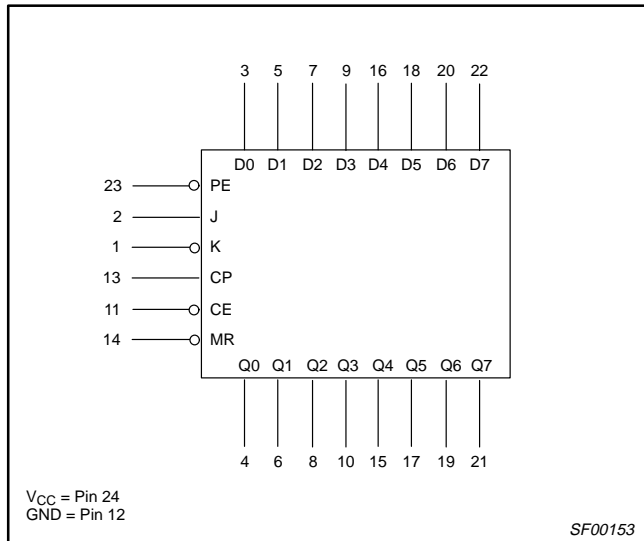
ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
24-pin plastic slim DIP (300mil)	N74F199N
24-pin plastic SOL	N74F199D

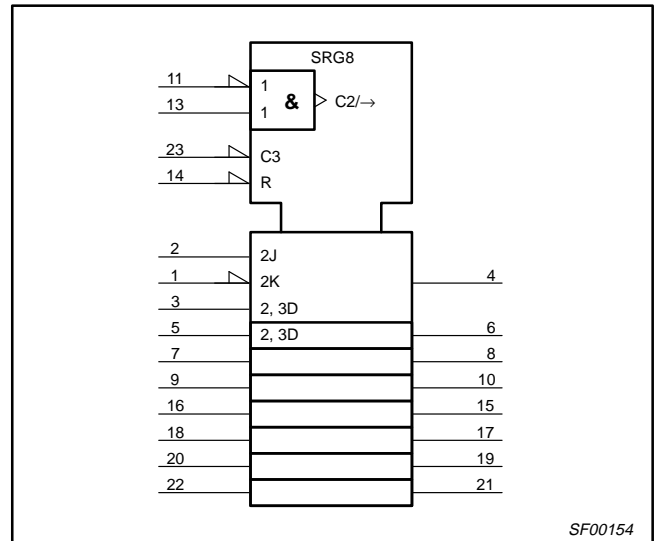
8-bit parallel-access shift register

74F199

LOGIC SYMBOL



IEEE/IEC SYMBOL



FUNCTION TABLE

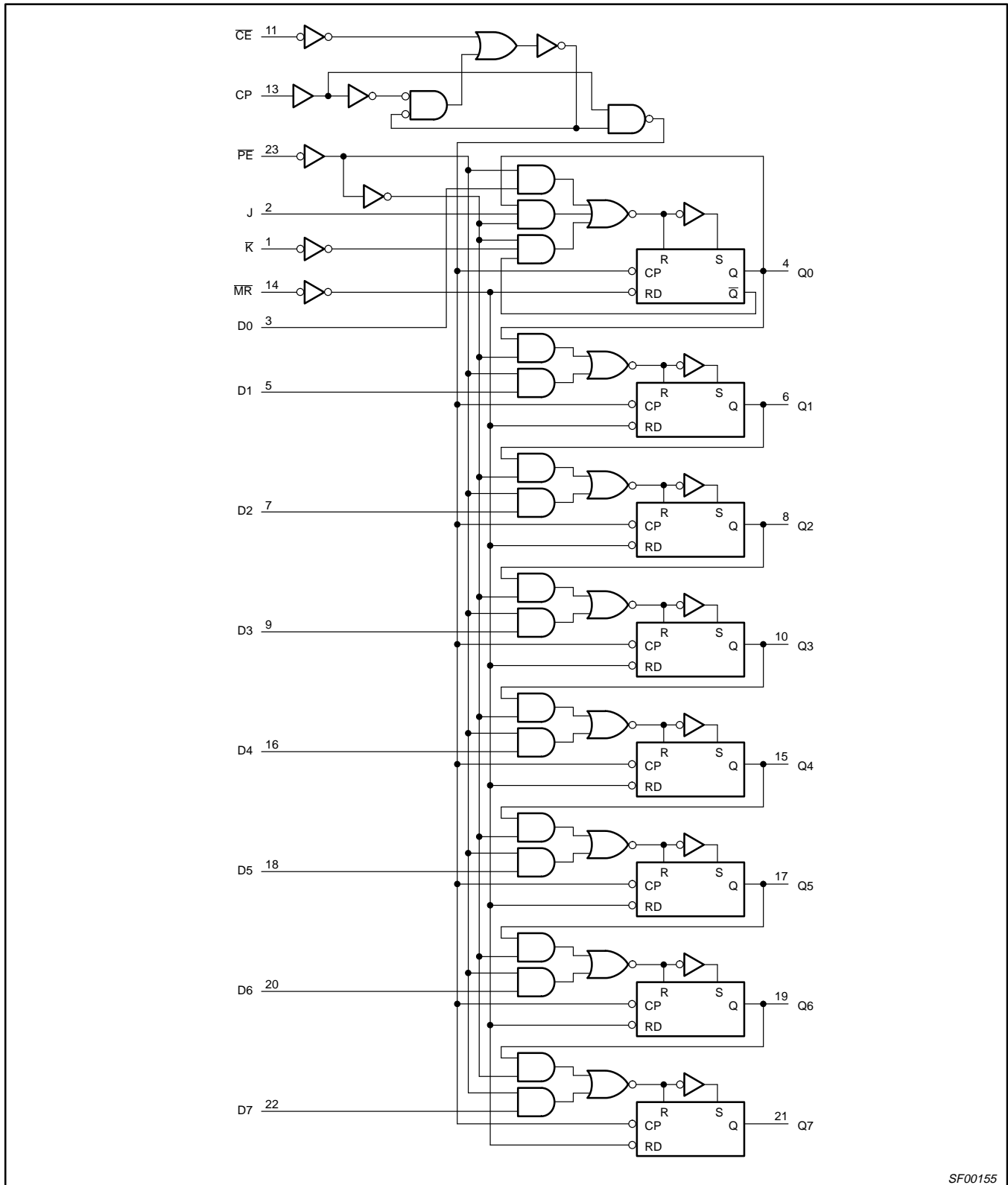
INPUTS							OUTPUTS					OPERATING MODES
MR	CP	CE	PE	J	K	Dn	Q0	Q1	...	Q6	Q7	
L	X	X	X	X	X	X	L	L	...	L	L	Reset (clear)
H	↑	l	h	h	h	X	H	q0	...	q5	q6	Shift, set First stage
H	↑	l	h	l	l	X	L	q0	...	q5	q6	Shift, reset First stage
H	↑	l	h	h	l	X	$\bar{q}0$	q0	...	q5	q6	Shift, toggle First stage
H	↑	l	h	l	h	X	q0	q0	...	q5	q6	Shift, retain First stage
H	↑	l	l	X	X	dn	d0	d1	...	d6	d7	Parallel load
H	↑	h	X	X	X	X	q0	q1	...	q6	q7	Hold (do nothing)

- H = High voltage level
- h = High voltage level one setup time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one setup time prior to the Low-to-High clock transition
- X = Don't care
- ↑ = Low-to-High clock transition
- dn(qn) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition

8-bit parallel-access shift register

74F199

LOGIC DIAGRAM

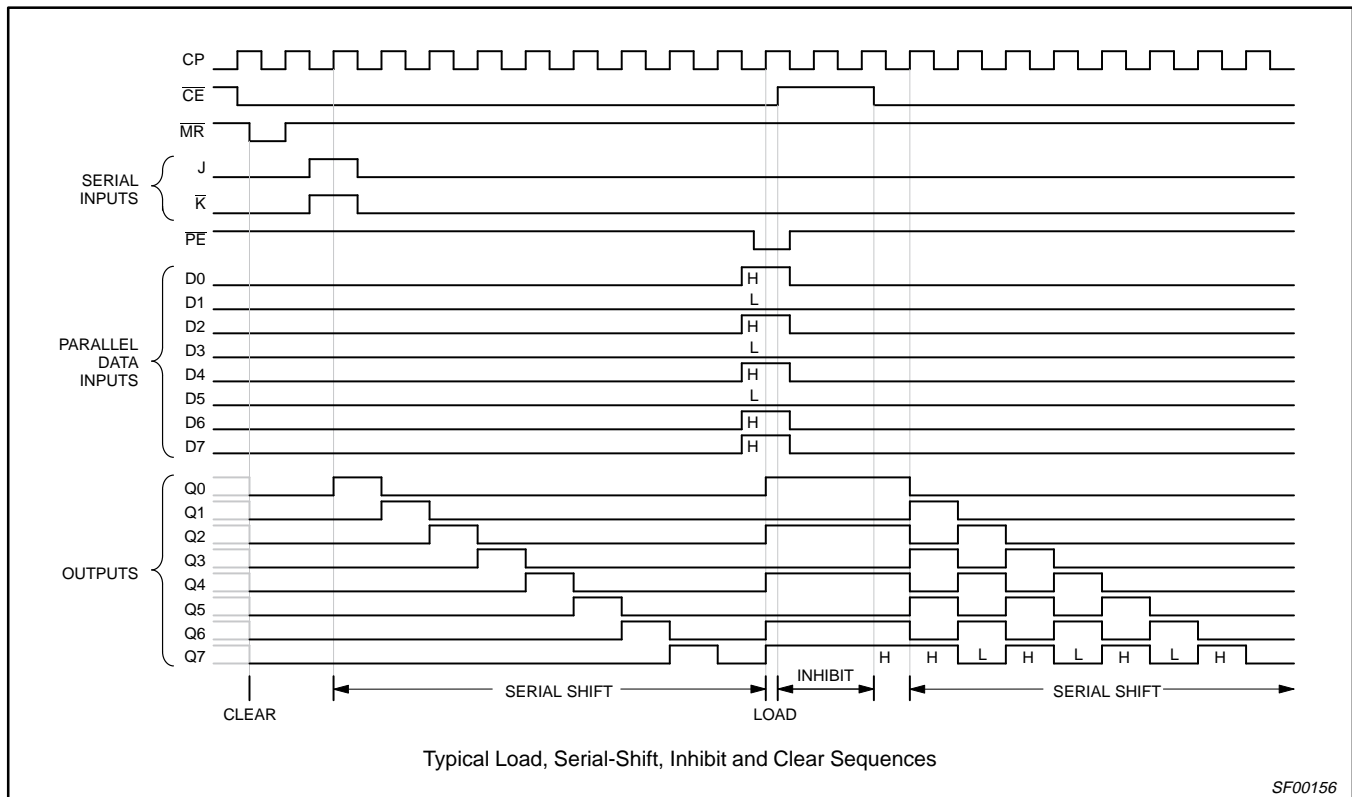


SF00155

8-bit parallel-access shift register

74F199

TYPICAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	40	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _{amb}	Operating free-air temperature range	0		+70	°C

8-bit parallel-access shift register

74F199

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		LIMITS			UNIT
				MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}	2.5			V
		V _{IH} = MIN, I _{OH} = MAX	±5%V _{CC}	2.7	3.4		
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}		0.35	0.50	V
		V _{IH} = MIN, I _{OL} = MAX	±5%V _{CC}		0.35	0.50	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				100	μA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V				-0.6	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-60		-150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX		65	90	mA
		I _{CCL}			75	105	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

8-bit parallel-access shift register

74F199

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Qn	Waveform 1	5.5 6.5	8.0 9.5	11.0 12.5	4.5 3.5	12.0 13.5	ns
t _{PHL}	Propagation delay MR to Qn	Waveform 2	5.5	8.0	10.5	5.0	12.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _S (H) t _S (L)	Setup time, High or Low Dn to CP	Waveform 3	0.0 1.5			0.0 2.5		ns
t _H (H) t _H (L)	Hold time, High or Low Dn to CP	Waveform 3	2.0 4.5			2.5 5.5		ns
t _S (H) t _S (L)	Setup time, High or Low J, K to CP	Waveform 3	0.0 2.5			0.0 3.0		ns
t _H (H) t _H (L)	Hold time, High or Low J, K to CP	Waveform 3	0.0 3.5			0.0 4.0		ns
t _S (H) t _S (L)	Setup time, High or Low CE to CP	Waveform 3	0.0 2.5			0.0 3.0		ns
t _H (H) t _H (L)	Hold time, High or Low CE to CP	Waveform 3	0.0 4.5			0.0 5.5		ns
t _S (H) t _S (L)	Setup time, High or Low PE to CP	Waveform 3	8.0 8.0			9.0 9.0		ns
t _H (H) t _H (L)	Hold time, High or Low PE to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
t _w (H)	CP pulse width, High	Waveform 1	4.5			5.5		ns
t _w (L)	MR pulse width, Low	Waveform 2	4.0			4.5		ns
t _{rec}	Recovery time MR to CP	Waveform 2	5.5			6.5		ns

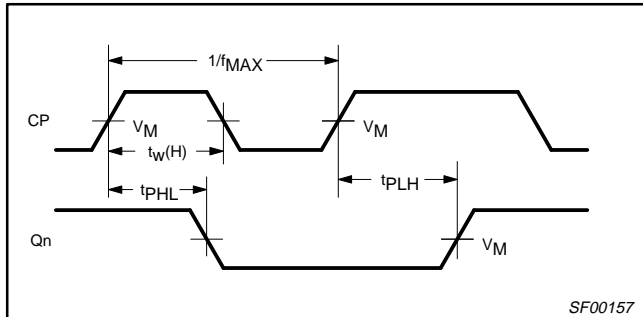
8-bit parallel-access shift register

74F199

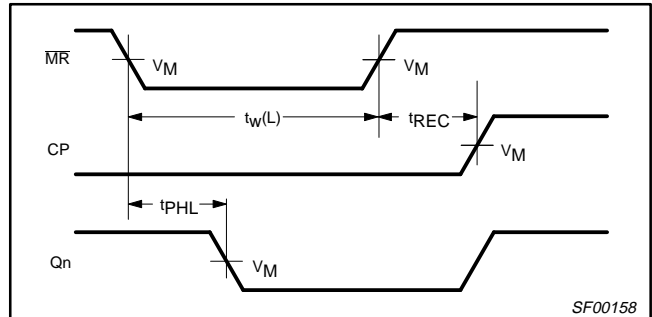
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

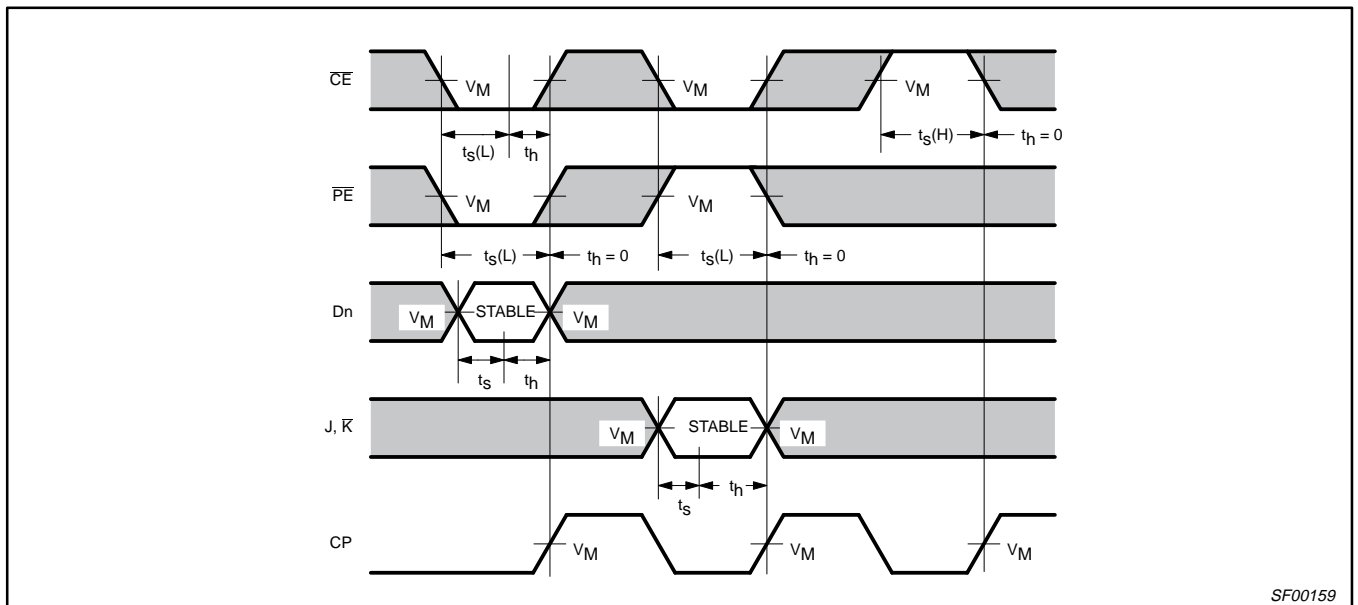
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



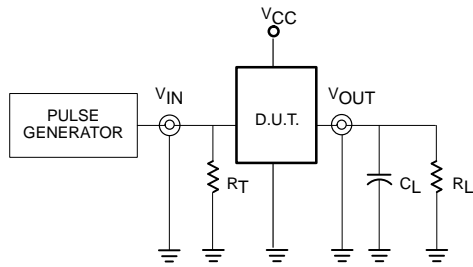
Waveform 3. Setup Time and Hold Time

SF00159

8-bit parallel-access shift register

74F199

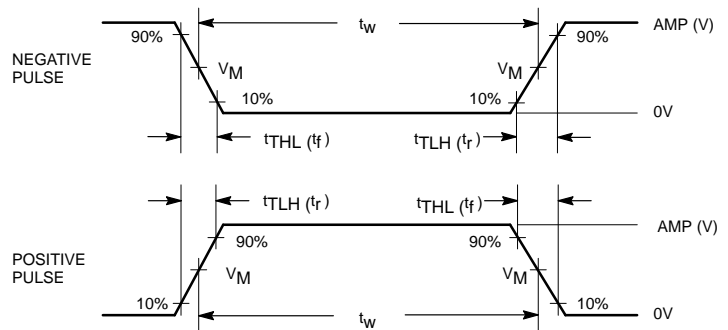
TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	$t_{TLH} (t_r)$	$t_{THL} (t_f)$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006