

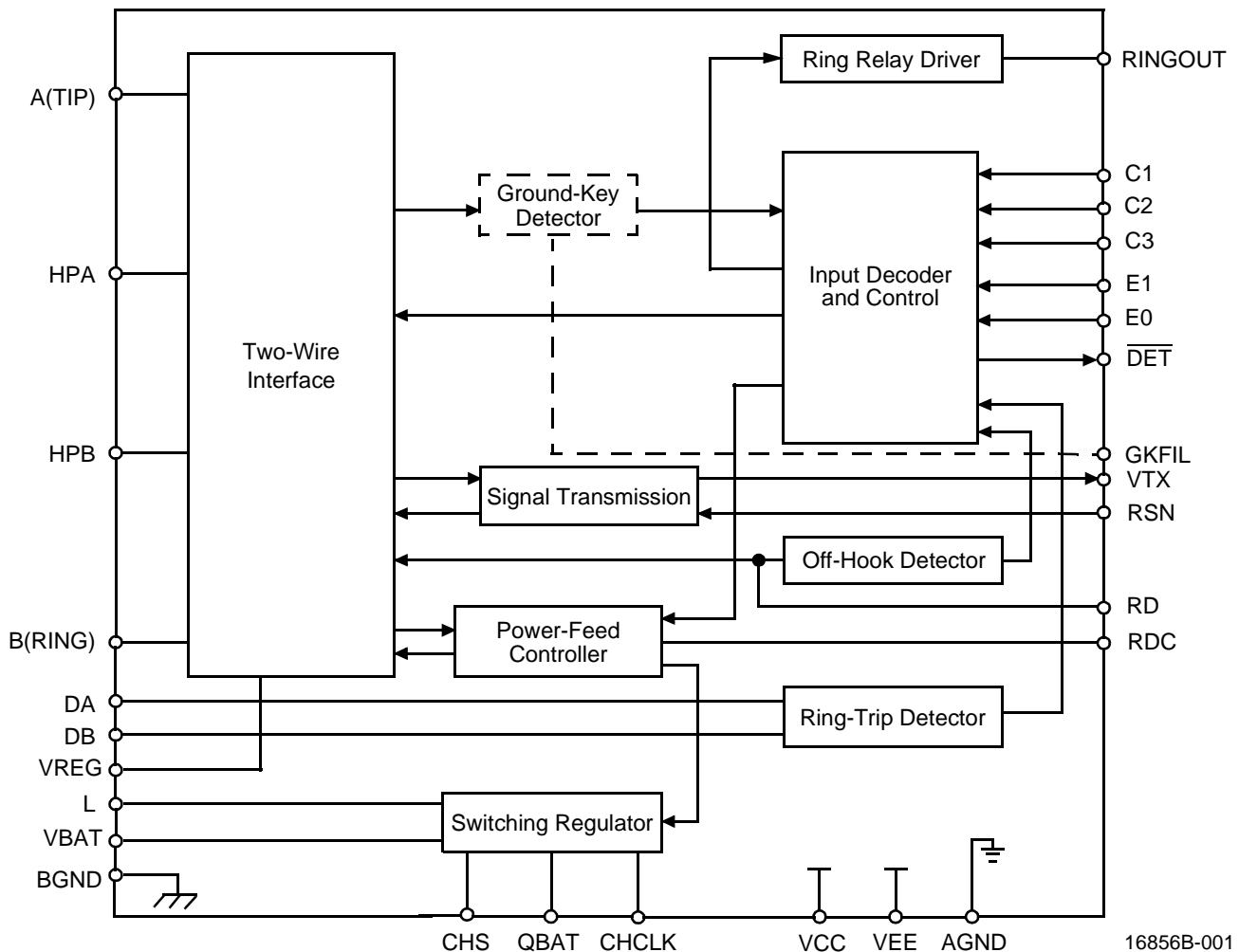
# Am79M535

## Metering Subscriber Line Interface Circuit

### DISTINCTIVE CHARACTERISTICS

- Programmable constant-current feed
- Line-feed characteristics independent of battery variations
- Programmable loop-detect threshold
- On-chip switching regulator for low-power dissipation
- Pin for external ground-key noise filter capacitor available
- Ground-key detect
- Two-wire impedance set by single external impedance
- Performs polarity reversal
- Tip Open state for ground-start lines
- Supports 2.2 Vrms metering (12 and 16 kHz)
- On-hook transmission

### BLOCK DIAGRAM



16856B-001

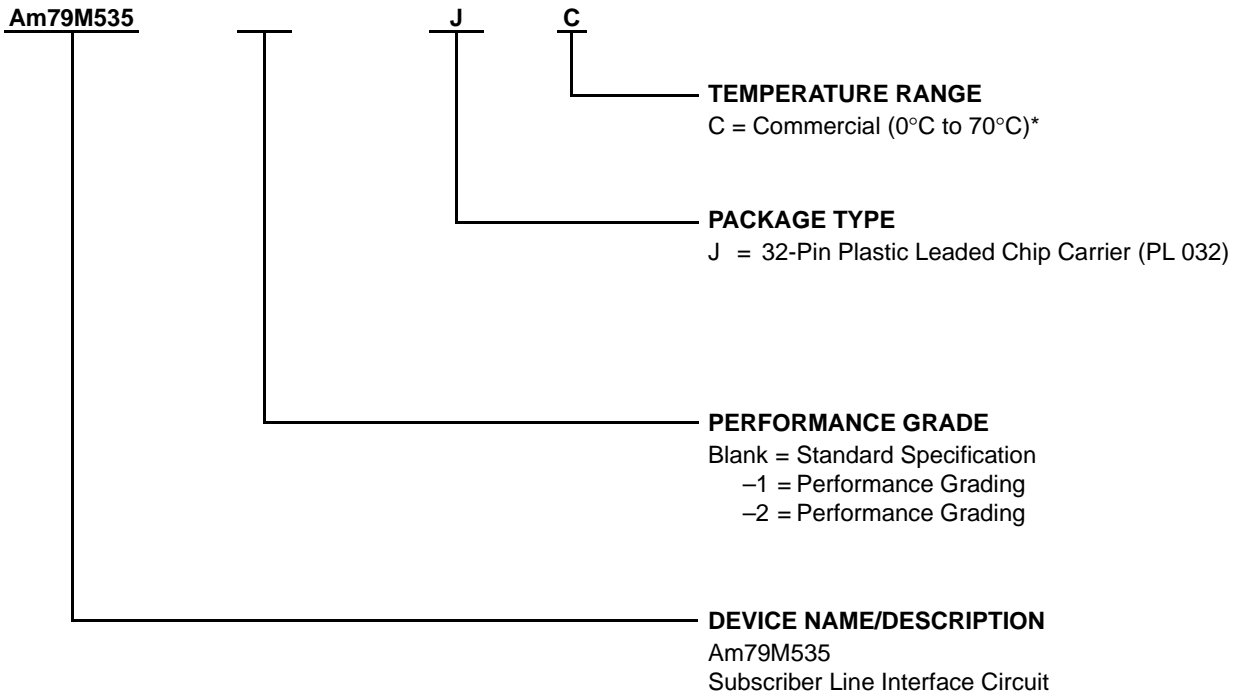
#### Notes:

1. Am79M535—E0 and E1 inputs; ring relay driver sourced internally to BGND; ground-key filter pin.
2. Current gain ( $K_1$ ) = 1000.

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am79M535	-1	JC
	-2	

#### Valid Combinations

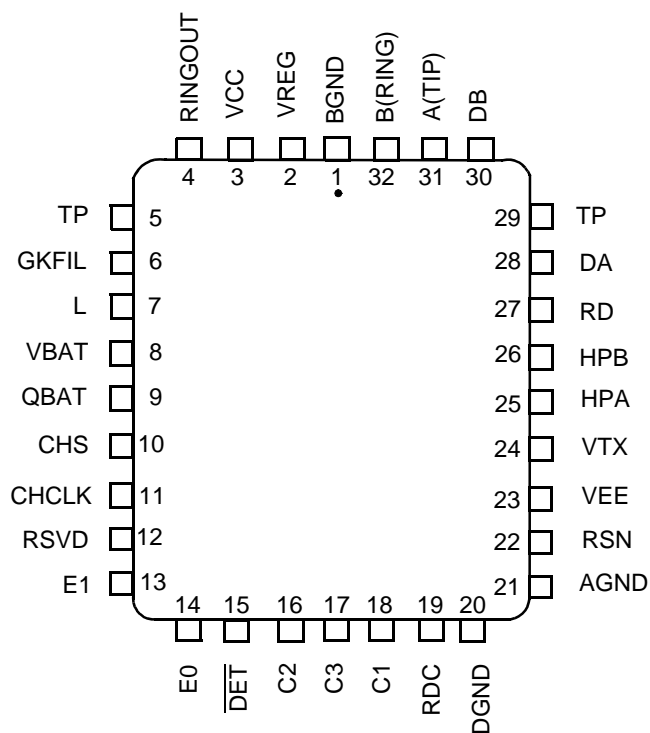
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

**Note:**

\* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterizations and periodic sampling of production units.

## CONNECTION DIAGRAM

### Top View



#### Notes:

1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (QBAT).
3. RSVD = Reserved. Do not connect to this pin.

## PIN DESCRIPTIONS

Pin Names	Type	Description
AGND	Gnd	Analog (quiet) ground
DGND	Gnd	Digital ground
A(TIP)	Output	Output of A(TIP) power amplifier
BGND	Gnd	Battery (power) ground
B(RING)	Output	Output of B(RING) power amplifier
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
CHCLK	Input	Chopper Clock. Input to switching regulator (TTL compatible). Freq = 256 kHz (Nominal).
CHS	Input	Chopper stabilization. Connection for external stabilization components.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator
DB	Input	Ring-trip positive. Positive input to ring-trip comparator
$\overline{\text{DET}}$	Output	Detector. When enabled, logic Low indicates that the selected detector is tripped. Logic inputs C3–C1, E1, and E0 select the detector. Open-collector with a built-in 15 k $\Omega$ pull-up resistor.
E0	Input	Read Enable. A logic Low disables $\overline{\text{DET}}$ . A logic High enables $\overline{\text{DET}}$ .
E1	Input	Ground-Key Enable. When E0 is High, E1 = High connects the ground-key detector to $\overline{\text{DET}}$ , and E1 = Low connects the off-hook or ring-trip detector to $\overline{\text{DET}}$ .
GKFIL	Capacitor	Ground-Key Filter Capacitor Connection. An external capacitor for filtering out high-frequency noise from the ground-key loop can be connected to this pin. An internal 36 k $\Omega$ –20%, +40% resistor is provided to form an RC filter with the external capacitor. In versions which have a GKFIL pin, a 3.3 nF minimum capacitance must be connected from the GKFIL pin to ground.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
L	Output	Switching Regulator Power Transistor. Connection point for filter inductor and anode of catch diode. Has up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Keep the diode connections short because of the high currents and high di/dt
QBAT	Battery	Quiet Battery. Filtered battery supply for the signal processing circuits.
RD	Resistor	Detector resistor. Threshold modification and filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the Receiver Summing Node (RSN). $V_{\text{RDC}}$ is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring Relay Driver. Sourcing from BGND with internal diode to $Q_{\text{BAT}}$ .
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Route the 256 kHz chopper clock and switch lines away from the RSN node.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.
VBAT	Battery	Connected to office battery supply through an external protection diode.
VCC	Power	+5 V power supply
VEE	Power	–5 V power supply
VREG	Input	Regulated Voltage. Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio. This output is 0.510 times the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

**ABSOLUTE MAXIMUM RATINGS**

Storage temperature . . . . .	-55°C to +150°C
V <sub>CC</sub> with respect to AGND/DGND . . .	-0.4 V to +7.0 V
V <sub>EE</sub> with respect to AGND/DGND . . .	+0.4 V to -7.0 V
V <sub>BAT</sub> with respect to AGND/DGND . . .	+0.4 V to -70 V
<b>Note:</b> Rise time of V <sub>BAT</sub> (dv/dt) must be limited to 27 V/μs or less when Q <sub>BAT</sub> bypass = 0.33 μF.	
BGND with respect to	
AGND/DGND . . . . .	+1.0 V to -3.0 V
A(TIP) or B(RING) to BGND:	
Continuous . . . . .	-70 V to +1.0 V
10 ms (f = 0.1 Hz) . . . . .	-70 V to +5.0 V
1 μs (f = 0.1 Hz) . . . . .	-90 V to +10 V
250 ns (f = 0.1 Hz) . . . . .	-120 V to +15 V
Current from A(TIP) or B(RING) . . . . .	±150 mA
Voltage on RINGOUT . . . . .	BGND to 70 V above Q <sub>BAT</sub>
Current through relay driver . . . . .	60 mA
Voltage on ring-trip input	
(DA and DB) . . . . .	V <sub>BAT</sub> to 0 V
Current into ring-trip inputs . . . . .	±10 mA
Peak current into regulator	
switch (L pin) . . . . .	150 mA
Switcher transient peak off	
voltage on L pin . . . . .	+1.0 V
C3-C1, E0, E1, CHCLK to	
AGND/DGND . . . . .	-0.4 V to V <sub>CC</sub> + 0.4 V
Maximum power dissipation, (see note) . . .	T <sub>A</sub> = 70°C
In 32-pin PLCC package . . . . .	1.74 W

**Note:** Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

**OPERATING RANGES****Commercial (C) Devices**

Ambient temperature . . . . .	0°C to +70°C*
V <sub>CC</sub> . . . . .	4.75 V to 5.25 V
V <sub>EE</sub> . . . . .	-4.75 V to -5.25 V
V <sub>BAT</sub> . . . . .	-40 V to -58 V
AGND/DGND . . . . .	0 V
BGND with respect to	
AGND/DGND . . . . .	-100 mV to +100 mV
Load resistance on VTX to ground . . . . .	10 kΩ min

*Operating Ranges define those limits between which the functionality of the device is guaranteed.*

*\* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterizations and periodic sampling of production units.*

## ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note	
Analog ( $V_{TX}$ ) output impedance			3		$\Omega$	4	
Analog ( $V_{TX}$ ) output offset	0°C to 70°C	-35		+35	mV	—	
		-30		+30		—	
	-40°C to +85°C	-40		+40		4	
		-1		+35		4	
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	$\Omega$	4	
Longitudinal impedance at A or B				35			
Overload level	4-wire	-3.1		+3.1	Vpk		
$Z_{2WIN} = 600$ to $900 \Omega$	2-wire	-6.0		+6.0		2	
<b>Transmission Performance, 2-Wire Impedance</b>							
2-wire return loss (See Test Circuit D)	300 Hz to 500 Hz	26			dB	4, 13	
	500 Hz to 2500 Hz	26					
	2500 Hz to 3400 Hz	20					
<b>Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C)</b>							
$R_L = 600 \Omega$ , Longitudinal to metallic L-T, L-4 (normalized to unity gain)	300 Hz to 3400 Hz		48		dB		
		-1*	52				
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz					—	
	normal polarity 0°C to +70°C	-2*	63			—	
	normal polarity -40°C to +85°C	-2	58			4	
	reverse polarity	-2	54			—	
	1 kHz to 3.4 kHz					—	
	normal polarity 0°C to +70°C	-2*	58			—	
normal polarity -40°C to +85°C	-2	54		4			
reverse polarity	-2	54		—			
Longitudinal signal generation 4-L	300 Hz to 800 Hz	40					
	300 Hz to 800 Hz	-1*	42				
Longitudinal current capability per wire	Active state		25		mArms	4	
	OHT state		18			4	
<b>Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B)</b>							
Gain accuracy 2- to 4-wire	0 dBm, 1 kHz, 0°C to +70°C	5.75	5.85	6.00	dB	—	
	0 dBm, 1 kHz, -40°C to +85°C	5.65	5.85	6.05		4	
	0 dBm, 1 kHz, 0°C to +70°C	-1*	5.75	5.85		5.95	—
	0 dBm, 1 kHz, -40°C to +85°C	-1	5.70	5.85		6.00	4
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz, 0°C to +70°C	-0.15		+0.15		—	
	0 dBm, 1 kHz, -40°C to +85°C	-0.20		+0.20		4	
	0 dBm, 1 kHz, 0°C to +70°C	-1*	-0.1	+0.1		—	
	0 dBm, 1 kHz, -40°C to +85°C	-1	-0.15	+0.15		4	
Variation with frequency	300 Hz to 3400 Hz					—	
	Relative to 1 kHz					—	
	0°C to +70°C	-0.1		+0.1	—		
	-40°C to +85°C	-0.15		+0.15	4		
Gain tracking	+7 dBm to -55 dBm, ref 0 dBm				—		
	0°C to +70°C	-0.1		+0.1	—		
	-40°C to +85°C	-0.15		+0.15	4		

**Notes:**

\* P.G. = Performance Grade

-2 grade performance parameters are equivalent to -1 performance parameters except where indicated.

## ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
<b>Balance Return Signal (4- to 4-Wire; See Test Circuit B)</b>						
Gain accuracy	0 dBm, 1 kHz, 0°C to +70°C	-6.00	-5.85	-5.75	dB	3
	0 dBm, 1 kHz, -40°C to +85°C	-6.05	-5.85	-5.65		3, 4
	0 dBm, 1 kHz, 0°C to +70°C -1*	-5.95	-5.85	-5.75		3
	0 dBm, 1 kHz, -40°C to +85°C -1	-6.00	-5.85	-5.70		3, 4
Variation with frequency	300 Hz to 3400 Hz Relative to 1 kHz				dB	—
	0°C to +70°C -40°C to +85°C	-0.10 -0.15		+0.10 +0.15		3, 4 3, 4
Gain tracking	+7 dBm to -55 dBm, ref 0 dBm				dB	—
	0°C to +70°C -40°C to +85°C	-0.10 -0.15		+0.10 +0.15		— 4
Group delay	f = 1 kHz		5.3		μs	4, 15
<b>Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire, See Test Circuits A and B)</b>						
Total harmonic distortion	0 dBm, 300 Hz to 3.4 kHz +9 dBm, 300 Hz to 3.4 kHz		-64 -55	-50 -40	dB	4, 10
Total harmonic distortion with metering				-35		
<b>Idle Channel Noise</b>						
C-message weighted noise	2-wire, 0°C to +70°C		+7	+15	dBrnC	—
	2-wire, 0°C to +70°C -1*		+7	+12		—
	2-wire, -40°C to +85°C		+7	+15		4
	4-wire, 0°C to +70°C		+7	+15		—
Psophometric weighted noise	2-wire, 0°C to +70°C		-83	-75	dBmp	7
	2-wire, 0°C to +70°C -1*		-83	-78		—
	2-wire, -40°C to +85°C		-83	-75		4, 7
	4-wire, 0°C to +70°C		-83	-75		7
Psophometric idle channel noise with metering	4-wire, 0°C to +70°C -1*		-83	-78	dBmp	—
	4-wire, -40°C to +85°C		-83	-75		4, 7
	2-wire			-46		4, 11
	4-wire			-52		
<b>Signal Frequency Out-of-Band Noise (See Test Circuit E)</b>						
Metallic	4 kHz to 9 kHz			-76	dBm	4, 5, 9
	9 kHz to 1 MHz			-76		4, 5, 9
	256 kHz and harmonics			-57		4, 5
Longitudinal	1 kHz to 15 kHz			-70	dBm	4, 5, 9
	Above 15 kHz			-85		4, 5, 9
	256 kHz and harmonics			-57		4, 5
<b>DC Feed Currents (See Figure 1a, 1b, 1c) Battery = -48 V</b>						
Active state loop-current accuracy	I <sub>LOOP</sub> (nominal) = 40 mA	-7.5		+7.5	%	
OHT state	R <sub>L</sub> = 600 Ω	18	20	22	mA	
Tip Open state	R <sub>L</sub> = 600 Ω			1.0		
Open Circuit state	R <sub>L</sub> = 0 Ω			1.0		
Fault current limit, I <sub>L</sub> LIM (I <sub>AX</sub> + I <sub>BX</sub> )	A and B shorted to GND			130	mA	

## ELECTRICAL CHARACTERISTICS (continued)

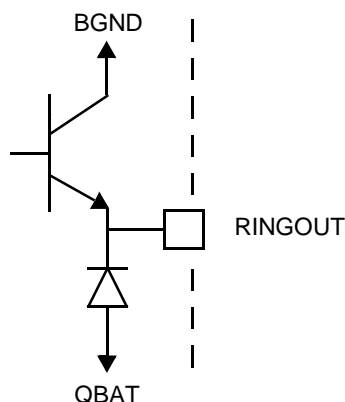
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
<b>Power Dissipation Battery = -48 V, Normal Polarity</b>						
On-hook Open Circuit state	-1*		35 35	120 80	mW	
On-hook OHT state	-1*		135 135	250 200		
On-hook Active state	-1*		200 200	400 300		
Off-hook OHT state	$R_L = 600 \Omega$		500	750		
Off-hook Active state	$R_L = 600 \Omega$		650	1000		
<b>Supply Currents</b>						
$V_{CC}$ on-hook supply current	Open Circuit state OHT state Active state		3.0 6.0 7.5	4.5 10.0 12.0	mA	
$V_{EE}$ on-hook supply current	Open Circuit state OHT state Active state		1.0 2.2 2.7	2.3 3.5 6.0		
$V_{BAT}$ on-hook supply current	Open Circuit state OHT state Active state		0.4 3.0 4.0	1.0 5.0 6.0		
<b>Power Supply Rejection Ratio (<math>V_{RIPPLE} = 50</math> mVrms)</b>						
$V_{CC}$	50 Hz to 3400 Hz	-1*	25 30	45 45	dB	6, 7
	3.4 kHz to 50 kHz	-1*	22 25	35 35		
$V_{EE}$	50 Hz to 3400 Hz	-1*	20 25	40 40		
	3.4 kHz to 50 kHz	-1*	10 10	25 25		
$V_{BAT}$	50 Hz to 3400 Hz		27 30	45 45		
	3.4 kHz to 50 kHz	-1*	20 25	40 40		
<b>Off-Hook Detector</b>						
Current threshold accuracy	$I_{DET} = 365/R_D$ Nominal	-20		+20	%	
<b>Ground-Key Detector Thresholds, Active state, Battery = -48 V (See Test Circuit F)</b>						
Ground-key resistance threshold	B(RING) to GND	2.0	5.0	10.0	k $\Omega$	
Ground-key current threshold	B(RING) to GND		9		mA	8
	Midpoint to GND		9			
<b>Ring-Trip Detector Input</b>						
Bias current		-5	-0.05		$\mu$ A	
Offset voltage	Source resistance 0 to 2 M $\Omega$	-50	0	+50	mV	12
<b>Logic Inputs (C4-C1, E0, E1, and CHCLK)</b>						
Input High voltage		2.0			V	
Input Low voltage				0.80		
Input High current	All inputs except E1	-75		40	$\mu$ A	
Input High current	Input E1	-75		45		
Input Low current		-0.40			mA	



## ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
<b>Logic Output (DET)</b>						
Output Low voltage	$I_{OUT} = 0.8 \text{ mA}$			0.40	V	
Output High voltage	$I_{OUT} = -0.1 \text{ mA}$	2.4				
<b>Relay Driver Outputs (RINGOUT)</b>						
On voltage	50 mA source	BGND -2	BGND -0.95		V	
Off leakage			0.5	100	$\mu\text{A}$	
Clamp voltage	50 mA sink	$Q_{BAT}$ -2			V	

## RELAY DRIVER SCHEMATIC



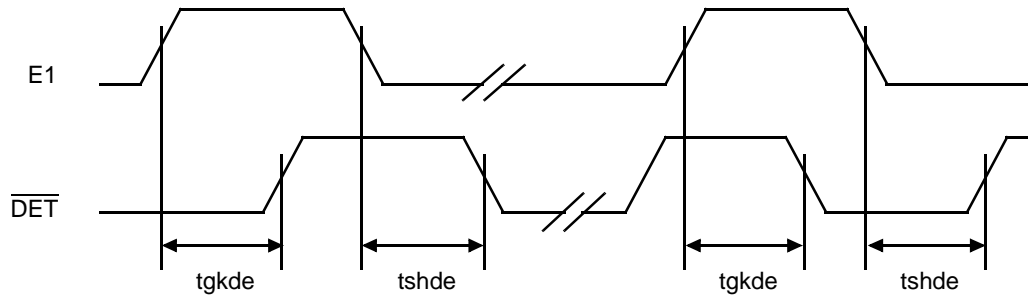
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## SWITCHING CHARACTERISTICS

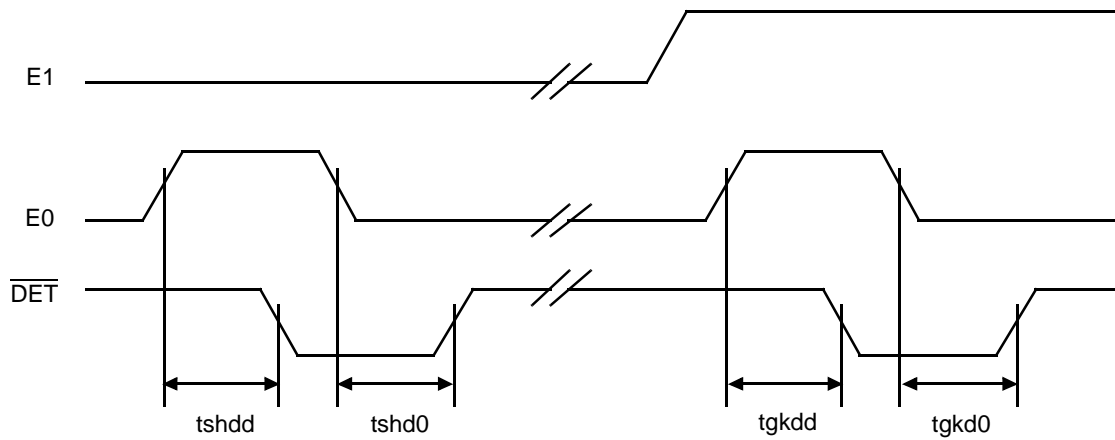
Symbol	Parameter	Test Conditions	Temperatures Ranges	Min	Typ	Max	Unit	Note	
tgkde	E1 Low to $\overline{\text{DET}}$ High (E0 = 1)	Ground-Key Detect state $R_L$ open, $R_G$ connected (See Figure H)	0°C to +70°C -40°C to +85°C			3.8 4.0	$\mu\text{s}$	4	
	E1 Low to $\overline{\text{DET}}$ Low (E0 = 1)		0°C to +70°C -40°C to +85°C		1.1 1.6				
tgkdd	E0 High to $\overline{\text{DET}}$ Low (E1 = 0)		0°C to +70°C -40°C to +85°C			1.1 1.6			
tgkd0	E0 Low to $\overline{\text{DET}}$ High (E1 = 0)		0°C to +70°C -40°C to +85°C			3.8 4.0			
tshde	E1 High to $\overline{\text{DET}}$ Low (E0 = 1)		Switchhook Detect state $R_L = 600 \Omega$ , $R_G$ open (See Figure G)	0°C to +70°C -40°C to +85°C					1.2 1.7
	E1 High to $\overline{\text{DET}}$ High (E0 = 1)			0°C to +70°C -40°C to +85°C		3.8 4.0			
tshdd	E0 High to $\overline{\text{DET}}$ Low (E1 = 1)	0°C to +70°C -40°C to +85°C				1.1 1.6			
tshd0	E0 Low to $\overline{\text{DET}}$ High (E1 = 1)	0°C to +70°C -40°C to +85°C				3.8 4.0			

SWITCHING WAVEFORMS

E1 to  $\overline{\text{DET}}$



E0 to  $\overline{\text{DET}}$

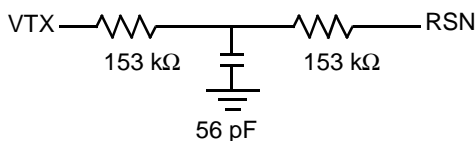


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**Note:**  
All delays measured at 1.4 V level.

**Notes:**

1. Unless otherwise noted, test conditions are  $BAT = -48\text{ V}$ ,  $V_{CC} = +5\text{ V}$ ,  $V_{EE} = -5\text{ V}$ ,  $R_L = 600\ \Omega$ ,  $C_{HP} = 0.22\ \mu\text{F}$ ,  $R_{DC1} = R_{DC2} = 31.25\ \text{k}\Omega$ ,  $C_{DC} = 0.1\ \mu\text{F}$ ,  $R_d = 51.1\ \text{k}\Omega$ , no fuse resistors, two-wire AC output impedance, programming impedance ( $Z_T$ ) =  $306\ \text{k}\Omega$  resistive, receive input summing impedance ( $Z_{RX}$ ) =  $300\ \text{k}\Omega$  resistive. (See Table 2 for component formulas.)
2. Overload level is defined when  $THD = 1\%$ .
3. Balance return signal is the signal generated at  $V_{TX}$  by  $V_{RX}$ . This specification assumes that the two-wire AC load impedance matches the impedance programmed by  $Z_T$ .
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. These tests are performed with a longitudinal impedance of  $90\ \Omega$  and metallic impedance of  $300\ \Omega$  for frequencies below  $12\ \text{kHz}$  and  $135\ \Omega$  for frequencies greater than  $12\ \text{kHz}$ . These tests are extremely sensitive to circuit board layout.
6. This parameter is tested at  $1\ \text{kHz}$  in production. Performance at other frequencies is guaranteed by characterization.
7. When the SLIC is in the Anti-sat 2 operating region, this parameter is degraded. The exact degradation depends on system design. The Anti-sat 2 region occurs at high loop resistances when  $|V_{BAT}| - |V_{AX} - V_{BX}|$  is less than approximately  $17\ \text{V}$ .
8. "Midpoint" is defined as the connection point between two  $300\ \Omega$  series resistors connected between A(TIP) and B(RING).
9. Fundamental and harmonics from  $256\ \text{kHz}$  switch-regulator chopper are not included.
10. Total harmonic distortion with metering as specified with a metering signal of  $2.2\ \text{V}_{rms}$  at the two-wire output, and a transmit signal of  $+3\ \text{dBm}$  or receive signal of  $-4\ \text{dBm}$ . The transmit or receive signals are single-frequency inputs, and the distortion is measured as the highest in-band harmonic at the two-wire or the four-wire output relative to the input signal.
11. Noise with metering is measured by applying a  $2.2\ \text{V}_{rms}$  metering signal (measured at the two-wire output) and measuring the psophometric noise at the two-wire and four-wire outputs over a  $200\ \text{ms}$  time interval.
12. Tested with  $0\ \Omega$  source impedance.  $2\ \text{M}\Omega$  is specified for system design purposes only.
13. Assumes the following  $Z_T$  network:



14. Group delay can be considerably reduced by using a  $Z_T$  network such as that shown in Note 13 above. The network reduces the group delay to less than  $2\ \mu\text{s}$ . The effect of group delay on linecard performance may be compensated for by using the QSLAC™ or DSLAC™ devices.

**Table 1. SLIC Decoding**

State	C3 C2 C1	Two-Wire Status	DET Output	
			E0 = 1* E1 = 0	E0 = 1* E1 = 1
0	0 0 0	Open Circuit	Ring trip	Ring trip
1	0 0 1	Ringing	Ring trip	Ring trip
2	0 1 0	Active	Loop detector	Ground key
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key
4	1 0 0	Tip Open	Loop detector	—
5	1 0 1	Reserved	Loop detector	—
6	1 1 0	Active Polarity Reversal	Loop detector	Ground key
7	1 1 1	OHT Polarity Reversal	Loop detector	Ground key

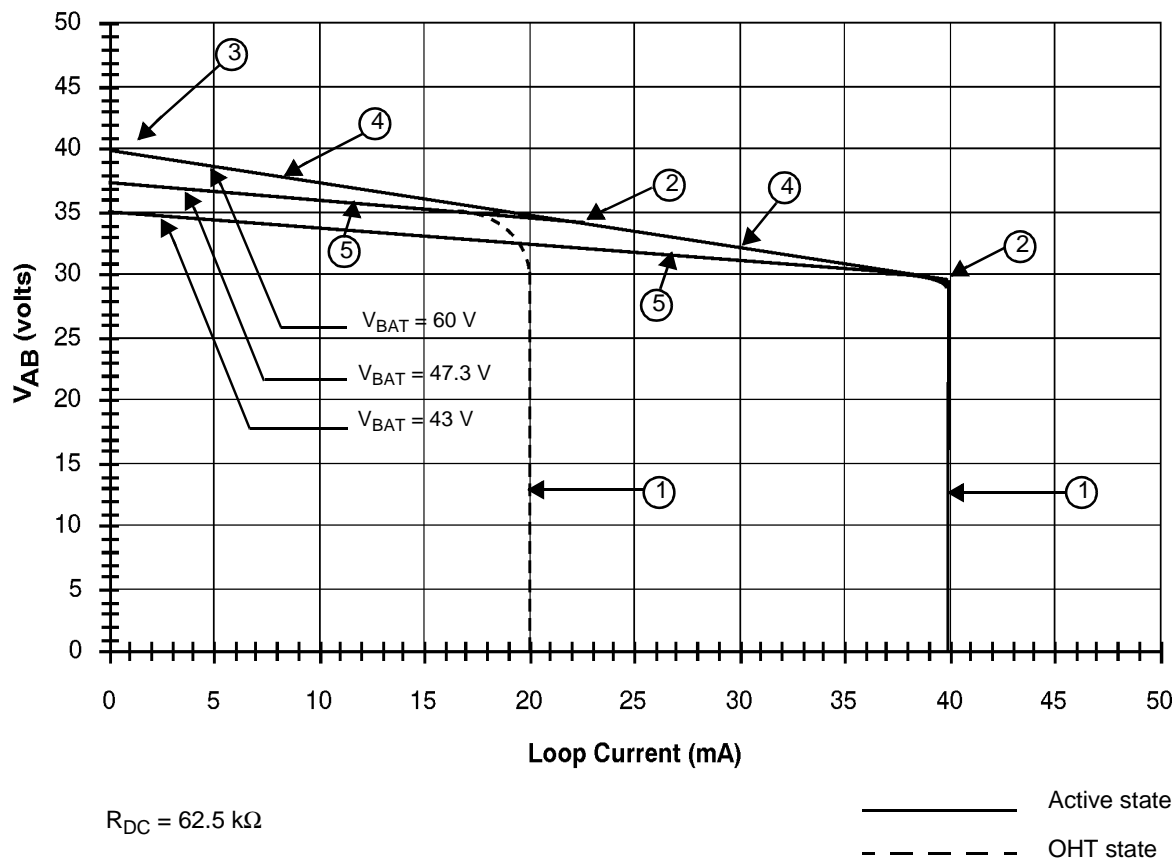
**Note:**

\* A logic Low on E0 disables the  $\overline{DET}$  output into the open-collector state.

**Table 2. User-Programmable Components**

$Z_T = 510(Z_{2WIN} - 2R_F)$	<p><math>Z_T</math> is connected between the VTX and RSN pins. The fuse resistors are <math>R_F</math>, and <math>Z_{2WIN}</math> is the desired 2-wire AC input impedance. When computing <math>Z_T</math>, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.</p>
$Z_{RX} = \frac{Z_L}{G_{42L}} \cdot \frac{1000 \cdot Z_T}{Z_T + 510(Z_L + 2R_F)}$	<p><math>Z_{RX}</math> is connected from <math>V_{RX}</math> to the RSN pin, <math>Z_T</math> is defined above, and <math>G_{42L}</math> is the desired receive gain.</p>
$R_{DC1} + R_{DC2} = \frac{2500}{I_{FEED}}$ $C_{DC} = 1.5 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1} \cdot R_{DC2}}$	<p><math>R_{DC1}</math>, <math>R_{DC2}</math>, and <math>C_{DC}</math> form the network connected to the RDC pin. <math>R_{DC1}</math> and <math>R_{DC2}</math> are approximately equal.</p>
$R_D = \frac{365}{I_T}, \quad C_D = \frac{0.5 \text{ ms}}{R_D}$	<p><math>R_D</math> and <math>C_D</math> form the network connected from RD to <math>-5</math> V and <math>I_T</math> is the threshold current between on hook and off hook.</p>
$Z_M = \frac{V_{MG}}{V_{M2W}} \cdot \frac{K_1(\omega) \cdot Z_L \cdot Z_T}{Z_T + 0.51 \cdot K_1(\omega)(2R_F + Z_L)}$	<p><math>Z_M</math> is connected from <math>V_{MG}</math> (metering source) to the RSN pin, <math>V_{M2W}</math> is the desired magnitude of the metering signal at the 2-wire output (usually 2.2 Vrms) and <math>K_1(\omega)</math> is defined below.</p> $K_1(\omega) = \frac{1000}{1 + j\omega(11.5 \cdot 10^{-9} + CX/2)(36 + Z_L + 2R_F)}$ <p>where: CX = The values of the identical capacitors from A and B to GND  <math>\omega = 2\pi \cdot</math> metering frequency</p>

## DC FEED CHARACTERISTICS



### Notes:

1. Constant-current region:

$$\text{Active state, } I_L = \frac{2500}{R_{DC}}$$

$$\text{OHT state, } I_L = \frac{1}{2} \frac{2500}{R_{DC}}$$

2. Anti-sat turn-on;

$$V_{AB} = 1.02 |V_{BAT}| - 14, \quad |V_{BAT}| < 43.1\text{ V (Anti-sat -2)}$$

$$V_{AB} = 29.95\text{ V}, \quad |V_{BAT}| \geq 43.1\text{ V (Anti-sat -1)}$$

3. Open Circuit voltage;

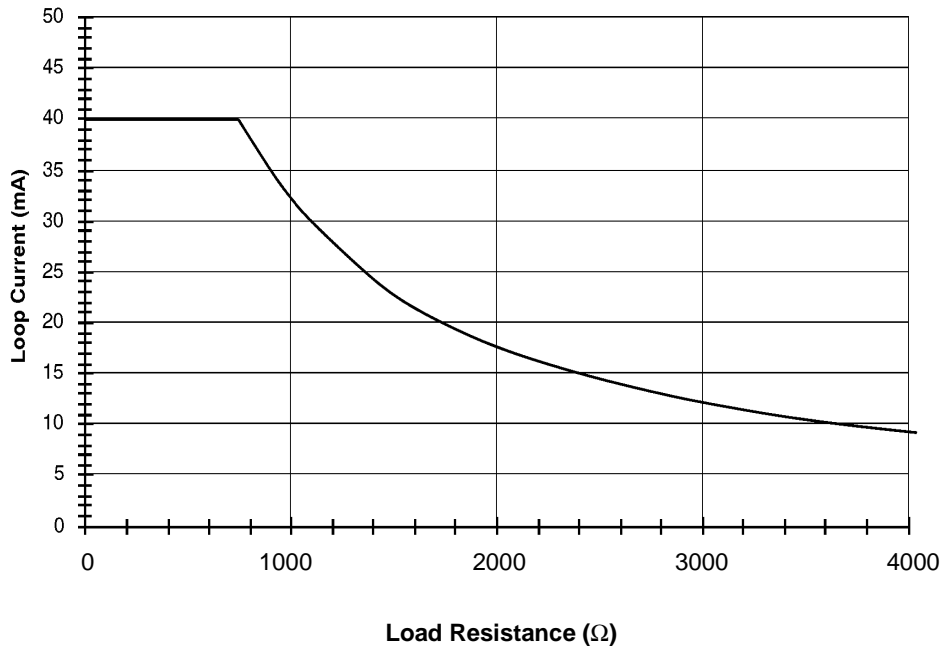
$$V_{AB} = 0.55 |V_{BAT}| + 11.4, \quad |V_{BAT}| \leq 53\text{ V (Anti-sat -2)}$$

$$V_{AB} = 40\text{ V}, \quad |V_{BAT}| > 53\text{ V (Anti-sat -1)}$$

4. Anti-sat -1 region

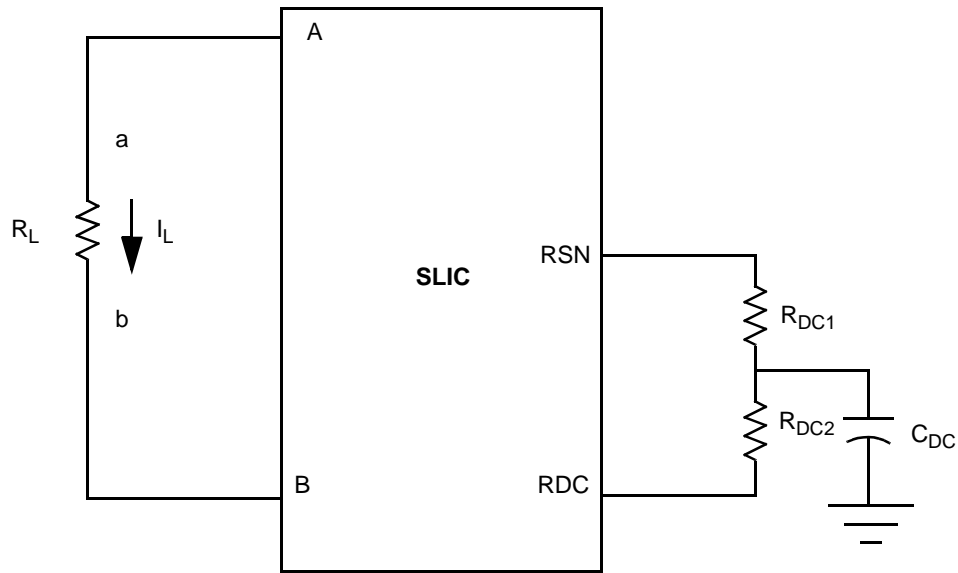
5. Anti-sat -2 region

a.  $V_A - V_B$  ( $V_{AB}$ ) Voltage vs. Loop Current (Typical)



$R_{DC} = 62.5 \text{ k}\Omega$   
 $V_{BAT} = 47.3 \text{ V}$

**b. Loop Current vs. Load Resistance (Typical)**



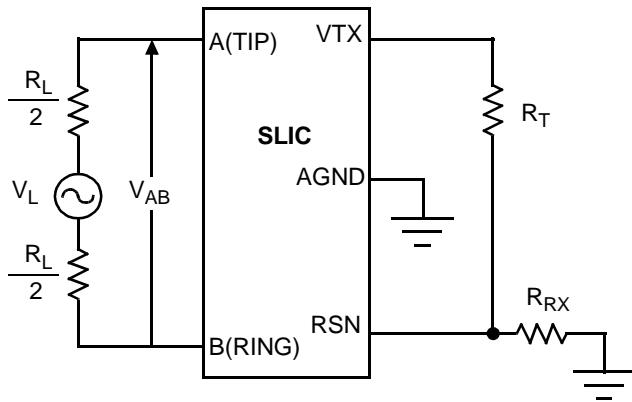
Current programmed by  $R_{DC1}$  and  $R_{DC}$

**c. Feed Programming**

16856B-004

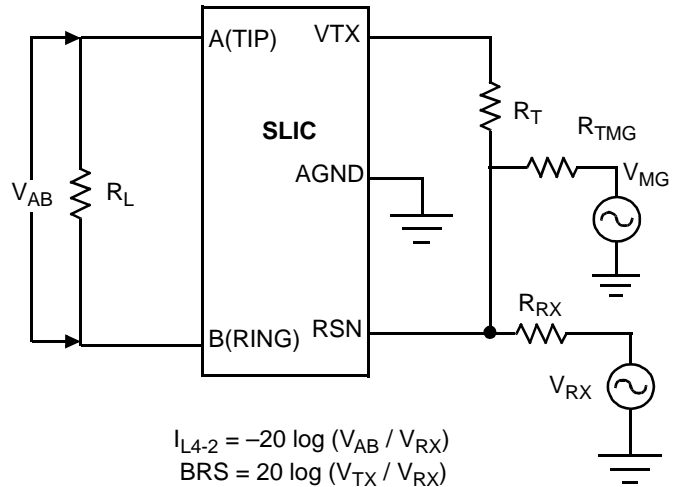
**Figure 1. DC Feed Characteristics**

TEST CIRCUITS



$$I_{L2-4} = -20 \log (V_{TX} / V_{AB})$$

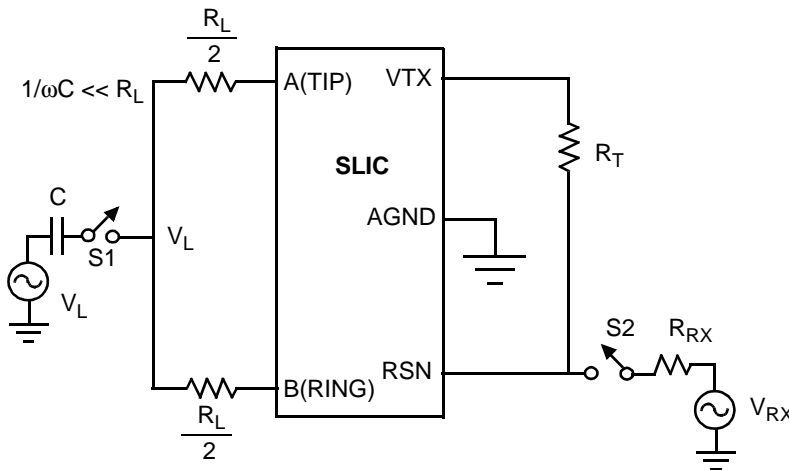
A. Two- to Four-Wire Insertion Loss



$$I_{L4-2} = -20 \log (V_{AB} / V_{RX})$$

$$BRS = 20 \log (V_{TX} / V_{RX})$$

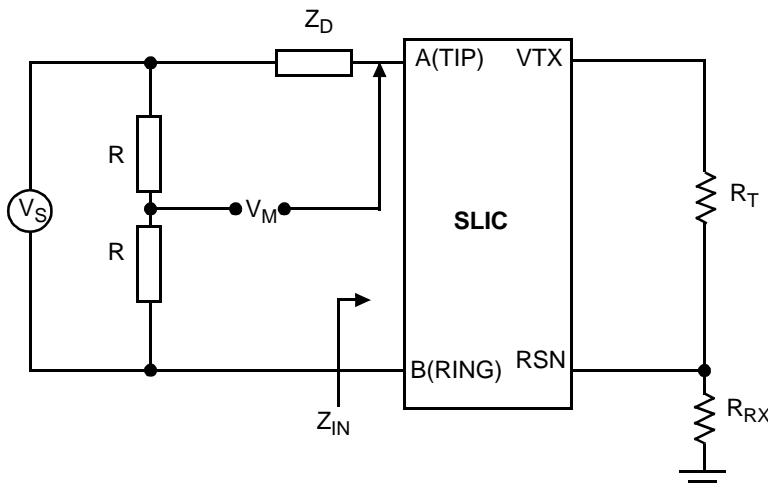
B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S1 Closed, S2 Open  
 L-T Long. Bal. =  $-20 \log (V_{AB} / V_L)$   
 L-4 Long. Bal. =  $-20 \log (V_{TX} / G_{TX} \cdot V_L)$

S2 Closed, S1 Open  
 4-L Long. Sig. Gen. =  $-20 \log (V_L / V_{RX})$

C. Longitudinal Balance

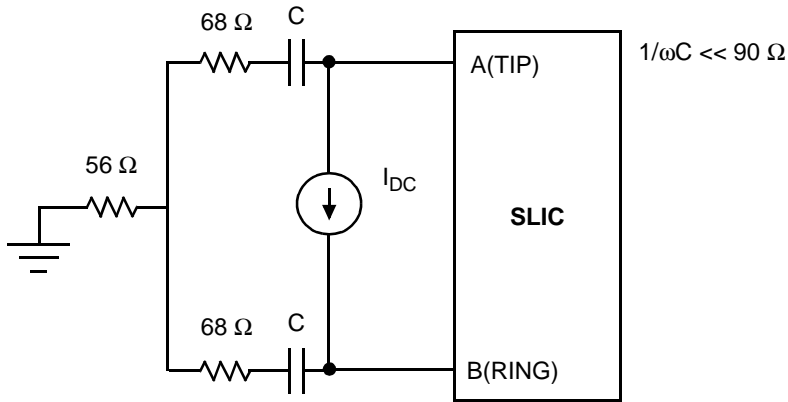


**Note:**  
 $Z_D$  is the desired impedance (e.g., the characteristic impedance of the line.)

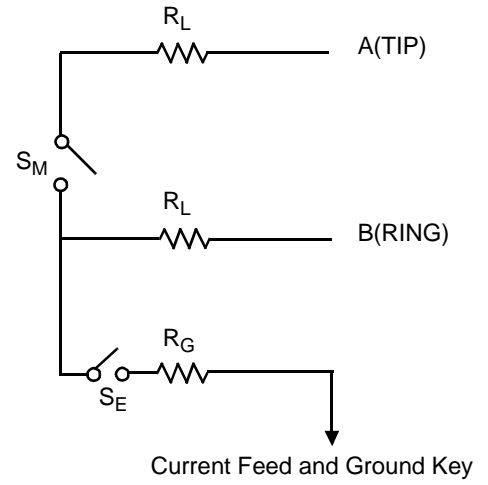
$$R_L = 20 \log (2 V_M / V_S)$$

D. Two-Wire Return Loss Test Circuit

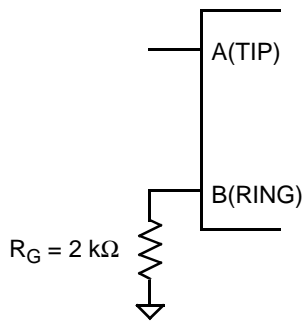
TESTS CIRCUITS (continued)



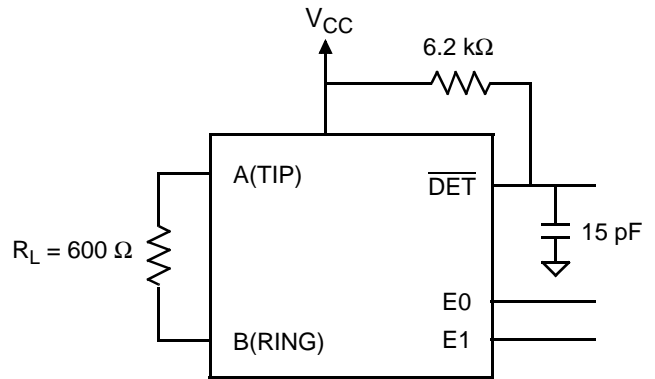
E. Single-Frequency Noise



F. Ground-Key Detection



G. Ground-Key Switching

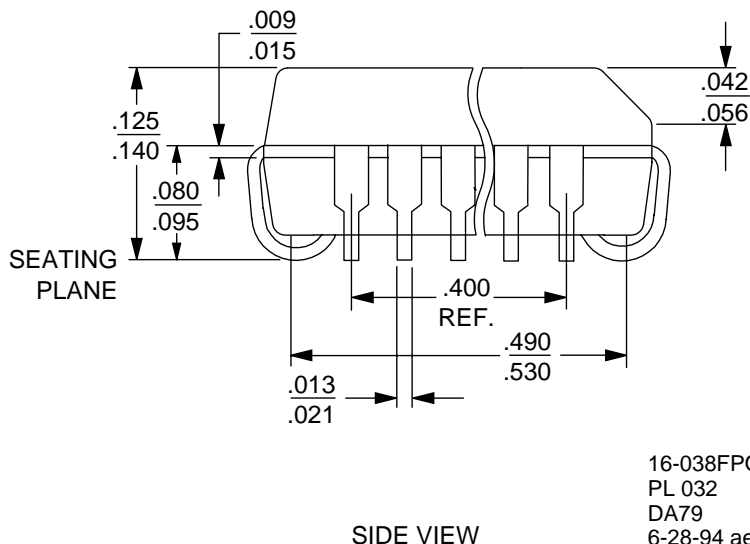
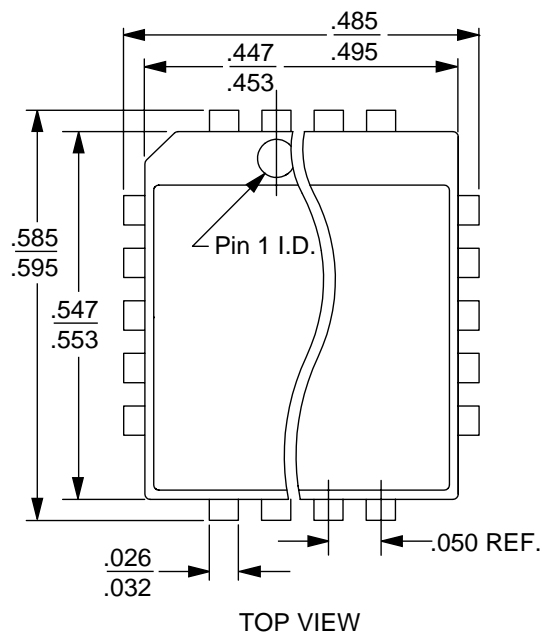


H. Loop-Detector Switching



## PHYSICAL DIMENSION

### PL032



16-038FPO-5  
PL 032  
DA79  
6-28-94 ae

## REVISION SUMMARY

### Revision B to C

- Minor changes were made to the data sheet style and format to conform to AMD standards.

### Revision C to D

- In the Pin Description table, inserted/changed TP pin description to: "Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation."
- Minor changes were made to the data sheet style and format to conform to AMD standards.

### Revision D to E

- The physical dimension (PL032) was added to the Physical Dimension section.
- Deleted the Ceramic DIP and Plastic DIP part (Am79M531) and references to it.
- Updated the Pin Description table to correct inconsistencies.

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