Product Brief
EDDC
SDA 9380

Potential Application

The SDA 9380 is a new component of the Infineon MEGAVISION® IC set to support single chip back end solutions for SDTV up to HDTV CRT's

EDDC

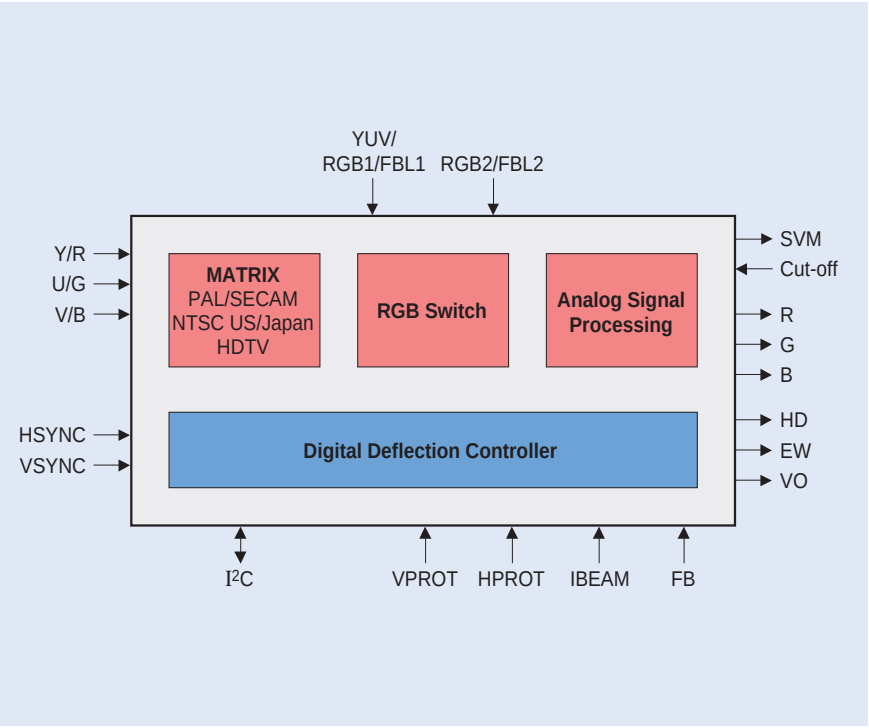
Features Deflection Controller

- PLL on chip - no external clock required
- I^2C-Bus alignment for all deflection parameters
- Line frequencies / standards
  PAL 50 Hz p, 100 Hz i - 31.2 kHz
  NTSC 60 Hz p, 120 Hz i - 31.5 kHz
  HDTV ATSC - 32.4 kHz
  HDTV MUSE - 33.7 kHz
  SVGA - 38 kHz
- Automatic switching between 31, 35 and 38 kHz in monitor mode
- Picture width and picture height EHT compensation
- Upper/lower EW corner correction separately adjustable
- V-angle and V-bow correction
- Vertical zoom/shrink and scroll function
- No re-adjustment of E/W after changing vertical S-correction and linearity
- H- and V-blanking time adjustable
- Auto adaption of V-frequency in the range of 192 and 680 lines per field
- Selectable black switch off modes
- Selectable softstart of the H-output stage
- Protection against EHT run away (X-rays protection)
- Protection against missing V-deflection (CRT-protection)
- H-frequent PWM output signal for generating an adjustable vertical frequent parabola or a constant pulse width
- DAC output with 8-Bit resolution for general purpose
- Digital output for general purpose

Features YUV/RGB

- Two YUV/RGB inputs and one RGB input with fast blanking capability
- Switchable color difference matrix for PAL/SECAM, NTSC (U.S. and Japan) and HDTV
- Common saturation, brightness and contrast control for all input channels
- Cut off and white level control loop
- Black stretching of non-standard input signal
- Selectable blue stretch function
- Peak drive limiter with soft clipping
- Average beam current limiter
- Luminance output signal SVM for scan velocity modulation, adjustable delay from SVM to the RGB outputs

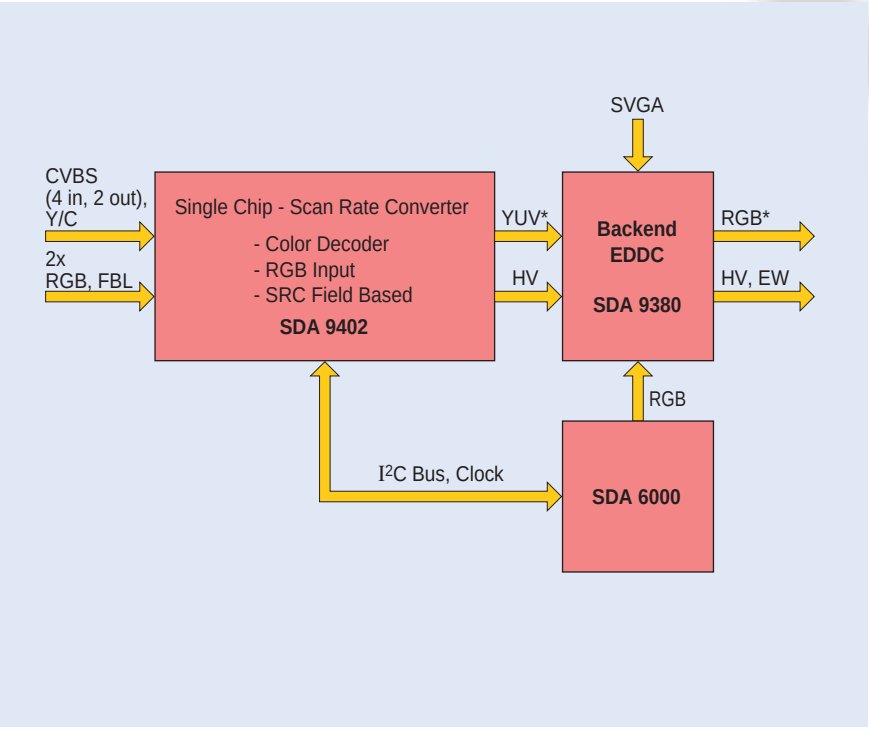
SDA 9380
Block Diagram



Technical Data

- I²C-Bus control
- P-MQFP-64 package
- 3.3 V and 8 V supply voltages

Application Example



How to reach us:
http://www.infineon.com

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Bereich Kommunikation,
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D-81541 München

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