IR Remote Control Transmitter with IR Diode Driver — SDA 2208-3

Preliminary Data — **Bipolar IC**

The SDA 2208-3 is designed as a remote control transmitter for direct driving of infrared transmitter diodes. The instructions are generated by an input matrix (i. e. keyboard) in the form of biphase codes. Distributed over 8 levels, there are a max. of 512 instructions available. The newly designed SDA 2208-3 is feature compatible with the pins and functions of the SDA 2208-2. The SDA 2208-3 is much better protected against electrostatic discharges (ESD).

Type	Ordering Code	Package
SDA 2208-3	Q67000-A8235	P-DIP-20

Circuit Description

Voltage Supply

Voltage consumption ceases in the quiescent state and is activated subsequent to connecting the component's matrix. When the matrix is disconnected, the IC automatically completes the telegram and returns into the quiescent state.

Clock Input

The clock input is equipped with a ceramic resonator. This resonator oscillates with its parallel resonance. In addition, the clock signal can be injected at pin CLK I. The oscillator can be also operated by using an LC circuit with an isolating capacitor.

Input Matrix

The matrix is comprised of 8 rows and 8 columns. Column A is used as supply voltage V_S. In order to transmit a telegram, the respective rows and columns have to be connected. The transmitter is switched on and a telegram is output. The length of the telegram depends on the duration of the matrix connection. A telegram is comprised of a start command, a variable number of information commands (depending on the duration of the matrix connection).

Programming via PPIN

The programming pin is used to provide access to all command sets or 512 commands since the 8 × 8 matrix limits the use to one command set or 64 different commands. By subdividing the command sets into 8 levels of 64 commands each, a specific level can be selected by either keeping the PPIN open or by combining it with one of the seven column inputs (CPB to CPH). When connecting PPIN with one column alone, the standby supply current I_S does not increase.

Safety Features against Incorrect Operation

As a prerequisite for an error-free telegram output with at least one information command, the matrix connection has to be free of interferences and its clock-frequency-dependent, minimal duration should be approx. 60 ms at a clock frequency of 500 kHz. The applied integrated circuit is equipped with a preventive mechanism (key bouncing) against erroneous outputs, which automatically resets the circuit during each detected interference. Equally, operating errors caused by connecting more than one row and one column are detected. The telegram will be ended through continuous transmitting of end. Operating errors can be cancelled only by disconnecting all matrix connections. The level selection key (PPIN function) will be effective only if it is depressed prior to or simultaneously with the matrix key. Also, a simultaneous depressing of several selection keys has the same effect on the telegram as an erroneous matrix operation.

Composition of a Telegram

Subsequent to switch-on, the command No. 511 (10-bit word length) is output as start command to indicate to the receiver the onset of transmission. Depending on the duration of the matrix connection, a series of identical commands will follow. If a telegram is ended by disconnecting the matrix connection, not more than one additional information command will be issued to be followed immediately by the end command. This end command is identical with the start command.

Command Structure

Each command consists of a presignal, an infrared pause, a start bit and 9 information bits. During the duration of the presignal ($256/f_{CLK}$), the receiver performs a simple amplitude adjustment of the input amplifier.

The infrared pause appears between the end of the presignal and the onset of the start bit. Again, the receiver is provided with enough time to recognize transmission distortions based on the limits of the transmission range.

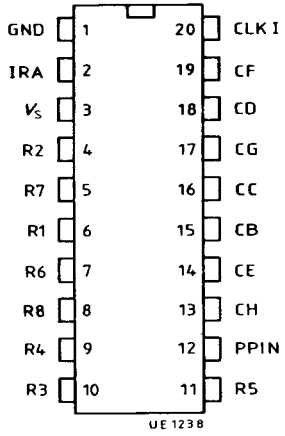
The start bit has been permanently programmed as "1" and is used as synchronization support for the receiver.

The bit structure has been **illustrated in the pulse diagram.**

Output Driver Stage

The fully integrated driver stage enables the direct connection of the infrared transmitter diodes to the infrared output IRA. The diode current is maintained at a constant level within a defined range to stabilize the transmitting power of the infrared diodes.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	GND	Ground
2	IRA	Output IRA
3	V_S	Supply voltage
4	R2	Matrix connection rows
5	R7	
6	R1	
7	R6	
8	R8	
9	R4	
10	R3	
11	R5	
12	PPIN	Programming Pin
13	CH	Matrix connection column
14	CE	
15	CB	
16	CC	
17	CG	
18	CD	
19	CF	
20	CLKI	Oscillator input

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values	Unit
Supply voltage range	V_S	– 0.3 to 10.5	V
Matrix rows	V_{row}	– 0.3 to V_S	V
Matrix columns	V_{col}	– 0.3 to V_S	V
Programming pin (PPIN)	V_{pp}	– 0.3 to V_S	V
Oscillator input (CLKI)	$V_{I\,OSC}$	– 0.3 to 2	V
Infrared output (IRA) inhibited in operation	 V_Q V_Q	 – 0.3 to 10.5 – 0.3 to 8	 V V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	60	K/W

Operating Range

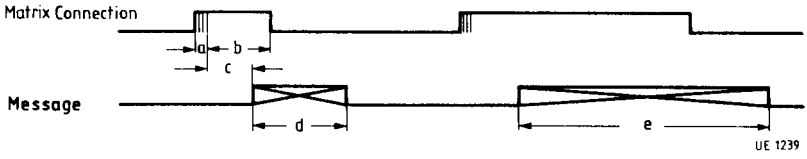
Supply voltage	V_S	4 to 10	V
Ambient temperature	T_A	0 to 70	°C
Oscillator frequency	f_{CLK}	430 to 530	kHz

Characteristics
V_S = 5.5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption transmitting phase standby operation	 I_S I_S		 19 < 1	 10	 mA µA
Output current IRA 2 V < V_2 < 6 V	I_2	500	900	1000	mA
Connecting resistance (row-column or column-PPIN)	$R_{row\,col}$			500	Ω

Pulse Diagrams

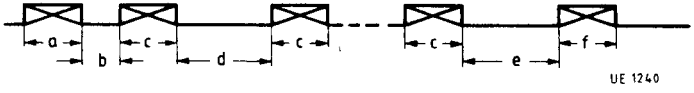
Basic Operating Sequence



for 500 kHz
b = 60.928 ms
c = 26.624 ms
d = 177.664

a) bounce
b) minimum key operating time to complete telegram with one information instruction
c) delay between the on-set of error-free matrix connection and on-set of telegram
d) telegram with one information command
e) telegram with several identical information commands

Composition of Telegram



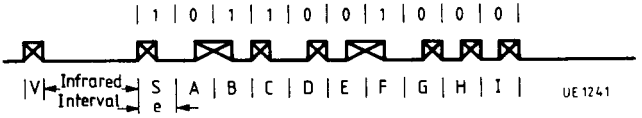
for 500 kHz
a = c = f = 13.312 ms
b = 19.968 ms
d = e = 177.76 ms

a) start command 10 bits
b) time interval between start and information command
c) information command 10 bits
d) time interval between identical information commands
e) time interval between information and end command
f) end command 10 bits

The timespan of an error-free matrix connection determines the number of identical information commands.

Pulse Diagrams

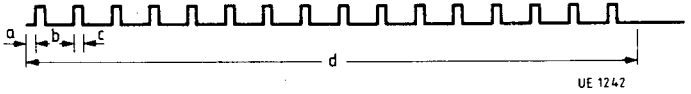
Command Structure in Biphase Code



Time duration single bit e: $512/f_{CLK}$
presignal V: $256/f_{CLK}$
infrared pause: $5 \times 256/f_{CLK}$

start bit S is always 1
bits A to I are addressable

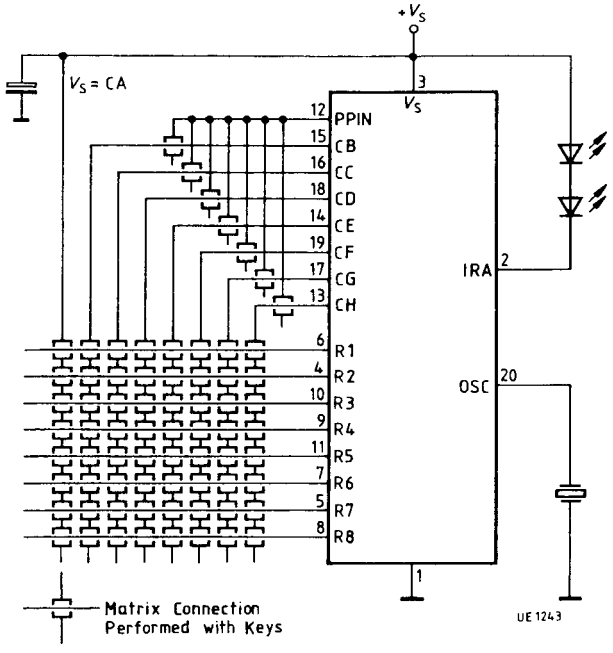
Structure of the Modulated Half Bit (as well as the presignal)



$a = c = 4/f_{CLK}$
$b = 16/f_{CLK}$
$d = 256/f_{CLK}$
16 pulses per half bit

The H signal indicates a constant current source at Q_{IRA}. The infrared transmitter diode is then active.

Block Diagram



Since the infrared transmitter diodes have to be driven with pulse currents of approx. 1 A, the following has to be complied with during the layout of the PC board:

1) The smoothing capacitor between V_S and ground should be located as closely as possible to the pins of the IC.
2) The supply line to the transmitter diodes is not to cause cross-talk in the key matrix.
3) No residual currents are to flow over the connection ceramic oscillator/ground pin.

Truth Table

No. of the instruction	Matrix connection row-column	Binary code IRA information instruction A	B	C	D	E	F	G	H	I
0	1A	0	0	0	0	0	0	0	0	0
1	1B	1	0	0	0	0	0	0	0	0
2	1C	0	1	0	0	0	0	0	0	0
3	1D	1	1	0	0	0	0	0	0	0
4	1E	0	0	1	0	0	0	0	0	0
5	1F	1	0	1	0	0	0	0	0	0
6	1G	0	1	1	0	0	0	0	0	0
7	1H	1	1	1	0	0	0	0	0	0
8	2A	0	0	0	1	0	0	0	0	0
9	2B	1	0	0	1	0	0	0	0	0
10	2C	0	1	0	1	0	0	0	0	0
11	2D	1	1	0	1	0	0	0	0	0
12	2E	0	0	1	1	0	0	0	0	0
13	2F	1	0	1	1	0	0	0	0	0
14	2G	0	1	1	1	0	0	0	0	0
15	2H	1	1	1	1	0	0	0	0	0
16	3A	0	0	0	0	1	0	0	0	0
17	3B	1	0	0	0	1	0	0	0	0
18	3C	0	1	0	0	1	0	0	0	0
19	3D	1	1	0	0	1	0	0	0	0
20	3E	0	0	1	0	1	0	0	0	0
21	3F	1	0	1	0	1	0	0	0	0
22	3G	0	1	1	0	1	0	0	0	0
23	3H	1	1	1	0	1	0	0	0	0
24	4A	0	0	0	1	1	0	0	0	0
25	4B	1	0	0	1	1	0	0	0	0
26	4C	0	1	0	1	1	0	0	0	0
27	4D	1	1	0	1	1	0	0	0	0
28	4E	0	0	1	1	1	0	0	0	0
29	4F	1	0	1	1	1	0	0	0	0
30	4G	0	1	1	1	1	0	0	0	0
31	4H	1	1	1	1	1	0	0	0	0
32	5A	0	0	0	0	0	1	0	0	0
33	5B	1	0	0	0	0	1	0	0	0
34	5C	0	1	0	0	0	1	0	0	0
35	5D	1	1	0	0	0	1	0	0	0
36	5E	0	0	1	0	0	1	0	0	0
37	5F	1	0	1	0	0	1	0	0	0
38	5G	0	1	1	0	0	1	0	0	0
39	5H	1	1	1	0	0	1	0	0	0
40	6A	0	0	0	1	0	1	0	0	0

Truth Table (cont'd)

No. of the instruction	Matrix connection row-column	Binary code IRA information instruction A	B	C	D	E	F	G	H	I
41	6B	1	0	0	1	0	1	0	0	0
42	6C	0	1	0	1	0	1	0	0	0
43	6D	1	1	0	1	0	1	0	0	0
44	6E	0	0	1	1	0	1	0	0	0
45	6F	1	0	1	1	0	1	0	0	0
46	6G	0	1	1	1	0	1	0	0	0
47	6H	1	1	1	1	0	1	0	0	0
48	7A	0	0	0	0	1	1	0	0	0
49	7B	1	0	0	0	1	1	0	0	0
50	7C	0	1	0	0	1	1	0	0	0
51	7D	1	1	0	0	1	1	0	0	0
52	7E	0	0	1	0	1	1	0	0	0
53	7F	1	0	1	0	1	1	0	0	0
54	7G	0	1	1	0	1	1	0	0	0
55	7H	1	1	1	0	1	1	0	0	0
56	8A	0	0	0	1	1	1	0	0	0
57	8B	1	0	0	1	1	1	0	0	0
58	8C	0	1	0	1	1	1	0	0	0
59	8D	1	1	0	1	1	1	0	0	0
60	8E	0	0	1	1	1	1	0	0	0
61	8F	1	0	1	1	1	1	0	0	0
62	8G	0	1	1	1	1	1	0	0	0
63	8H	1	1	1	1	1	1	0	0	0

	G	H	I
Command 0 to 63: PPIN free	0	0	0
Command 64 to 127: PPIN connected with CB	1	0	0
Command 128 to 191: PPIN connected with CC	0	1	0
Command 192 to 255: PPIN connected with CD	1	1	0
Command 256 to 319: PPIN connected with CE	0	0	1
Command 320 to 383: PPIN connected with CF	1	0	1
Command 384 to 447: PPIN connected with CG	0	1	1
Command 448 to 511: PPIN connected with CH	1	1	1

In every command set, the assignment instruction – matrix connection (row – column) is analogous to the group 0 to 63.

Example:

Command 64 is generated, when PPIN is connected with CB, and R1 with CA.