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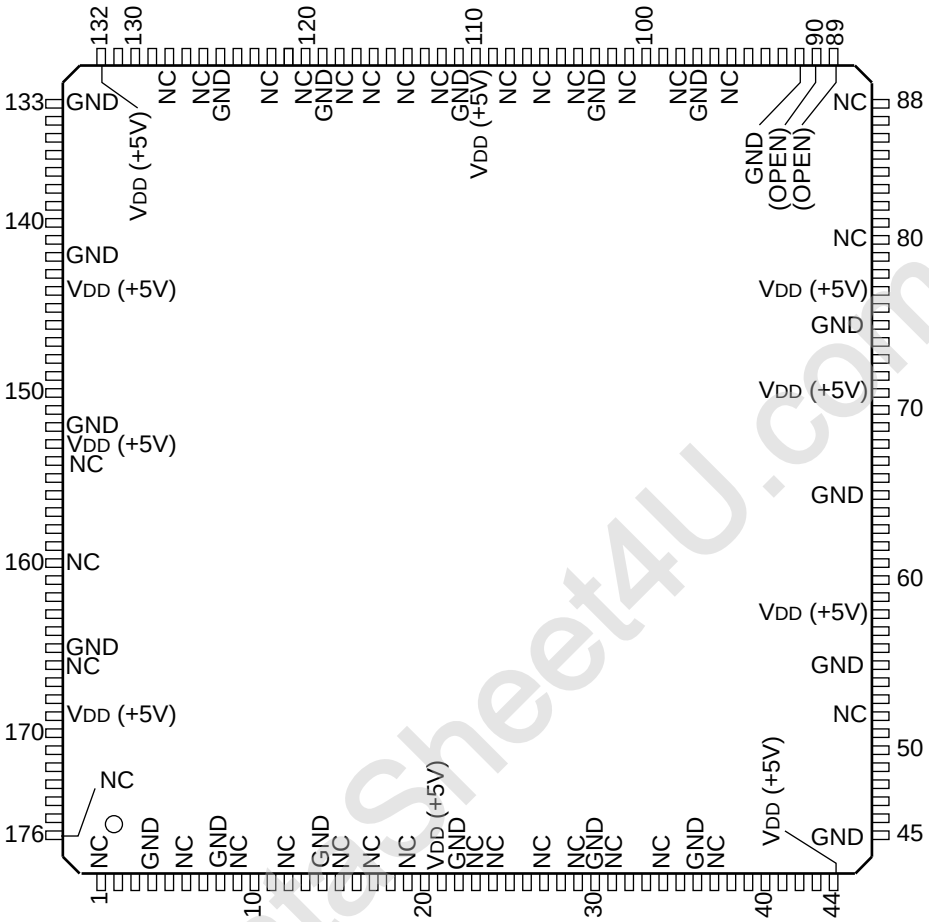
IL16

C-MOS SCSI2 PROTOCOL-CONTROLLER

-TOP VIEW



V_{DD}=(+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1		NC	45		Vss	89		OPEN	133		Vss
2	O	DBOE6	46	O	DBOE15	90		OPEN	134	I	A0
3	O	DBOE5	47	O	DBOE14	91		Vss	135	I	A1
4		Vss	48	O	DBOE13	92	O	DBOE8	136	I	A2
5	O	DBOE4	49	I	$\overline{S}$/DSEL	93	O	INIT	137	I	A3
6		NC	50	I	$\overline{IORD}$ (DMR/$\overline{W}$)	94	O	TARG	138	I	A4
7	I/O	$\overline{LDBP}$	51	I	$\overline{IOWR}$ ($\overline{DMLDS}$)	95		NC	139	I	$\overline{CS0}$
8		Vss	52		NC	96	I	TEST2	140	I	$\overline{CS1}$
9		NC	53	I	DMA0	97		Vss	141	I/O	LDP
10	I/O	$\overline{DB7}$	54	I/O	LDMDP	98		NC	142		Vss
11	I/O	$\overline{DB6}$	55		Vss	99	I/O	$\overline{DB11}$	143	I/O	D0
12		NC	56	I/O	DMD0	100	I/O	$\overline{DB10}$	144		V_{DD}
13	I/O	$\overline{DB5}$	57	I/O	DMD1	101		NC	145	I/O	D1
14		Vss	58		V_{DD}	102	I/O	$\overline{DB9}$	146	I/O	D2
15		NC	59	I/O	DMD2	103		Vss	147	I/O	D3
16	I/O	$\overline{DB4}$	60	I/O	DMD3	104		NC	148	I/O	D4
17		NC	61	I/O	DMD4	105	I/O	$\overline{DB8}$	149	I/O	D5
18	I/O	$\overline{DB3}$	62	I/O	DMD5	106		NC	150	I/O	D6
19		NC	63	I/O	DMD6	107	I/O	$\overline{I/O}$	151	I/O	D7
20	I/O	$\overline{DB2}$	64	I/O	DMD7	108		NC	152		Vss
21		V_{DD}	65		Vss	109	I/O	$\overline{REQ}$	153		V_{DD}
22		Vss	66	I/O	DMD8	110		V_{DD}	154		NC
23		NC	67	I/O	DMD9	111		Vss	155	I/O	D8
24		NC	68	I/O	DMD10	112		NC	156	I/O	D9
25	I/O	$\overline{DB1}$	69	I/O	DMD11	113	I/O	$\overline{C/D}$	157	I/O	D10
26	I/O	$\overline{DB0}$	70	I/O	DMD12	114		NC	158	I/O	D11
27		NC	71		V_{DD}	115	I/O	$\overline{SEL}$	159	I/O	D12
28	I/O	$\overline{UDBP}$	72	I/O	DMD13	116		NC	160		NC
29		NC	73	I/O	DMD14	117	I/O	$\overline{MSG}$	161	I/O	D13
30		Vss	74	I/O	DMD15	118		NC	162	I/O	D14
31		NC	75		Vss	119		Vss	163	I/O	D15
32	I/O	$\overline{DB15}$	76	I/O	UDMDP	120		NC	164	I/O	UDP
33	I/O	$\overline{DB14}$	77		V_{DD}	121	I/O	$\overline{RST}$	165		Vss
34		NC	78	I	CLK	122		NC	166		NC
35	I/O	$\overline{DB13}$	79	I	$\overline{DMBHE}$ ($\overline{DMUDS}$)	123	I/O	$\overline{ACK}$	167	I	$\overline{BHE}$
36		Vss	80		NC	124	I/O	$\overline{BSY}$	168	I	$\overline{WR}$ ($\overline{LDS}$)
37		NC	81	I	$\overline{DACK}$	125		Vss	169		V_{DD}
38	I/O	$\overline{DB12}$	82	O	DREQ	126		NC	170	I	$\overline{RD}$ (R/$\overline{W}$)
39	O	DBOE3	83	I	TP	127	I/O	$\overline{ATN}$	171	O	INT ($\overline{INT}$)
40	O	DBOE2	84	O	DBOE12	128		NC	172	I	MODE
41	O	DBOE1	85	O	DBOE11	129	O	SELOE	173	I/O	$\overline{RESET}$
42	O	DBOE0	86	O	DBOE10	130	O	RSTOE	174	O	LDBOEP
43	O	UDBOEP	87	O	DBOE9	131	O	BSYOE	175	O	DBOE7
44		V_{DD}	88		NC	132		V_{DD}	176		NC

INPUT

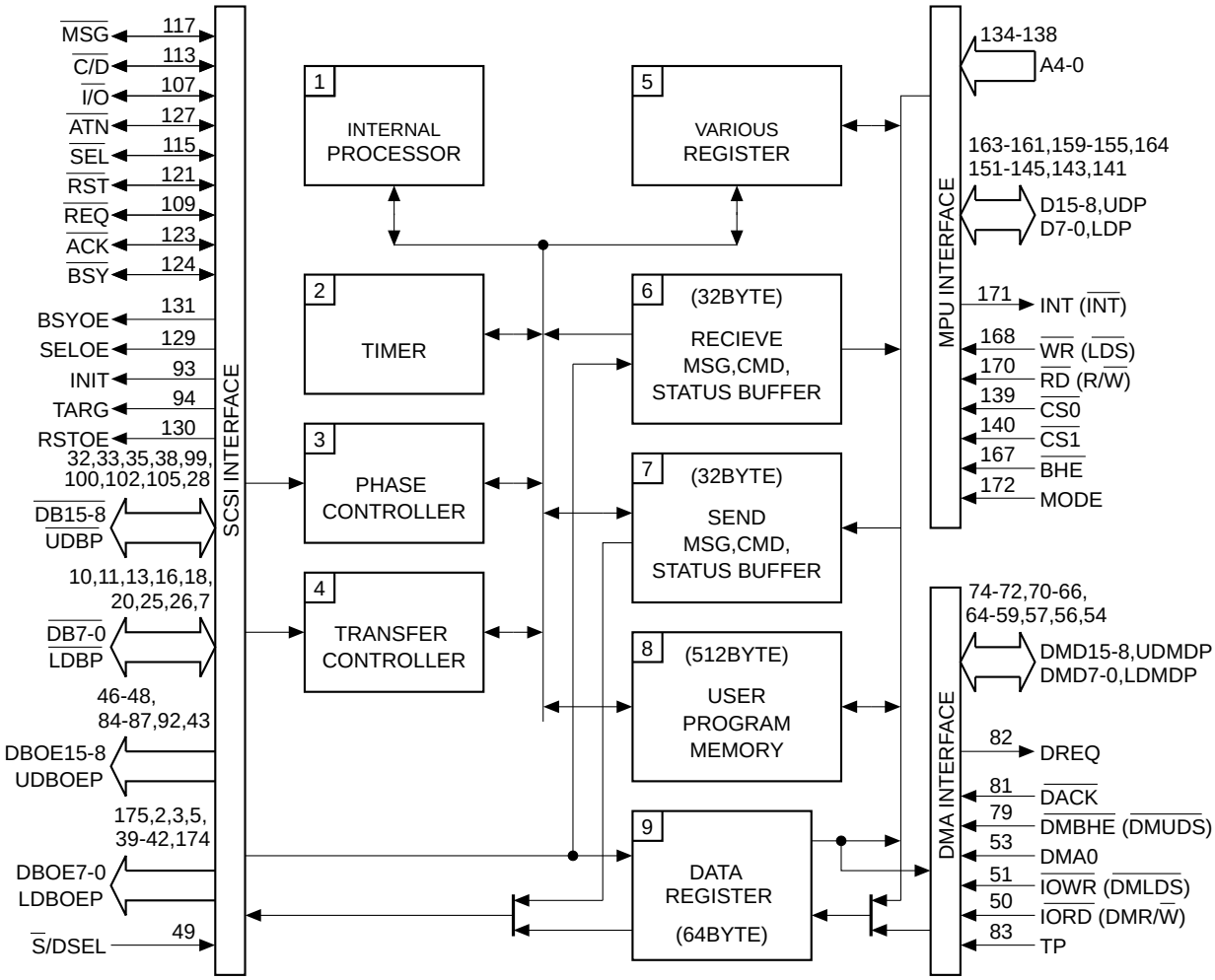
A0-A4	; ADDRESS 0-4
$\overline{BHE}$ ($\overline{UDS}$)	; BUS HIGH ENABLE (UPPER DATA STROBE)
CLK	; CLOCK
$\overline{CS0}$,$\overline{CS1}$	; CHIP SELECT 0,1
$\overline{DACK}$	; DMA ACKNOWLEDGE
DMA0	; DMA ADDRESS 0
$\overline{DMBHE}$ ($\overline{DMUDS}$)	; DMA BUS HIGH ENABLE (DMA UPPER DATA STROBE)
$\overline{IORD}$ (DMR/$\overline{W}$)	; I/O READ (DMA READ/WRITE)
$\overline{IOWR}$ ($\overline{DMLDS}$)	; I/O WRITE (DMA LOWER DATA STROBE)
MODE	; MODE
$\overline{RD}$ (R/$\overline{W}$)	; READ (READ/WRITE)
$\overline{S}$/DSEL	; SINGLE-END DIFFERENTIAL SELECT
TP	; TRANSFER PERMISSION
TEST2	; TEST
$\overline{WR}$ ($\overline{LDS}$)	; WRITE (LOWER DATA STROBE)

OUTPUT

BSYOE	; BUSY OUTPUT ENABLE
$\overline{DBOE0\text{-}7}$	; DATA BUS0-7 ENABLE
$\overline{DBOE8\text{-}15}$	; DATA BUS8-15 ENABLE
DREQ	; DMA REQUEST
INIT	; INITIATOR
INT ($\overline{INT}$)	; INTERRUPT REQUEST
LDBOEP	; LOWER DATA BUS OUTPUT ENABLE PARITY
RSTOE	; RESET OUTPUT ENABLE
SELOE	; SELECT OUTPUT ENABLE
TARG	; TARGET
UDBOEP	; UPPER DATA BUS OUTPUT ENABLE PARITY

INPUT/OUTPUT

$\overline{ACK}$	; ACKNOWLEDGE
$\overline{ATN}$	; ATTENTION
$\overline{BSY}$	; BUSY
$\overline{C/D}$	; CONTROL/DATA
D0-D7	; DATA 0-7
D8-15	; DATA 8-15
$\overline{DB0\text{-}7}$	; DATA BUS0-7
$\overline{DB8\text{-}15}$	; DATA BUS 8-15
DMD0-7	; DMA DATA 0-7
DMD8-15	; DMA DATA 8-15
$\overline{I/O}$	; INPUT/OUTPUT
LDP	; LOWER DATA PARITY
$\overline{LDBP}$	; LOWER DATA BUS PARITY
LDMDP	; LOWER DMA DATA PARITY
$\overline{MSG}$	; MESSAGE
$\overline{REQ}$	; REQUEST
$\overline{RESET}$	; RESET
$\overline{RST}$	; RESET
$\overline{SEL}$	; SELECT
UDP	; UPPER DATA PARITY
$\overline{UDBP}$	; UPPER DATA BUS PARITY
UDMDP	; UPPER DMA DATA PARITY


MSG 117
C/D 113
I/O 107
ATN 127
SEL 115
RST 121
REQ 109
ACK 123
BSY 124
BSYOE 131
SELOE 129
INIT 93
TARG 94
RSTOE 130
32,33,35,38,99,
100,102,105,28
DB15-8
UDBP
10,11,13,16,18,
20,25,26,7
DB7-0
LDBP
46-48,
84-87,92,43
DBOE15-8
UDBOEP
175,2,3,5,
39-42,174
DBOE7-0
LDBOEP
S/DSEL 49
SCSI INTERFACE
1 INTERNAL PROCESSOR
2 TIMER
3 PHASE CONTROLLER
4 TRANSFER CONTROLLER
5 VARIOUS REGISTER
6 (32BYTE) RECIEVE MSG,CMD, STATUS BUFFER
7 (32BYTE) SEND MSG,CMD, STATUS BUFFER
8 (512BYTE) USER PROGRAM MEMORY
9 DATA REGISTER (64BYTE)
MPU INTERFACE
134-138
A4-0
163-161,159-155,164
151-145,143,141
D15-8,UDP
D7-0,LDP
171 INT (INT)
168 WR (LDS)
170 RD (R/W)
139 CS0
140 CS1
167 BHE
172 MODE
DMA INTERFACE
74-72,70-66,
64-59,57,56,54
DMD15-8,UDMDP
DMD7-0,LDMDP
82 DREQ
81 DACK
79 DMBHE (DMUDS)
53 DMA0
51 IOWR (DMLDS)
50 IORD (DMR/W)
83 TP