NEC

NEC Electronics Inc.

μPD42101
Line Buffer for NTSC TV

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Description

The μPD42101 is a 910-word by 8-bit line buffer fabricated with a CMOS silicon-gate process. The device helps to create an NTSC flicker-free television picture (noninterlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD42101 can also be used as a digital delay line. The delay length is variable from 10 bits (at maximum clock speed) to 910 bits.

Features

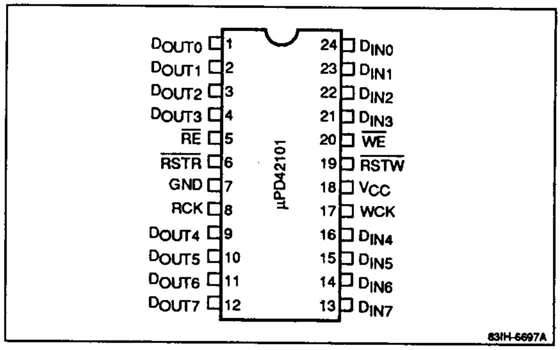
- 910-word x 8-bit organization
- Line buffer for NTSC, $4f_{SC}$ digital television systems
- Asynchronous, simultaneous read/write operation
- 1H (910-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 24-pin plastic DIP and miniflat packaging

Ordering Information

Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD42101C-3	34 ns	34 ns	24-pin plastic DIP
C-2	34 ns	69 ns	
C-1	69 ns	69 ns	
μPD42101G-3	34 ns	34 ns	24-pin plastic miniflat
G-2	34 ns	69 ns	
G-1	69 ns	69 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

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PIN FUNCTIONS

D_{IN0} - D_{IN7} (Data Inputs)

In a digital television application, the digital composite signal, luminance, chrominance, etc. information is written into these inputs.

D_{OUT0} - D_{OUT7} (Data Outputs)

The tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ (Write Address Reset Input)

Bringing this signal low when $\overline{WE}$ is also low resets the internal write address to 0. If $\overline{WE}$ is at a high level when the $\overline{RSTW}$ input is brought low, the internal write address is set to 909. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ (Read Address Reset Input)

This signal is strobed by the rising edge of RCK and resets the internal read address to 0 if $\overline{RE}$ is also low. If $\overline{RE}$ is at a high level when the $\overline{RSTR}$ input is brought low, the internal read address is set to 909.

$\overline{WE}$ (Write Enable Input)

This input controls write operation. If $\overline{WE}$ is low, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ (Read Enable Input)

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the data outpus become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK (Write Clock Input)

All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 909 to 0 and begin increasing again.

RCK (Read Clock Input)

All read cycles are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 909 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltages on any input pin, V_I	−1.5 to + 7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

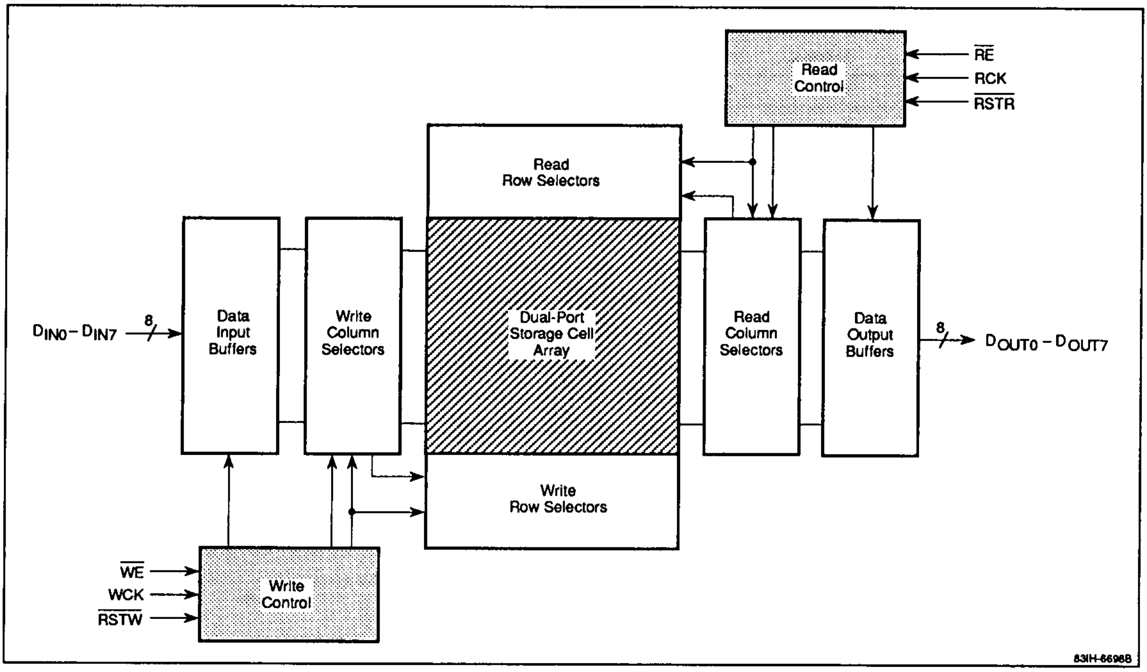
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Pins Under Test
Input capacitance	C_I		5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O		7	pF	D_{OUT0} - D_{OUT7}

Block Diagram



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DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_I	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD42101-3		μPD42101-2		μPD42101-1			
Parameter	Symbol	min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}		70		60		35	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)
Write clock cycle time	t_{WCK}	34	1090	69	1090	69	1090	ns	
WCK pulse width	t_{WCW}	14		25		25		ns	
WCK precharge time	t_{WCP}	14		25		25		ns	
Read clock cycle time	t_{RCK}	34	1090	34	1090	69	1090	ns	
RCK pulse width	t_{RCW}	14		14		25		ns	
RCK precharge time	t_{RCP}	14		14		25		ns	
Access time	t_{AC}		27		27		49	ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42101-3 min	μPD42101-3 Max	μPD42101-2 Min	μPD42101-2 Max	μPD42101-1 Min	μPD42101-1 Max	Unit	Test Conditions
Output hold time	t_{OH}	5		5		5		ns	
Output active time	t_{LZ}	5	27	5	27	5	49	ns	(Note 5)
Output disable time	t_{HZ}	5	27	5	27	5	49	ns	(Note 5)
Data-in setup time	t_{DS}	14		18		18		ns	
Data-in hold time	t_{DH}	5		5		5		ns	
Reset active setup time	t_{RS}	14		14		20		ns	(Note 7)
Reset active hold time	t_{RH}	5		5		5		ns	(Note 7)
Reset inactive hold time	t_{RN1}	5		5		5		ns	(Note 8)
Reset inactive setup time	t_{RN2}	14		14		20		ns	(Note 8)
Write enable setup time	t_{WES}	14		20		20		ns	(Note 9)
Write enable hold time	t_{WEH}	5		5		5		ns	(Note 9)
Write enable high delay from WCK	t_{WEN1}	5		5		5		ns	(Note 10)
Write enable low delay to WCK	t_{WEN2}	14		20		20		ns	(Note 10)
Read enable setup time	t_{RES}	14		14		20		ns	(Note 9)
Read enable hold time	t_{REH}	5		5		5		ns	(Note 9)
Read enable high delay from RCK	t_{REN1}	5		5		5		ns	(Note 10)
Read enable low delay to RCK	t_{REN2}	14		14		20		ns	(Note 10)
Write disable pulse width	t_{WEW}	0		0		0		ns	(Note 6)
Read disable pulse width	t_{REW}	0		0		0		ns	(Note 6)
Write reset time	t_{RSTW}	0		0		0		ns	(Note 6)
Read reset time	t_{RSTR}	0		0		0		ns	(Note 6)
Transition time	t_T	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) After power-up, a read reset cycle and a write reset cycle must be executed before proper device operation is achieved.

(3) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V. See figure 1.

(4) Input timing reference levels = 1.5 V. Output timing reference levels are 0.8 and 2.0 V. See figure 2.

(5) This delay is measured at 200 mV from the steady-state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1-line cycle operation:
$t_{WEW} + t_{RSTW} + 910\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 910\ (t_{RCK}) \leq 1$ ms

(7) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(8) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(9) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(10) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(11) Data is guaranteed to remain valid for a minimum of 1 ms after it is written. After this time, the data stored may be discharged, since this device uses a dynamic storage element.

Figure 1. Input Timing

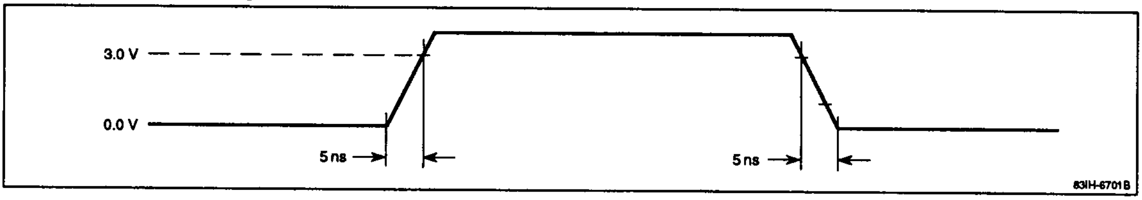


Figure 2. Output Timing

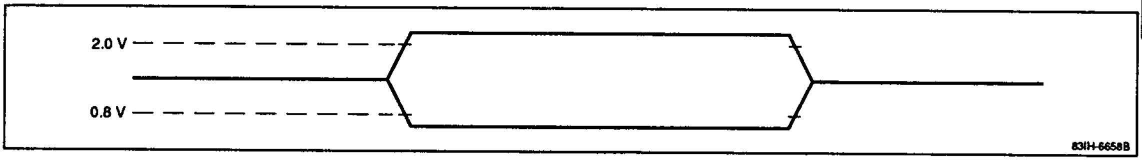


Figure 3. Output Load for t_{AC} and t_{OH}

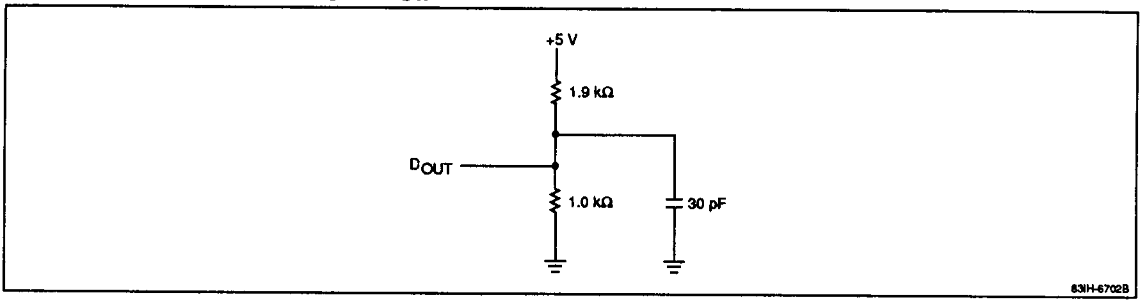
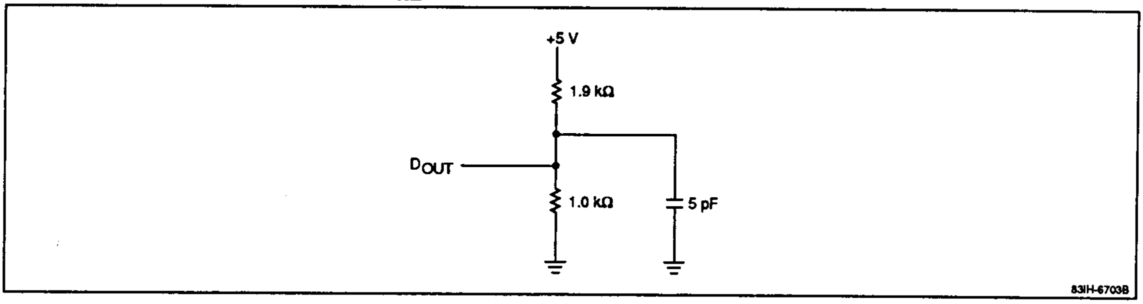
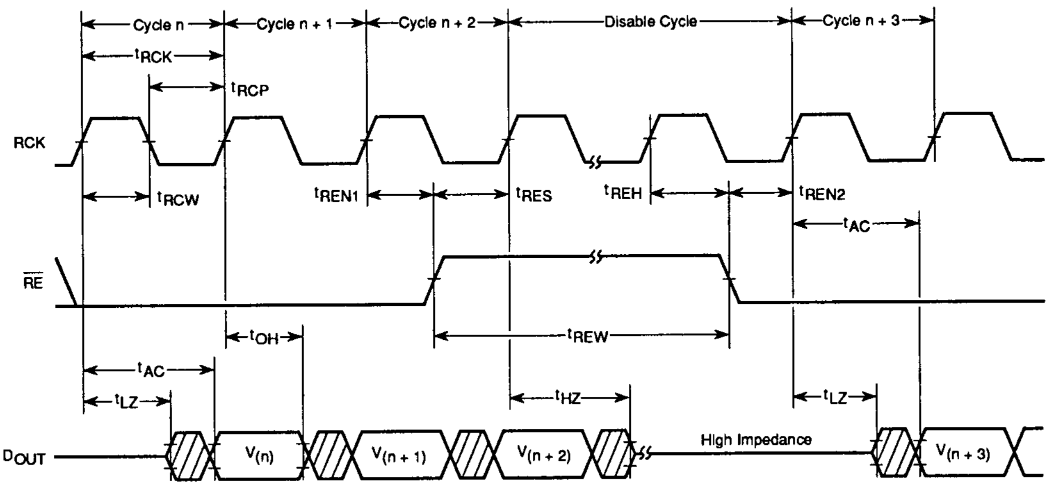


Figure 4. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

Read Cycle



Notes:

[1] $\overline{RSTR} = V_{IH}$.

[2] V = valid data.

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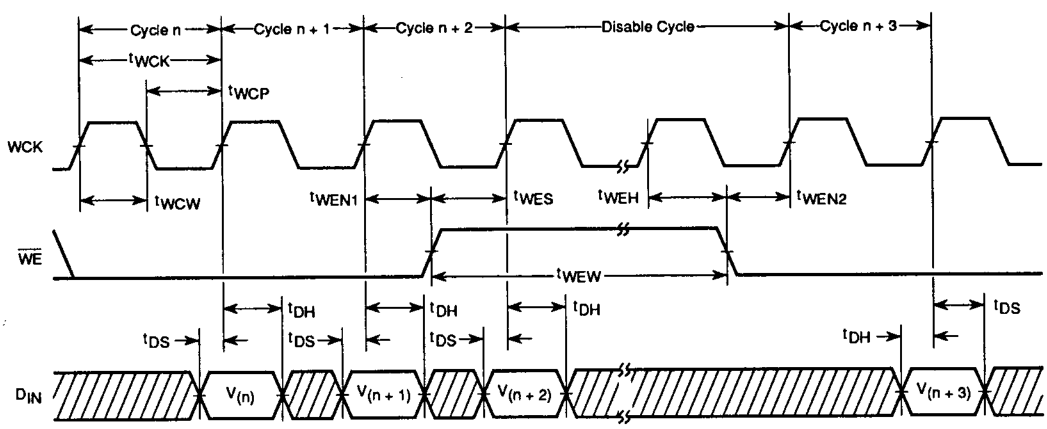
Write Cycle



Notes:

[1] $\overline{RSTW} = V_{IH}$.

[2] V = valid data.

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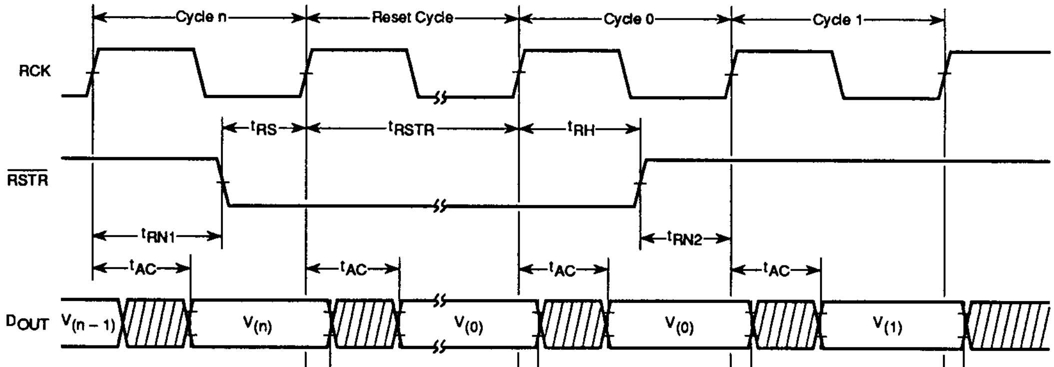
Timing Waveforms (cont)

Read Reset Cycle



Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = valid data.

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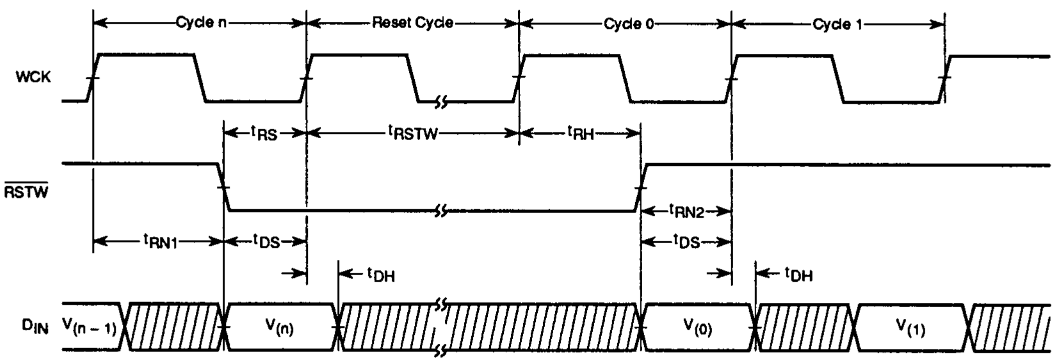
Write Reset Cycle



Note:
[1] $\overline{WE}$ = V_{IL}.
[2] V = valid data.

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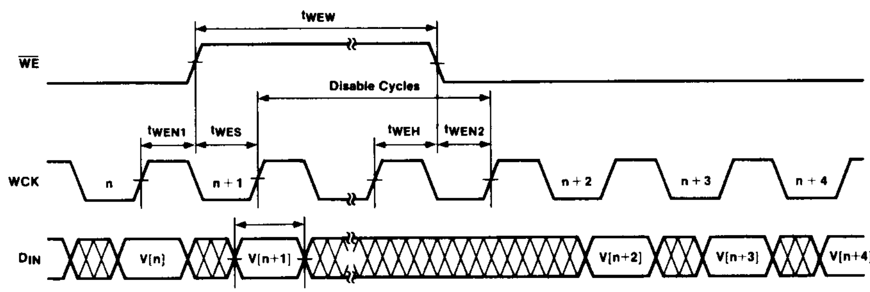
Timing Waveforms (cont)

Write Disable Cycle



Note:
[1] V = Valid Data.

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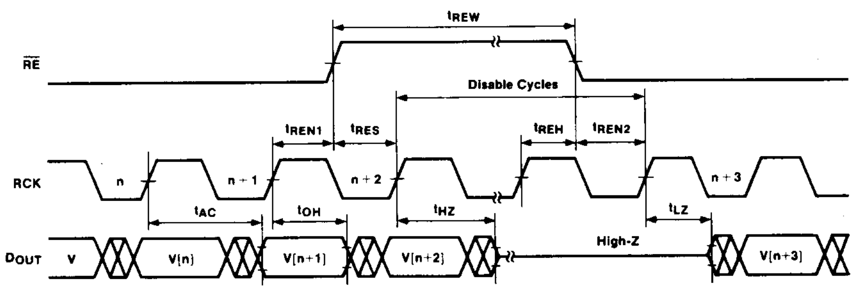
Read Disable Cycle



Note:
[1] V = Valid Data.

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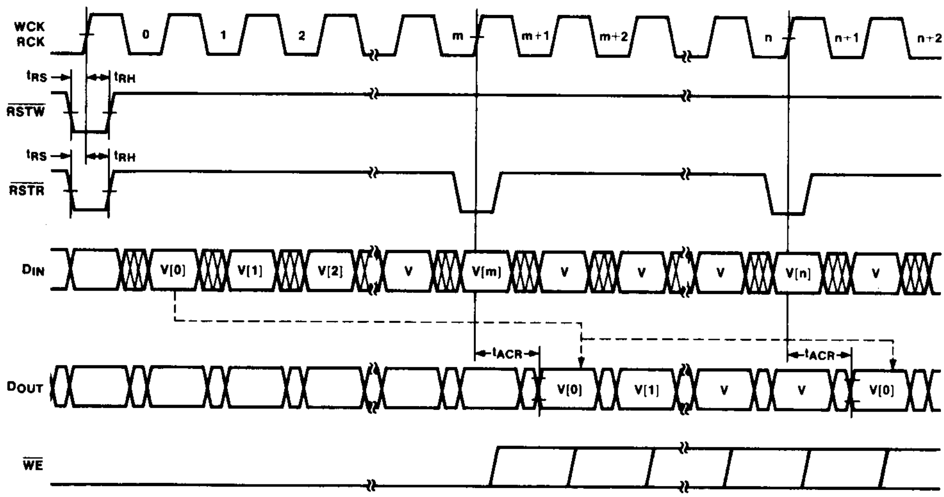
Timing Waveforms (cont)

Re-Read Cycle



Note:

[1] $\overline{RE}$ = V_{IL}.

[2] V = Valid Data.

[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

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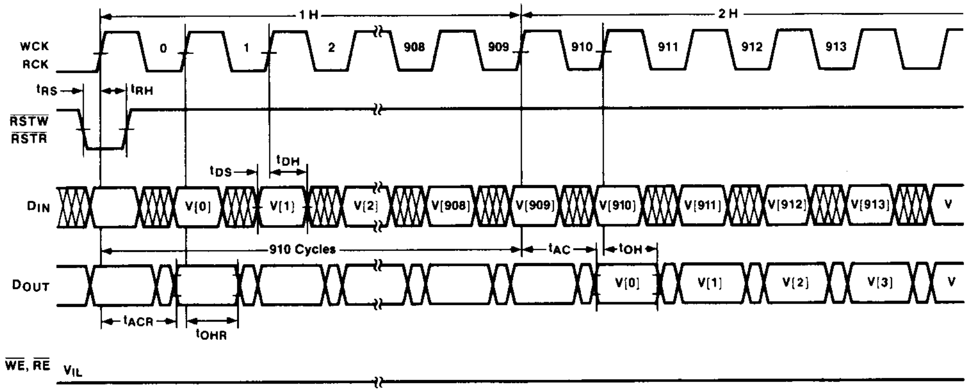
Timing Waveforms (cont)

910-Bit Delay Line Cycle



Note:
[1] V = Valid Data.
[2] 1H = the first group of 910 bits. 2H = the second group of 910 bits.

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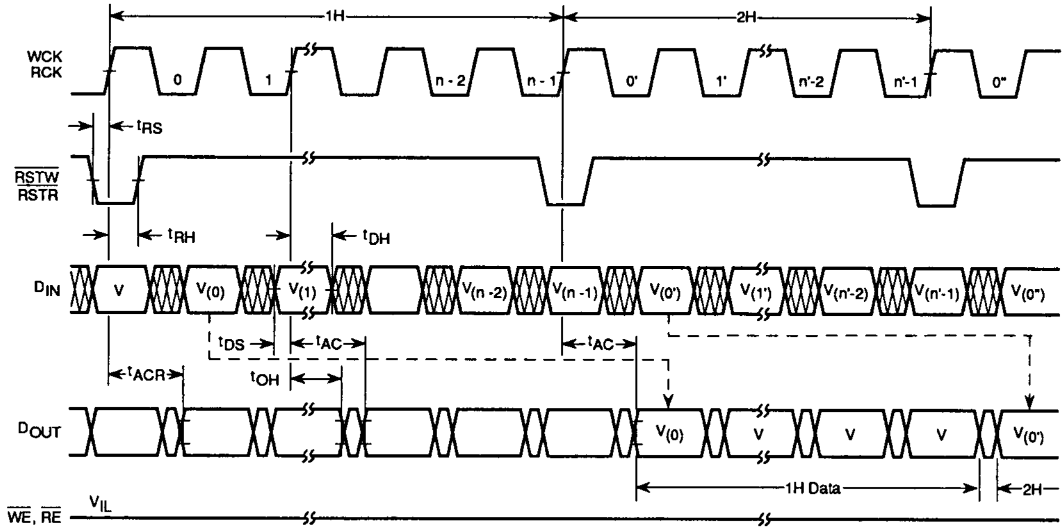
Timing Waveforms (cont)

n-Bit Delay Line Cycle



Notes:

[1] V = valid data

[2] 1H = the first group of bits. 2H = the second group of n' bits.

[3] $\overline{RE} = \overline{WE} = V_{IL}$.

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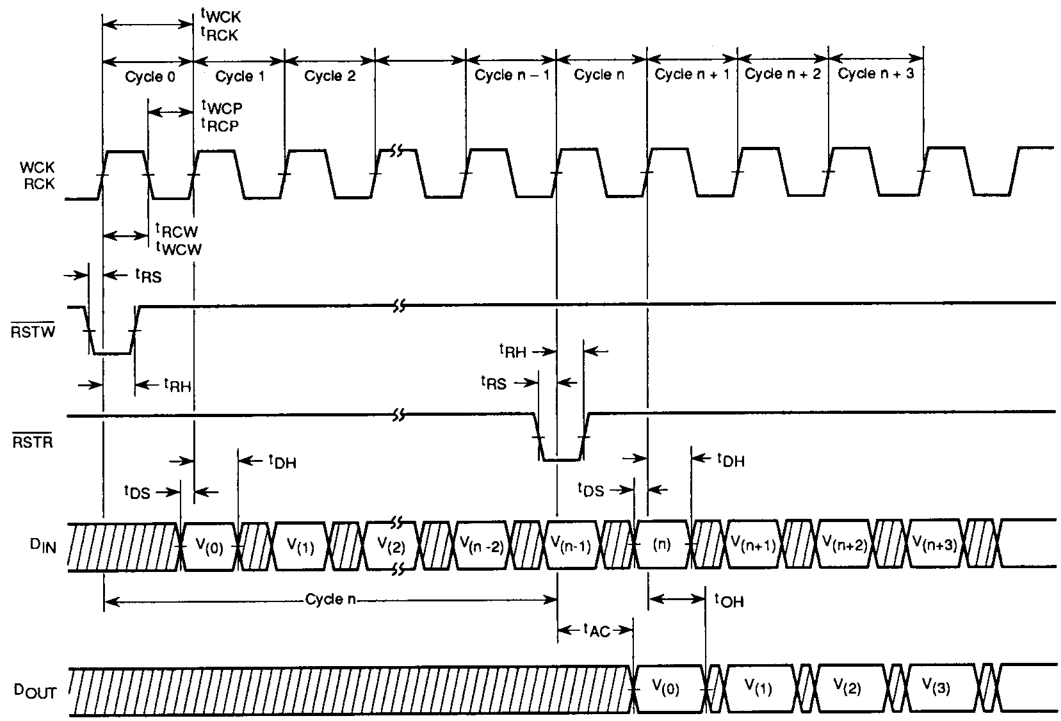
Timing Waveforms (cont)

n-Bit Delay Line Timing Cycle (1)



Notes:

[1] $\overline{RE}$ and $\overline{WE}$ = V_{IL}.

[2] V = valid data.

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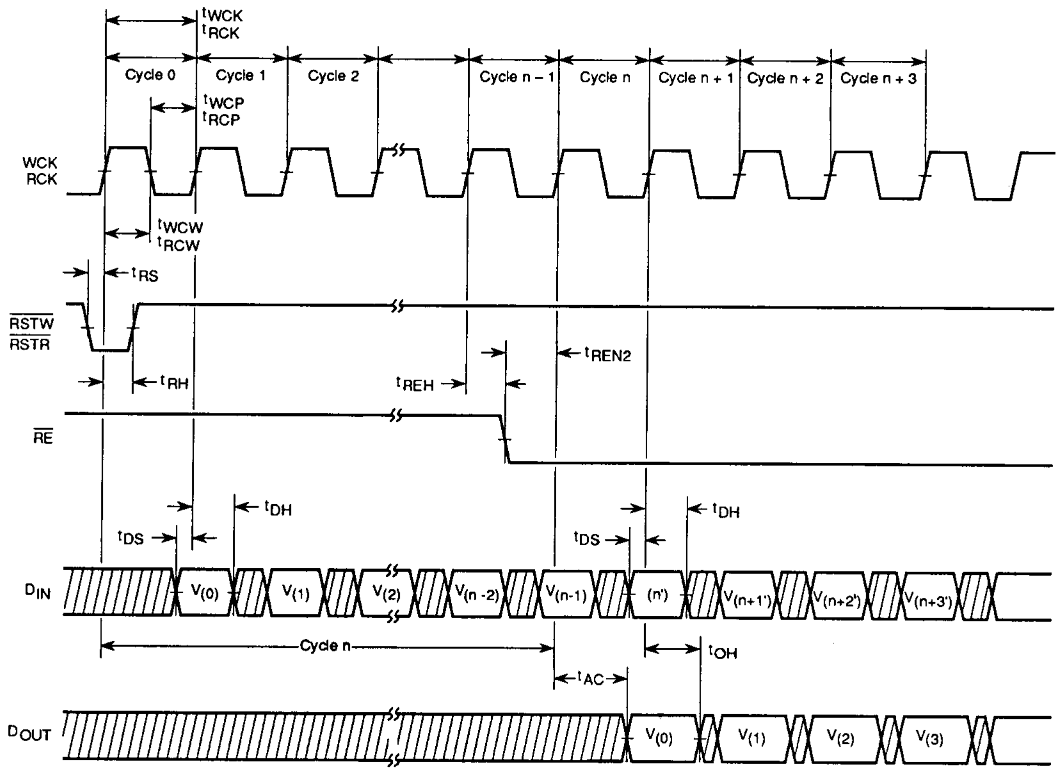
Timing Waveforms (cont)

n-Bit Delay Line Timing Cycle (2)



Notes:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

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Applications

1H (910-bit) Delay Line

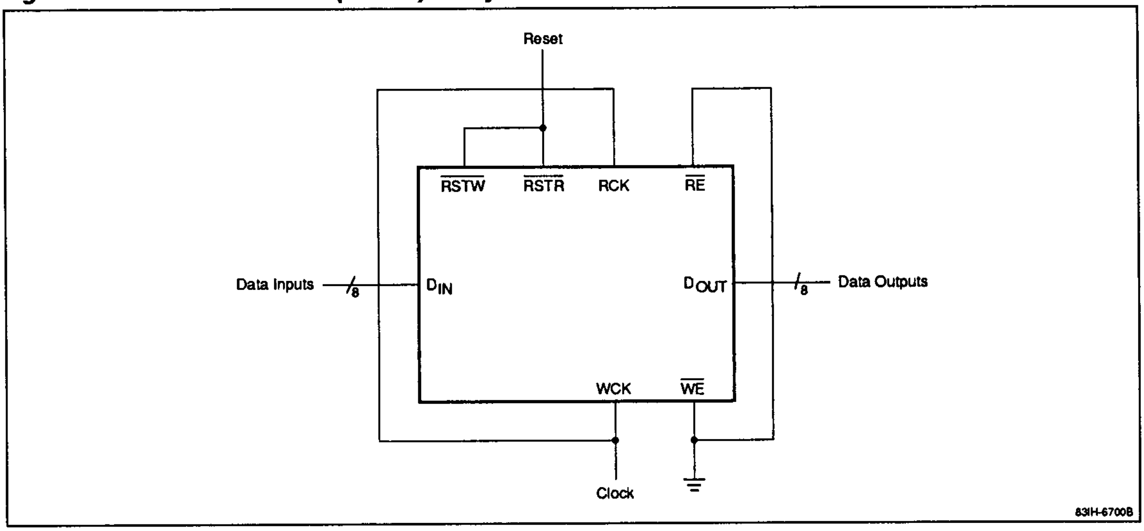
Any one of the following methods may be used to configure a 1H (910-bit) delay line, or to vary the number of delay bits from a minimum of 5 (when operating at $4f_{SC}$) to a maximum of 910 (figure 5).

(1) Execute a reset cycle proportionate to the desired delay length.

(2) Adjust the input timing of $\overline{RSTW}$ and $\overline{RSTR}$ to the desired delay length (see waveform for n-bit Delay Line Timing 1).

(3) Adjust the address by disabling $\overline{WE}$ or $\overline{RE}$ for a period proportionate to the desired delay length.

Figure 5. Connection of a 1H (910-bit) Delay Line

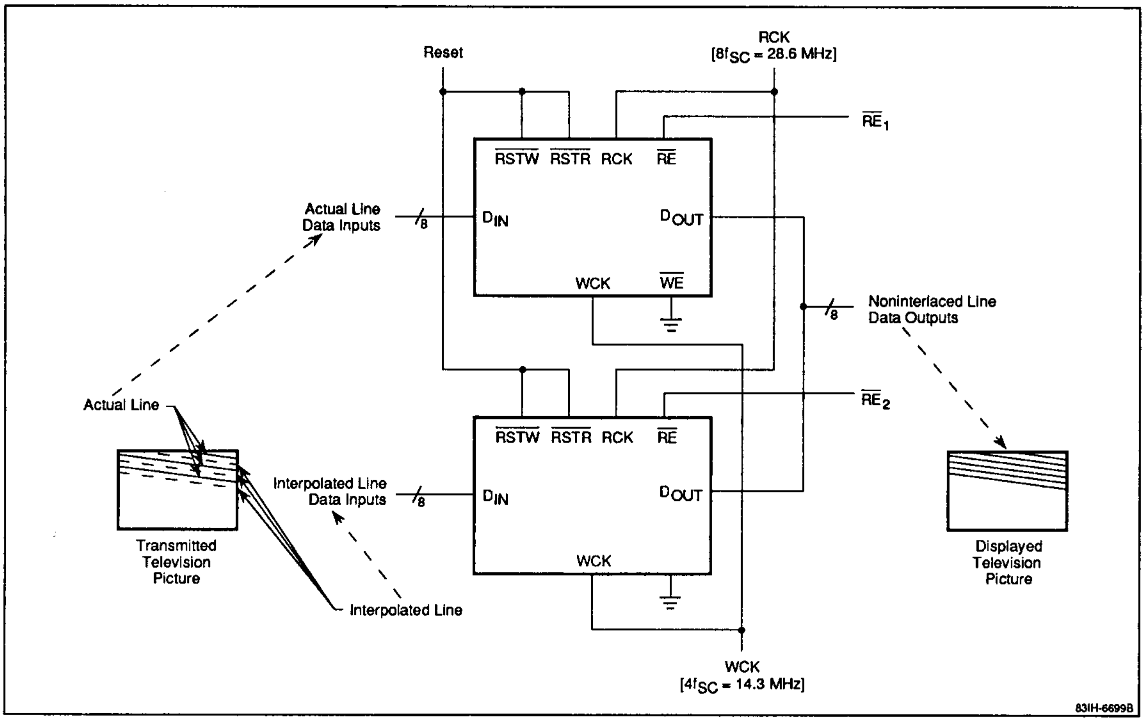


Applications (cont)

Noninterlaced Scan Conversion

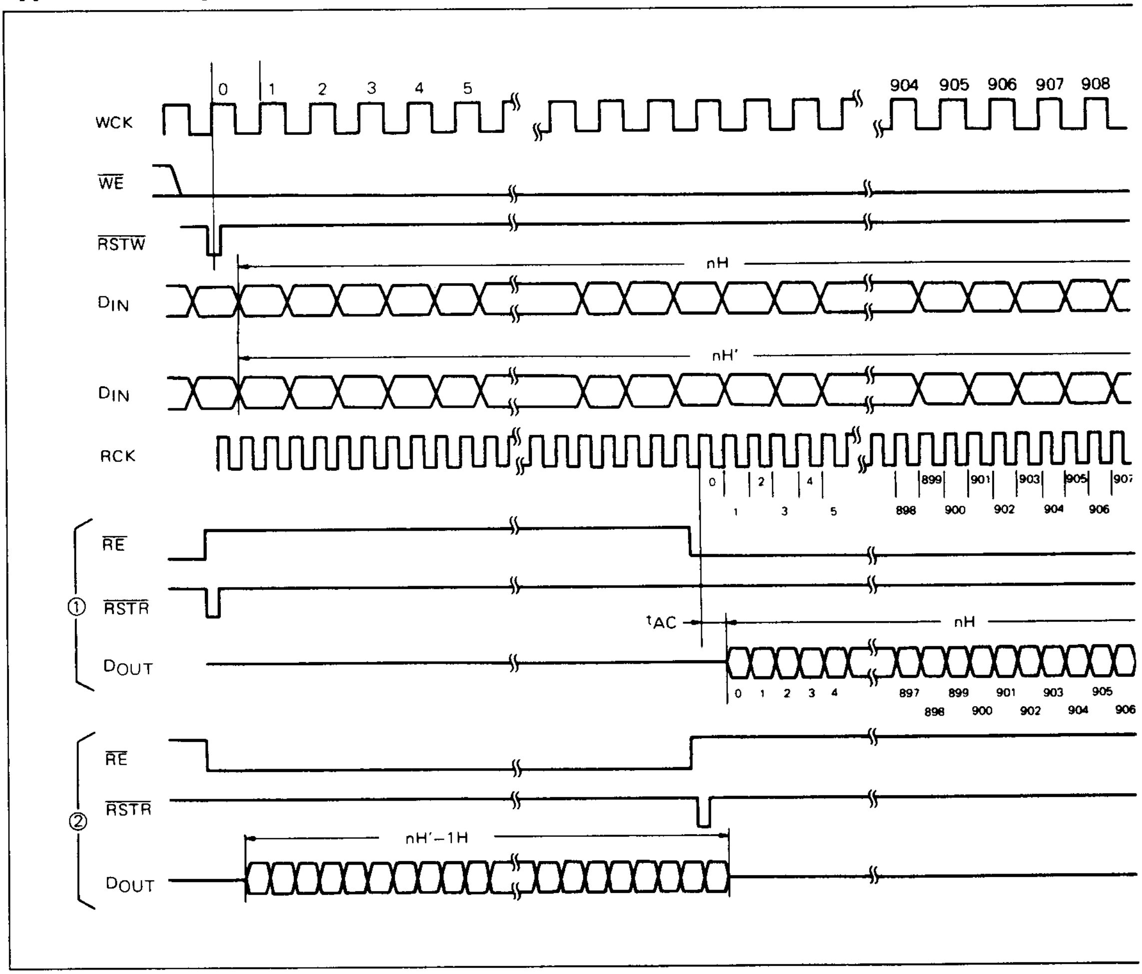
It is also possible to use either one or two μPD42101s for noninterlaced scan conversion. If one device is used, the same data is read twice at 28.6 MHz ($8f_{SC}$) to prepare it for writing at 14.3 MHz ($4f_{SC}$). If two devices are used as shown in figure 6, data input at 14.3 MHz is read alternately at 28.6 MHz with $\overline{RE}$. Actual line signals and complement line signals are entered as input data. Complement signals can also be obtained using the μPD42101 if resetting is performed for each line. A single signal type is assumed in this case. In actual applications, noninterlaced scan conversion with brightness (Y) and color difference (C) and RGB signals will require as many as two or three times the number of μPD42101 devices shown in this example.

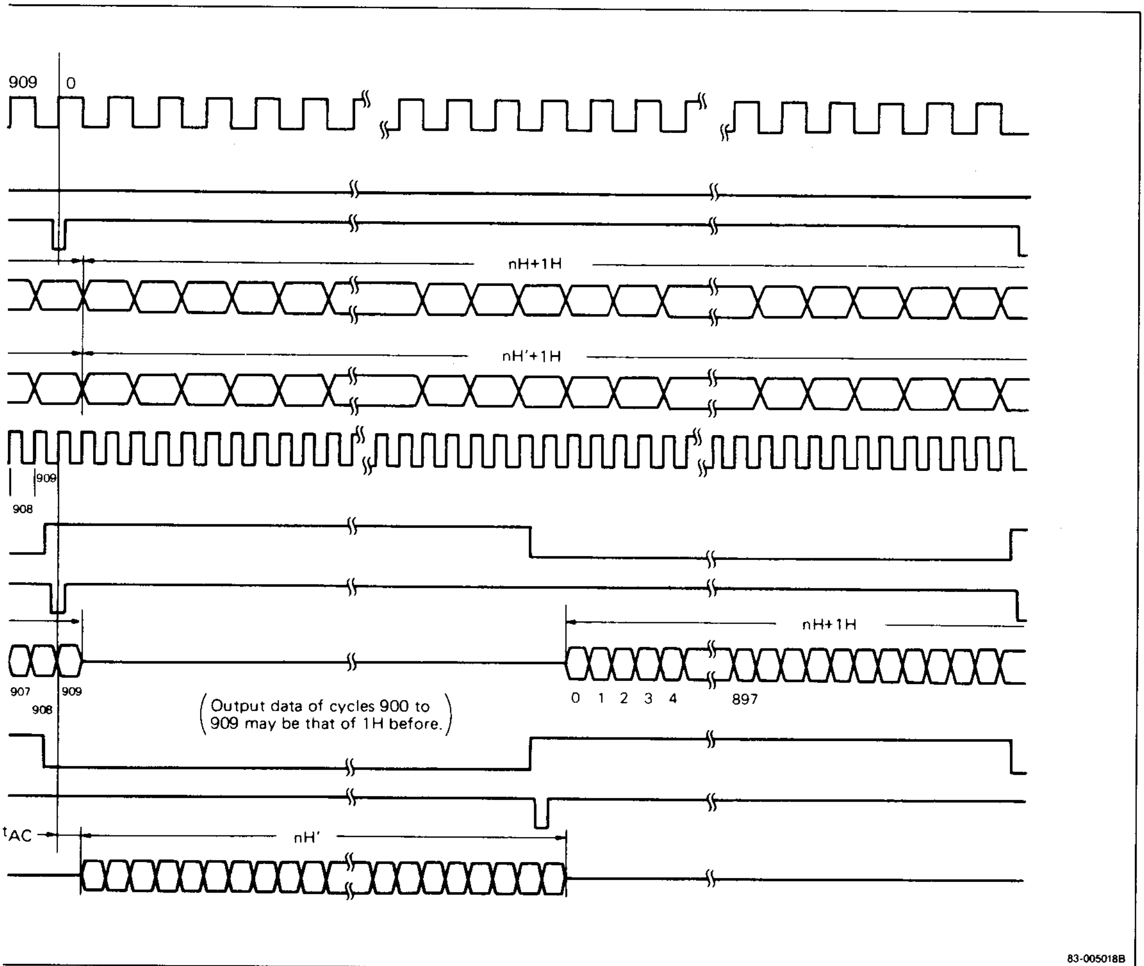
Figure 6. Example of Noninterlaced Scan Conversion



Timing Waveforms (cont)

Application Timing for Noninterlaced Scan Conversion




909
0
nH+1H
nH'+1H
909
908
nH+1H
907
909
908
0 1 2 3 4
897
(Output data of cycles 900 to 909 may be that of 1H before.)
tAC
nH'
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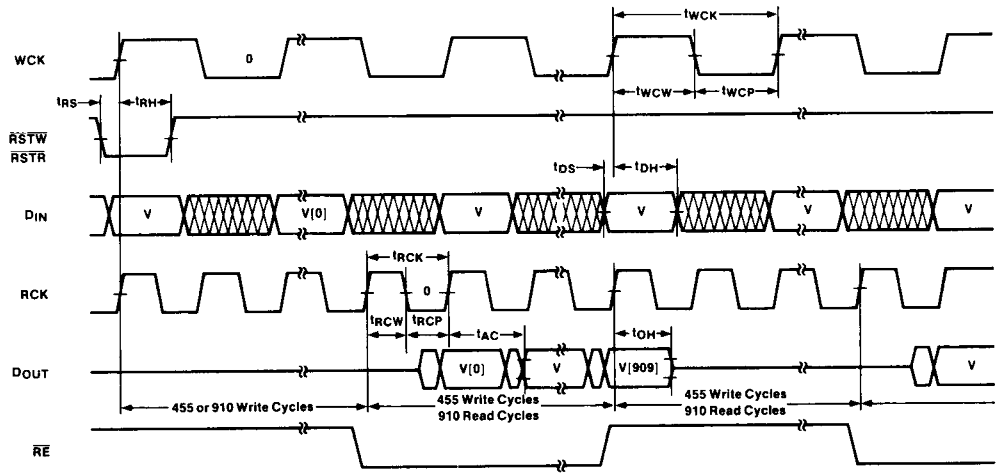
Timing Waveforms (cont)

Basic Timing for Noninterlaced Scan Conversion



Note:

[1] $\overline{WE} = V_{IL}$.

[2] V = Valid Data.

[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

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