CZ80CPU
8-Bit Microprocessor Megafunction

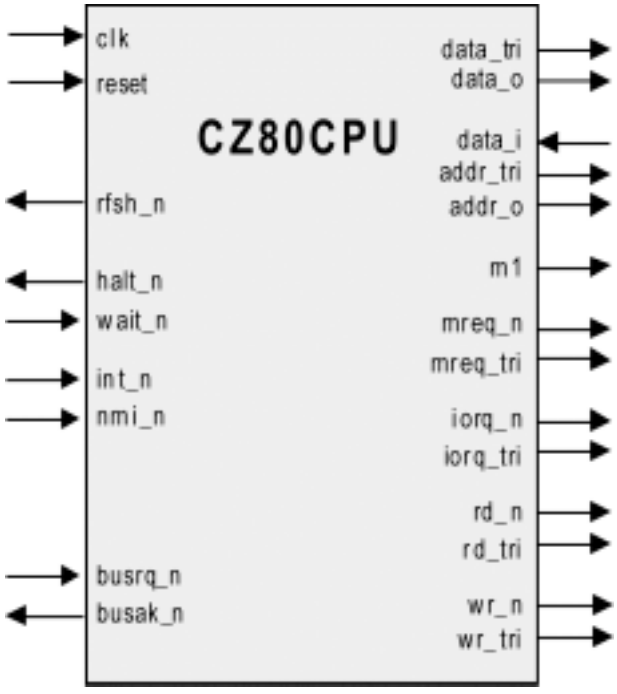
General Description

Implements a fast, fully-functional, single-chip, 8-bit microprocessor with the same instruction set as the Z80.

The core has a 16-bit address bus capable of directly accessing 64kB of memory space. It has 252 root instructions with the reserved 4 bytes as prefixes, and accesses an additional 308 instructions.

The microcode-free design was developed for reuse in ASIC and FPGA implementations. It is strictly synchronous, with no internal tri-states and a synchronous reset.

Symbol



Features

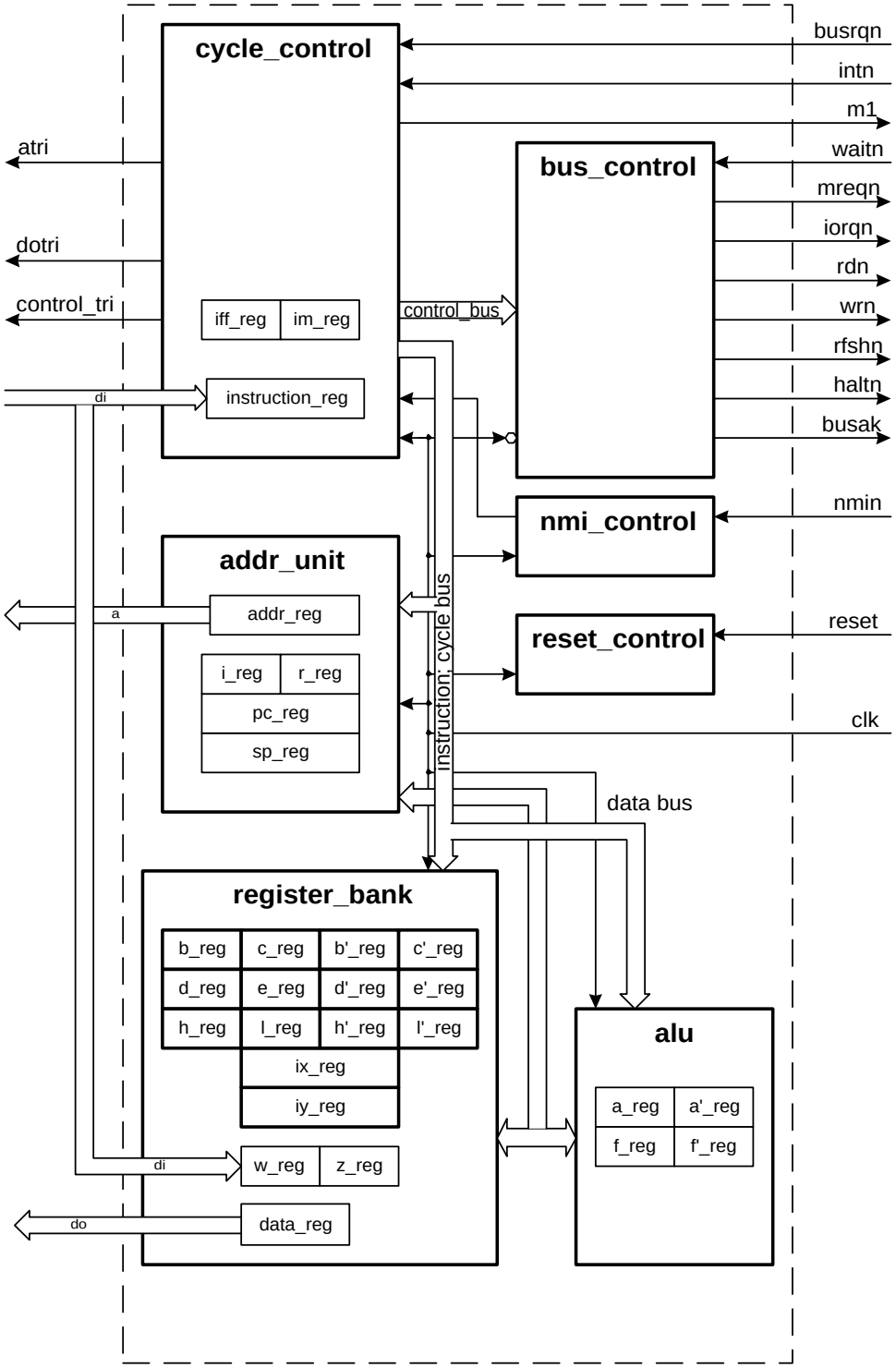
Programming features contain 208 bits of read/write memory that are accessible to the programmer. The internal registers include an accumulator and six 8-bit registers that can be paired as three 16-bit registers. In addition to general registers, a 16-bit stack-pointer, 16-bit program-counter, and two 16-bit index registers are provided.

- Control Unit
  - 8-bit Instruction decoder
- Arithmetic-Logic Unit
  - 8-bit arithmetic and logical operations
  - 16-bit arithmetic operations
  - Boolean manipulations
- Register File Unit
  - Duplicate set of both general purpose and flag registers
  - Two 16-bit index registers
- Interrupt Controller
  - Three modes of maskable interrupts
  - Non maskable interrupt
- External Memory interface
  - Can address up to 64 KB of program memory
  - Can address up to 64 KB of data memory
  - Can address up to 64 KB of input/output devices
- On-core dynamic memory refresh counter

Applications

Suitable for many embedded controller applications, including industrial control systems, point-of-sale terminals, and automotive controls.

Block Diagram



Pin Description

Name	Type	Polarity/ Bus size	Description
clk	I	Rise	**Clock** Feeds internal clock counters and all synchronous circuits.
reset	I	High	**Hardware reset input** A high on this pin for two clock cycles while the oscillator is running resets the device.
wait_n	I	Low	**Wait** A low on this pin indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a wait state as long as this signal is active.
int_n	I	Low	**Interrupt Request** This signal is generated by an I/O device. The CPU honors a request at the end of the current instruction, if the internal software-controlled interrupt enable flip-flop is enabled.
nmi_n	I	Low	**Non-maskable Interrupt** This pin has a higher priority then int_n and is always recognized at the end of the current instruction independent of the status of the interrupt enable flip-flop and forced the CPU to restart at address 0066h.
busreq_n	I	Low	**Bus Request** It has higher priority than nmi_n and is always recognized at the end of the current machine cycles. Active state on this pin forces the CPU address bus, data bus, and control signal to go to a high-impedance state, so that other devices can control these lines.
busak_n	O	Low	**Bus Request Acknowledgment** Low on this pin indicates to the requesting device that the CPU address bus, data bus, and control signal have entered their high-impedance state and it can now control these lines.
m1	O	High	**Machine Cycles One** This pin together with mreq_n indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. It together with iorq_n indicates an interrupt acknowledge cycle.
addr_o addr_tri	O O	8 High	**Address Bus** Addr_o forms a 16-bit address bus. The address bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.
data_i data_o data_tri	I O O	8 8 High	**Data Bus** (input/output, 3-state) 8-bit bidirectional data bus, used for data exchanges with memory and I/O.
mreq_n mreq_tri	O O	Low High	**Memory Request** Indicates that the address bus holds a valid address for memory read or memory write operation.
ioreq_n ioreq_tri	O O	Low High	**I/O Request** Indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation.
rd_n rd_tri	O O	Low High	**Read** rd_n indicates that the CPU wants to read data from memory, or that an I/O device or memory should use this signal to gate data onto the CPU data bus.
wr_n wr_tri	O O	Low High	**Write** Indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O device.
rfsh_n	O	Low	**Refresh Timing** This signal together with mreq_n, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.
halt_n	O	Low	**Halt** State low on this pin indicates that the CPU has executed a Halt instruction and is awaiting either a nonmaskable or a maskable interrupt before operation can resume.

Functional Description

The CZ80CPU core is partitioned into modules as shown in the Block Diagram and described below.

Cycle Control

The main control machine, which synchronizes all the others. It has an instruction register and all registers controlled interrupts, bus request cycle, wait states etc. This unit controls bus control signals too.

Bus Control

Registers are triggered on the falling edge and or gates. These are used to form the bus control timing, changed on both clock edges. This is the only unit that has registers synchronized on the falling clock edge.

Address Unit

This unit controls all operations on addresses (calculates the next instruction address, nested data address, jump and return address etc.) and increments and decrements the 16-bit addr register. It includes pc_reg (program counter), sp_reg (stack pointer), i_reg (interrupt register) and r_reg (refresh register).

NMI Control

This unit detects a falling edge on the nmin pin. If detected, the internal nmi register is set and this causes a non-maskable interrupt service cycle.

Reset Control

This unit controls the state of external signal resetn. If it has value '0' for at least three full clock cycles, then it sets the internal synchronous reset signal (rst) to '1.'

Register Bank

This includes all the commonly used registers (based and alternative) and the logic element needed to change the data in these registers.

Arithmetic-Logic Unit (ALU)

The unit accumulator and flag registers, and performs 8-bit arithmetic and logic operations, 16-bit arithmetic operations (without increment and decrement), bit operations, and sets the flag register.

Verification Methods

The CZ80CPU core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Zilog Z84C00 chip, and the results compared with the core's simulation outputs.

Device Utilization & Performance

The CZ80CPU is designed to run at frequencies up to 80 MHz on a typical 0.5-micron process and it uses less than 8K gates depending on the technology. The CZ80CPU is a technology independent design that can be implemented in a variety of process technologies.

Supported Family	Device Tested	Utilization			Performance
		LEs	Memory	Memory bits	F_{max}
Cyclone	EP1C6-6	3897	-	-	82 MHz
Stratix	EP1S10-5	3621	-	-	99 MHz
Stratix-II	EP2S15-3	3048	-	-	138 MHz

Note: Results optimized for speed

Deliverables

- VHDL or Verilog HDL source code
- Post-synthesis EDIF netlist (netlist license)
- Testbench (self-checking)
- Vectors for testing the core
- Place & route scripts (netlist license)
- Simulation script
- Synthesis script
- Documentation

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This megafunction developed by the processor experts at Evatronix SA